SIEMENS

ICs for Entertainment Electronics

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Siemens Aktiengesellschaft

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Contents
Summary of Types

Contents

1 Summary of types **Page**

1.1 Types in alphanumerical order 9
1.2 ICs in TV sets (Summary) 13
1.2.1 ICs in TV sets (in application-oriented order) 14
1.3 ICs in radio sets (Summary) 17
1.3.1 ICs in radio sets (in application-oriented order) 18
1.4 ICs for general purpose applications 19

2 General information

2.1 Type designation code for ICs 23
2.2 Mounting instructions 23
2.3 Ultrasonic cleaning of integrated circuits 24
2.4 Processing guidelines for MOS ICs 24
2.5 Data classification 27
2.6 Quality specifications 28
2.7 Summary of terms and symbols 31

3 Technical data 35

4 System descriptions 641

5 Packaging information 651

6 List of Sales Offices 659

1.1 Types in alphanumerical order

	Type	Ordering code		Page
	S 041 E	Q67000-A694	FM IF amplifier with demodulator	35
	S 041 P	Q67000-A529	AM IF amplifier with demodulator	35
	S 042 E	Q67000-A627	Mixer	41
	S 042 P	Q67000-A335	Mixer	41
	S 0280	Q67000-A1264	IC for station decoding SK	46
	S 0281	Q67000-A1265	IC for message decoding DK	50
	S 551	Q67100-Z109	Message decoder for FM road traffic information service	53
	S 552	Q67100-Z110	Area decoder for FM road traffic information service	62
■	SAB 3209	Q67100-Y395	Infrared remote control system – receiver (3 analog functions)	69
	SAB 3210	Q67100-Y396	Infrared remote control system – transmitter	80
	SAB 4209	Q67100-Y460	Infrared remote control system – receiver (4 analog functions)	90
	SAS 560 S	Q67000-S30	Switching amplifier for 4-channel touch tuning	102
	SAS 570 S	Q67000-S31	Switching amplifier for 4-channel touch tuning	102
	SAS 580	Q67000-S28	Switching amplifier for 4-channel touch tuning	106
	SAS 590	Q67000-S29	Switching amplifier for 4-channel touch tuning	106
▼	SDA 2005	Q67100-Y502	Onscreen IC	114
	SDA 2006	Q67100-Q264	512-bit nonvolatile EAROM	124
	SDA 2008	Q67100-Y503	Infrared remote control system – transmitter	134
	SDA 2010	Q67120-C74	Application-oriented single chip microcomputer	151
	SDA 2014	Q67000-Y538	LED display driver incl. cascade connection	158
▼	SDA 2020	Q67120-C131	Application-oriented single chip microcomputer	166
▼	SDA 2030	Q67120-C132	Application-oriented single chip microcomputer	173
	SDA 2101	Q67000-A1753	Frequency divider 1 : 64 with preamplifier	180
	SDA 2110	Q67120-C73	Application-oriented single chip microcomputer	184
▼	SDA 2112-2	Q67000-A1778-E12	PLL IC for 125 kHz resolution	191
	SDA 2114 P	Q67000-A1859	Infrared diode driver IC incl. power-on transistor for PMOS control	201
▼	SDA 2116	Q67100-A2128	Nonvolatile memory 1 Kbit E^2PROM	206
	SDA 2120	Q67000-A1953	120 MHz PLL for AM/FM receivers	211
▼	SDA 2131	Q67000-A2044	Static LED display driver with blanking capability	224
▼	SDA 2201	Q67000-H2428	Frequency divider 1 : 64 with preamplifier	230
▼	SDA 2208	Q67000-A2201	Remote control transmitter with IR diode driver	234
▼	SDA 2311	Q67000-A2314	1 GHz divider 1 : 64 with preamplifier	243
▼	SDA 3002	Q67000-A2267	TV PLL	249
▼	SDA 3010	Q67120-C86	Application-oriented single chip microcomputer	259
▼	SDA 3110	Q67120-C87	Application-oriented single chip microcomputer	267

▼ New type
■ Not for new design

Summary of Types

	Type	Ordering code		Page
	SDA 3205	Q67100-Y578	Infrared remote control system – receiver	274
	SDA 3206	Q67100-Y577	Infrared remote control system – transmitter	283
■	SDA 4040	Q67000-A1462	UHF/VHF divider 1:256 with preamplifier	290
	SDA 4041	Q67000-A1463	UHF/VHF divider 1:256 with preamplifier	294
▼	SDA 4042	Q67000-A1892	Frequency divider 1:256 with preamplifier	299
	TBA 120 S	Q67000-A657	FM IF amplifier with demodulator	303
■	TBA 120 AS	Q67000-A716	FM IF amplifier with demodulator	303
	TBA 120 T	Q67000-A919	FM IF amplifier with demodulator	311
	TBA 120 U	Q67000-A920	FM IF amplifier with demodulator	311
▼	TBA 129	Q67000-A2330	FM IF amplifier with demodulator	321
	TBA 1440 G	Q67000-A1022	Video IF IC for black/white and color TV sets	324
	TBA 1441	Q67000-A1224	Video IF IC for black/white and color TV sets	324
	TCA 440	Q67000-A669	AM receiver circuit	330
	TCA 440 I	Q67000-A669-S2	AM receiver circuit	330
	TCA 440 II	Q67000-A669-S3	AM receiver circuit	330
	TCA 4500 A	Q67000-A1471	Stereo decoder	347
	TCA 4510	Q67000-A1533	PLL stereo decoder	351
▼	TCA 4511	Q67000-A1648	PLL stereo decoder	359
	TDA 1037	Q67000-A1229	AF power amplifier IC with thermal shutdown	367
	TDA 1037 D	Q67000-A1387	AF power amplifier IC with thermal shutdown	367
	TDA 1046	Q67000-A1092	AM receiver IC with demodulator	376
	TDA 1047	Q67000-A1091	FM IF amplifier with demodulator for radio receivers	385
	TDA 1048 G	Q67000-A1090	Controlled AM amplifier with demodulator and AF volume control	392
	TDA 2048	Q67000-A1773	Controlled AM amplifier for French sound IF standard	396
▼	TDA 2440	Q67000-A2164	Video IF IC for black/white and color TV sets	401
▼	TDA 2441	Q67000-A2174	Video IF IC for black/white and color TV sets	401
▼	TDA 2842	Q67000-A2385	Quasi-parallel sound IC	406
▼	TDA 4001	Q67000-A1779	AM receiver IC with demodulator	411
	TDA 4050 B	Q67000-A1373	Infrared preamplifier	418
	TDA 4100	Q67000-A1443	AM FM combination IC for radio sets	423
▼	TDA 4200-2	Q67000-A1469-E11	FM IF circuit for car radios	431
	TDA 4260	Q67000-A1300	AFC IC with programmable current deviation	436
	TDA 4283 T	Q67000-A2388	Quasi-parallel sound IC	439
	TDA 4290-2	Q67000-A1359	Tone control IC	445
▼	TDA 4290-2S	Q67000-A1359-E20	Tone control IC	445
▼	TDA 4292	Q67000-A2197	Stereo tone control with base width switch	453
▼	TDA 4600-2	Q67000-A1451-E19	Control IC for switched-mode power supplies	470
▼	TDA 4600-2D	Q67000-A2171	Control IC for switched-mode power supplies	470
	TDA 4610	Q67000-A1523	East west correction IC	480

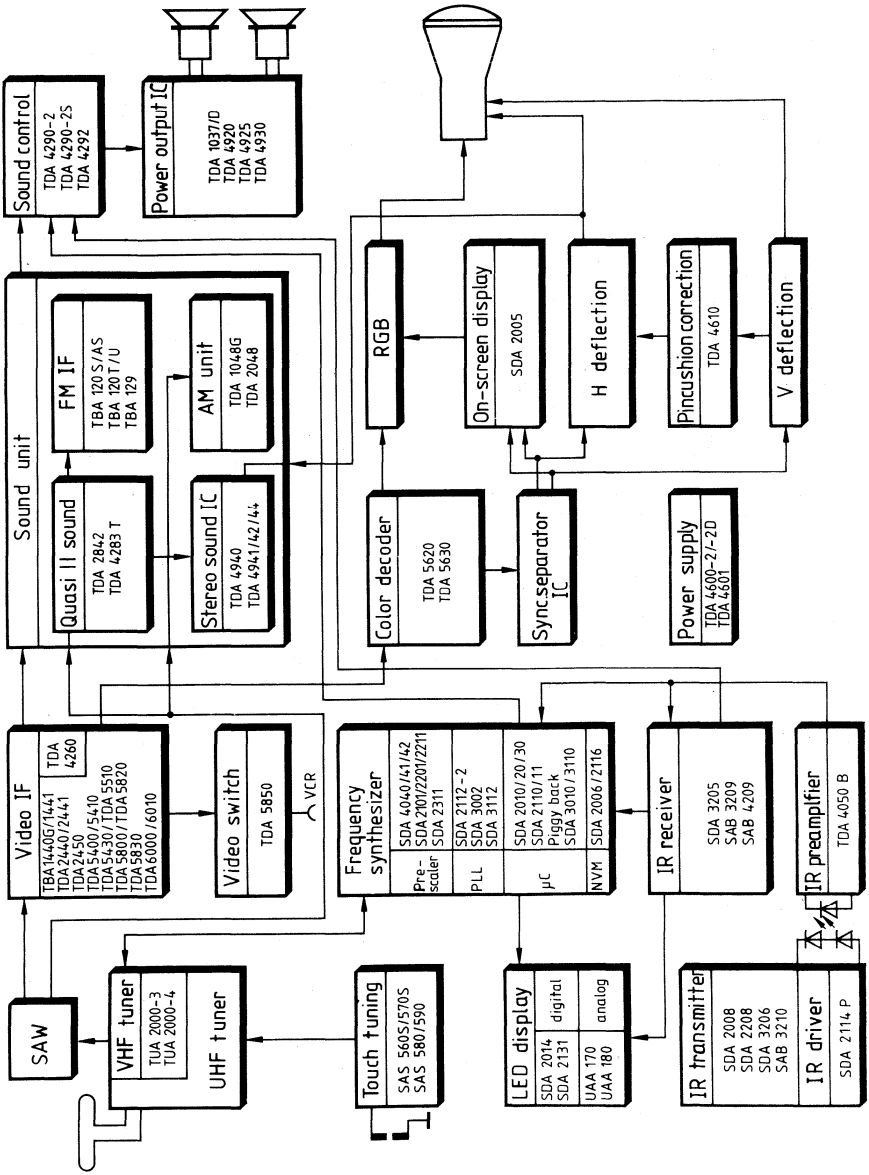
▼ New type
■ Not for new design

Summary of Types

	Type	Ordering code		Page
	TDA 4920	Q67000-A1846	Stereo/bridge AF amplifier	486
	TDA 4925	Q67000-A1893	Stereo/bridge AF amplifier	496
▼	TDA 4930	Q67000-A2156	Stereo/bridge AF amplifier	505
▼	TDA 4940	Q67000-A1872	FM IF amplifier with pilot tone decoding for TV stereo application	513
▼	TDA 4941	Q67000-A1952	TV stereo matrix with headset and VCR connection	520
▼	TDA 4942	Q67000-A1926	TV stereo matrix with tape recorder connection	532
▼	TDA 4944	Q67000-A2186	TV stereo matrix with VCR connection	539
▼	TDA 5400	Q67000-A2165	Video IF IC with AFC	543
▼	TDA 5410	Q67000-A2173	Video IF IC with AFC	543
▼	TDA 5430	Q67000-A2202	Video IF IC with 30 V AFC	548
	TDA 5500	Q67000-A1377	Video IF IC with VCR connection	553
▼	TDA 5510	Q67000-A2196	Video IF IC with VCR connection	559
▼	TDA 5620	Q67000-A2214	PAL color decoder	564
▼	TDA 5630	Q67000-A2215	SECAM color decoder	576
■	TDA 5800	Q67000-A1777	Video IF IC with AFC and VCR connection	586
	TDA 5820	Q67000-A1776	Video IF IC with AFC for CCIR and French standard	591
	TDA 5850	Q67000-A1775	VCR supplementary IC for French standard (Peri connector)	597
▼	TDA 6000	Q67000-A2203	Video IF IC with synchronous demodulator	600
▼	TDA 6010	Q67000-A2227	Video IF IC with synchronous demodulator	600
	TUA 2000	Q67000-A1764-C702	TV tuner IC	604
▼	TUA 2000-2	Q67000-A1764-C705	TV tuner IC	616
	UAA 170	Q67000-A940	LED driver for light spot displays	628
	UAA 180	Q67000-A1104	LED driver for light band displays	635

▼ New type
■ Not for new design

1.2 ICs in TV sets



Summary of Types

1.2.1 ICs in TV sets (in application-oriented order)

			Page
	Tuner		
	TUA 2000	TV tuner IC	604
▼	TUA 2000-2	TV tuner IC	616
	Prescaler		
	SDA 2101	Frequency divider 1:64 with preamplifier	180
▼	SDA 2201	Frequency divider 1:64 with preamplifier	230
▼	SDA 2311	1 GHz divider 1:64 with preamplifier	243
■	SDA 4040	UHF/VHF divider 1:256 with preamplifier	290
	SDA 4041	UHF/VHF divider 1:256 with preamplifier	294
▼	SDA 4042	Frequency divider 1:256 with preamplifier	299
	Video IF IC		
	TBA 1440G	Video IF IC for black/white and color TV sets	324
	TBA 1441	Video IF IC for black/white and color TV sets	324
▼	TDA 2440	Video IF IC for black/white and color TV sets	401
▼	TDA 2441	Video IF IC for black/white and color TV sets	401
	TDA 4260	AFC IC with programmable current deviation	436
▼	TDA 5400	Video IF IC with AFC	543
▼	TDA 5410	Video IF IC with AFC	543
▼	TDA 5430	Video IF with 30 V AFC	548
	TDA 5500	Video IF IC with VCR connection	553
▼	TDA 5510	Video IF IC with VCR connection	559
■	TDA 5800	Video IF IC with AFC and VCR connection	586
	TDA 5820	Video IF IC with AFC for CCIR and French standard	591
	TDA 5850	VCR supplementary IC for French standard (Peri connector)	597
▼	TDA 6000	Video IF IC with synchronous demodulator	600
▼	TDA 6010	Video IF IC with synchronous demodulator	600
	Quasi-parallel sound		
	TDA 4283 T	Quasi-parallel sound IC with FM IF with sym. input	439

▼ New type
■ Not for new design

Summary of Types

			Page
	TV stereo sound		
▼	TDA 4940	FM IF amplifier with pilot decoding for TV stereo application	513
▼	TDA 4941	TV stereo matrix with headset and VCR connection	520
▼	TDA 4942	TV stereo matrix with tape recorder connection	532
▼	TDA 4944	TV stereo matrix with VCR connection	539
	Sound unit IF amplifier		
	TBA 120 S	FM IF amplifier with demodulator	303
■	TBA 120 AS	FM IF amplifier with demodulator	303
	TBA 120 T	FM IF amplifier with demodulator	311
	TBA 120 U	FM IF amplifier with demodulator	311
▼	TBA 129	FM IF amplifier with demodulator	321
	TDA 1048 G	Controlled AM amplifier with demodulator and AF volume control	392
	TDA 2048	Controlled AM amplifier for French sound IF standard	396
	Signal processing in TV receivers		
▼	TDA 5620	PAL color decoder	564
▼	TDA 5630	SECAM color decoder	576
	Single chip microcomputer family		
	SDA 2010	Application-oriented single chip microcomputer	151
▼	SDA 2020	Application-oriented single chip microcomputer	166
▼	SDA 2030	Application-oriented single chip microcomputer	173
	SDA 2110	Application-oriented single chip microcomputer	184
▼	SDA 3010	Application-oriented single chip microcomputer	259
▼	SDA 3110	Application-oriented single chip microcomputer	267

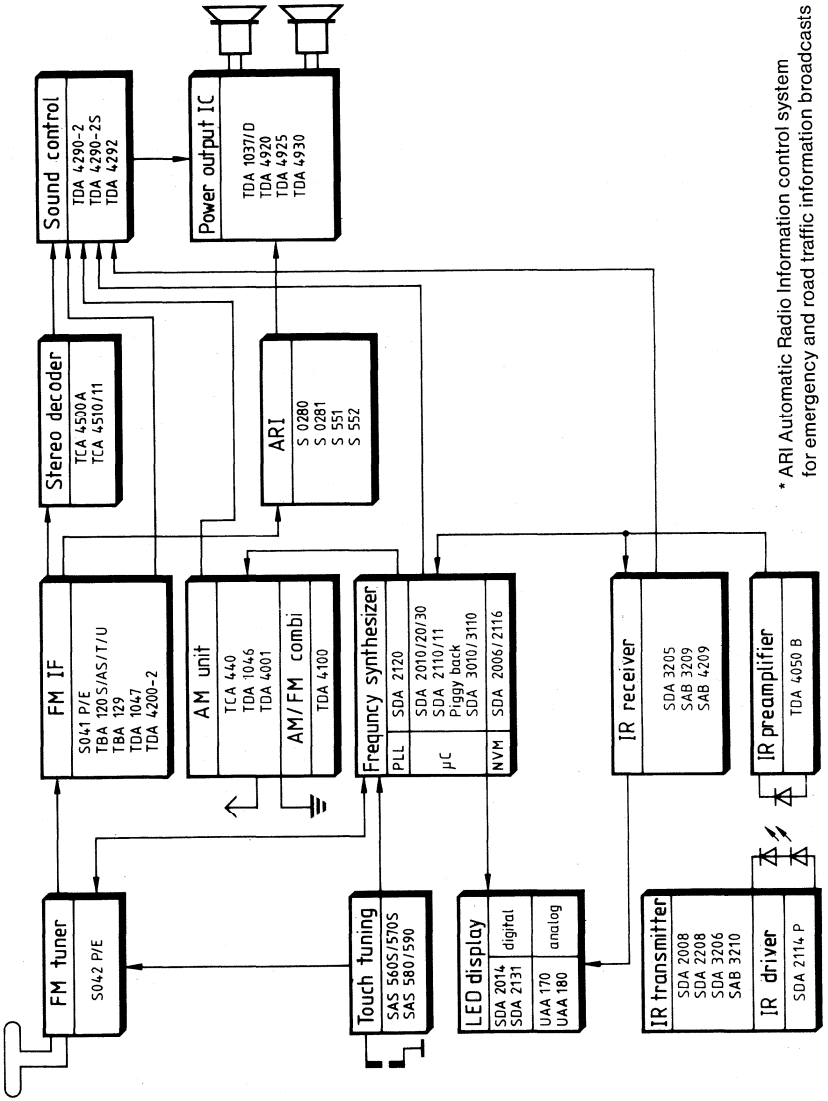
▼ New type
■ Not for new design

Summary of Types

			Page
	Siemens digital tuning systems SDA 210, SDA 220, SDA 230 for TV applications		643
	SDA 2101	Frequency divider 1:64 with preamplifier	180
▼	SDA 2201	Frequency divider 1:64 with preamplifier	230
▼	SDA 2311	Switchable divider 1:64 with preamplifier	243
▼	SDA 2112-2	PLL IC	191
▼	SDA 3002	TV phase-locked loop IC	249
	SDA 2010	Application-oriented single chip microcomputer	151
▼	SDA 2020	Application-oriented single chip microcomputer	166
▼	SDA 2030	Application-oriented single chip microcomputer	173
▼	SDA 2131	Static LED display driver with blanking capability	224
▼	SDA 2005	On-screen IC	114
	SDA 2006	Nonvolatile memory 512 bit EAROM	124
▼	SDA 2116	Nonvolatile memory 1 Kbit E^2PROM	206
	SDA 2008	IR remote control system – transmitter	134
	TDA 4050 B	IR preamplifier	418
	Siemens digital tuning system SIECON 21 M for CATV converters		646
	SDA 2101	Frequency divider 1:64 incl. preamplifier	180
▼	SDA 2112-2	PLL IC	191
	SDA 2110	Application-oriented single chip microcomputer	184
	SDA 2008	IR remote control system – transmitter	134
	TDA 4050 B	IR preamplifier	418
	Function units		
▼	TDA 4600-2	Control IC for switched-mode power supplies	470
▼	TDA 4600-2D	Control IC for switched-mode power supplies	470
	TDA 4610	East-west correction IC	480

▼ New type
■ Not for new design

1.3 ICs in radio sets



1.3.1 ICs in radio sets

Tuner

		Page
S 042 E	Mixer	41
S 042 P	Mixer	41

IF unit

S 041 E	FM IF amplifier incl. demodulator	35
S 041 P	FM IF amplifier incl. demodulator	35
TCA 440	AM receiver circuit	330
TDA 1046	AM receiver IC incl. demodulator	376
TDA 1047	FM IF amplifier IC incl. demodulator for radio receivers	385
▼ TDA 4001	AM receiver IC with demodulator	411
TDA 4100	AM FM combination IC suited for radio sets	423
▼ TDA 4200-2	FM IF IC for car radios	431

Stereo decoder

TCA 4500 A	Stereo decoder	347
TCA 4510	Phase-locked loop stereo decoder for low-voltage operation	351
▼ TCA 4511	Phase-locked loop stereo decoder	359

Siemens radio tuning system (frequency synthesis)

SDA 2120	120 MHz PLL	211
SDA 2010	Application-oriented single chip microcomputer	151
SDA 2110	Application-oriented single chip microcomputer	184
▼ SDA 2131	Static LED display driver with blanking capability	224
SDA 2006	Nonvolatile memory 512 bit EAROM	124
▼ SDA 2116	Nonvolatile memory 1 Kbit E^2PROM	206

▼ New type
■ Not for new design

1.4 ICs for general purpose applications

Remote control systems **Page**

■ SAB 3209 Infrared remote control system – receiver (3 analog functions) 69
SAB 3210 Infrared remote control system – transmitter 80
SAB 4209 Infrared remote control system – receiver (4 analog functions) 90
SDA 2008 Infrared remote control system – transmitter 134
SDA 2114 P IR diode driver incl. power-on transistor for PMOS control 201
▼ SDA 2208 Remote control transmitter with IR diode driver 234

AF power amplifier

TDA 1037 AF power amplifier IC with thermal shutdown 367
TDA 1037 D AF power amplifier IC with thermal shutdown 367
TDA 4920 Stereo/bridge AF amplifier 486
TDA 4925 Stereo/bridge AF amplifier 496
▼ TDA 4930 Stereo/bridge AF amplifier 505

Mono and stereo tone control

TDA 4290-2 Tone control IC 445
▼ TDA 4290-2S Tone control IC 445
▼ TDA 4292 Stereo tone control with base width switch 453

Switches

SAS 560 S Switching amplifier for 4-channel touch tuning 102
SAS 570 S Switching amplifier for 4-channel touch tuning 102
SAS 580 Switching amplifier for 4-channel touch tuning 106
SAS 590 Switching amplifier for 4-channel touch tuning 106

LED arrey driving

UAA 170 LED driver for light spot displays 628
UAA 180 LED driver for light band displays 635

▼ New type
■ Not for new design

General Information

2.1 Type designation code for ICs

The IC type designations are based on the European code system of Pro Electron. The code system is explained in the Pro Electron brochure D 15, edition 1982.

which can be obtained from: Pro Electron
Boulevard de Waterloo 103, B-1000 Bruxelles

2.2 Mounting instructions

2.2.1 Plastic plug-in package with 4, 6, 8, 14, 16, 18, 22, 24, 28, 36, 40, 48 pins, and power plug-in package TO-220

Plastic plug-in packages are soldered to the PC board side which does not face the equipment case. The pins are bent downwards by an angle of 90°, and fit into holes spaced at an equal distance of 2.54 mm and having a diameter of 0.7 to 0.9 mm. The dimension x is shown in the corresponding package outline drawing.

The bottom of the package does not touch the PC board after insertion, because the pins have shoulders just below the package (see figure).

After inserting the package into the PC board, two or more pins should be bent by an angle of approximately 30° towards the PC board so that the package need not be held down during soldering. The maximum permissible soldering temperature for iron soldering is 265 °C (max. 10 s), and for dip soldering 240 °C (max. 4 s).

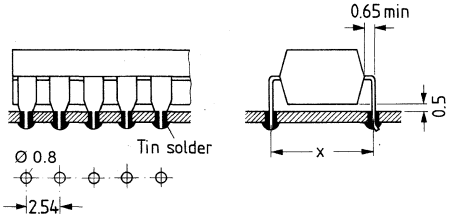


Fig. 1

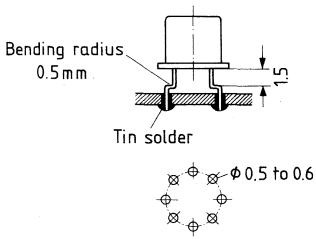


Fig. 2

Dimensions in mm

2.2.2 Package 5 H 8 DIN 41873 and similar packages

The package may be mounted in any position. The pins may be kinked at a minimum distance of 1.5 mm to the case according to the hole spacing (fig. 2). Pins that are too long should be clipped before soldering. Iron or dip soldering may be used.

Maximum soldering time for dip soldering at 250 °C bath temperature: $t_{max} = 5$ s
at 300 °C bath temperature: $t_{max} = 4$ s
for iron soldering at 250 °C iron temperature: $t_{max} = 15$ s
at 300 °C iron temperature: $t_{max} = 12$ s
at 350 °C iron temperature: $t_{max} = 8$ s
(does not apply to MOS circuits)

2.2.3 MOS ICs

If **MOS ICs** are used, care should be taken that no current flows between solder bath or soldering iron respectively, and PCB. It is, therefore, recommended to ground the pins to be soldered and the solder bath or the soldering iron.
The MOS circuits should be protected from static charges when they are prepared and inserted into the PCB. In no case may the MOS ICs be taken from or inserted into the circuit when the operating voltage is switched on.

2.3 Ultrasonic cleaning of integrated circuits

Freon and isopropyl alcohol (trade name: propanol) can be used as solvents. These solvents can also be used for the plastic packages as they do not corrode the plastic material.

An ultrasonic bath in double half wave operation is recommended due to the low degree of component stress.

The following ultrasonic limits are permitted:

Sound frequency	$f > 40$ kHz
Duration	$t < 2$ min
Sound pulse pressure	$p < 0.29$ bar
Sound power	$N < 0.5$ W/cm^2/liter

2.4 Processing guidelines for MOS ICs

2.4.1 General

MOS (**M**etal **O**xide **S**ilicon) technology components require careful handling, as the component can be destroyed by uncontrolled electrical charges, voltages of ungrounded equipment, overvoltage spikes, or similar influences. The following handling guidelines must be adhered to, even if the components have protective circuitry (e.g. protective diodes) at their inputs.
MOS components and other components with similar sensitivity that must be handled in accordance with this guideline, have been specially marked.

2.4.2 Scope

This guideline applies to the storage, shipping, testing, and processing of all types of MOS components, as well as fitted and soldered PC boards comprising such components.

2.4.3 General handling

2.4.3.1 MOS components must remain in their containers until being processed.

2.4.3.2 MOS components may only be handled at work stations specially equipped for this purpose.

2.4.3.3 Personnel working at these work stations must wear the specified clothing and the bracelet required for grounding.

2.4.3.4 MOS components should only be picked up at their package, wirhout touching the pins.

2.4.3.5 If short-circuit rings or straps are attached to the components, they should remain, if possible, until the component reaches the test area.

2.4.3.6 All MOS component transportation units and equipped PC boards must first be brought to the same potential by setting them down at the work station or by being touched by the personnel, before the individual MOS component may be touched.

2.4.3.7 Machines, tools, or equipment, with which MOS components are processed or transported are to be conductive.

The metal parts of machines, tools, and equipment, which can be touched from the outside, are included in a potential compensation system that is connected to the MOS work station and ground, insofar as this is not contrary to VDE regulations (e.g. for tools with low voltage transformers).

2.4.3.8 Sensitive PC boards and those equipped with MOS components, must be handled as described in paragraph 2.4.8.4.

2.4.4 Delivery, forwarding

MOS components and PC boards equipped with MOS components must be shipped in clearly marked and suitable packing material, e.g. in conductive foam material, in metal or plastic rails provided with an anti-static coating or with short-circuit connectors. Plastic rails may not be used more often than 10 times.

Additionally, the delivered packing or the transportation equipment used in production, must bear a standardized label.

2.4.5 Storage

MOS components may only be stored in defined, marked areas. During storage, the components should remain in the packing material in which they were delivered. In case of repacking or removal from stock please observe paragraph 2.4.3

If smaller quantities have to be forwarded, individual components must be repacked into conductive transportation containers suited for MOS.

2.4.6 Transportation

MOS components may only be transported in containers or transportation carts reserved for MOS.

The carts and containers for the individual components must be made of conductive material (steel rails, or conductive plastic), or be provided with conductive coating (conductive silver paint).

Transportation carts must be equipped with a contact strip trailing on the ground. These carts can be recognized due to an orange marking (RAL 2004).

Transport containers, painted orange (RAL 2004), labelled MOS, may only be used as containers for MOS components and for PC boards fitted with MOS components. These containers must be lined with conductive sponge rubber. Supplier, e.g. Canespa KG, Gutenbergstr. 13, D-3005 Hemmingen 1. Designation of the sponge rubber: electrically conductive special foam material "Packing 2000".

2.4.7 Incoming inspection

Incoming inspection of MOS components should be limited to a minimum. If necessary, tests should be carried out in accordance with sections 2.4.3. and 2.4.9.

2.4.8 **Material and mounting**

2.4.8.1 Drive belts of machines used for MOS processing, which come into contact with the MOS components (like bending and cutting machines, conveyor belts) have to be treated with antistatic spray (e.g. Antistatic Spray 100 from Kontaktchemie). It would be better, however, to eliminate such contact.

2.4.8.2 If MOS components must be soldered in or out by hand, only suitable soldering irons are to be used, see paragraph 2.4.3.7, e.g. ADCOLA L 101 of the Polytronik GmbH, Quagliostr. 6, D-8000 München 90, or soldering irons with protective insulation of the ERSA and ZEVATRON companies.

Do not use soldering irons with thyristor regulation – voltage spikes!

Desoldering equipment which frees the holes by suction, e.g. ERSA Soldapullt, must be equipped with metal tips.

2.4.8.3 Soldered PC boards equipped with MOS components, which are endangered during transportation, have to be named by the technical order; inclusion in the factory specifications is required.

They must be transported in appropriate and marked transportation equipment, see paragraph 2.4.6. If there is no such note in the factory specifications, no precautions are to be taken.

2.4.8.4 All MOS components must be processed in accordance with paragraph 2.4.3. Short-circuit rings or short-circuit straps must not be removed during the assembly on the PC board if they can easily be removed in the test area.

Conductors and MOS components on soldered PC boards should not be touched.

2.4.8.5 The Statometer H 1407 from Herfurth GmbH, Postfach 13249, D-2000 Hamburg 50, is suitable for non-contact measurement of electrostatic charges.

2.4.9 **Electrical test**

2.4.9.1 The components must be processed in accordance with paragraphs 2.4.3 and 2.4.8. Before the fitted and soldered PC boards are tested, any attached short-circuit ring is to be removed.

2.4.9.2 Test sockets are not permitted to carry any voltage during insertion or removal of individual components or fitted PC boards, unless otherwise stated in the factory specifications. It must be assured that the test devices do not generate voltage spikes when they are turned on and off during operation, or in case of a failure of the line fuse, or in case of activation of other fuses.

2.4.9.3 Signal voltages may only be applied to MOS circuit inputs at the time when the supply voltage is turned on, or afterwards. They must be removed before or at the same time as the supply voltage is turned off.

2.4.9.4 The information in the appropriate data books must be observed.

2.4.10 **Packaging**

Recommended packaging: wrapping the fitted PC boards in conductive material, e.g. aluminum foil, and packing them into suitable cardboard boxes or packaging containers lined on both sides with conductive foam material. Any attached short-circuit elements are to be removed.

2.4.11 **Obligation**

The users may complement or alter the before-mentioned guideline on their own responsibility at any time.

In-house specifications must be observed.

2.5 Data classification

Maximum ratings

Maximum ratings are absolute limits. The integrated circuit may be destroyed if only a single value is exceeded.

Electrical characteristics

The electrical characteristics include the guaranteed tolerances of the values, which the IC stays within for the specified operating range.

The typical characteristics are mean values which are expected from production. Unless otherwise specified, the typical characteristics apply to $T_{amb} = 25\,°C$ and the specified supply voltage.

Operating data

In the operating range, the functions shown in the circuit description will be fulfilled.

2.6 Quality specifications

The delivery quality of integrated circuits is specified as follows:

2.6.1 Maximum ratings and tolerance limits of the characteristics

2.6.2 Sampling inspection, AQL values (acceptable quality level)

Inspection by attributes[1)] is based on the identical sampling inspection plans DIN 40080, (or) ABC Standard 105, inspection level II, normal inspection.

A delivery lot for which the defect percentage for a certain characteristic is equal or less than the specified AQL value, will most probably (more than 90%) be accepted in the appropriate sampling inspection.

The average defect percentage of delivered products lies, in general, clearly below the AQL value. Only the number of defective units is evaluated in the sampling inspection.

2.6.3 Defects

A component is considered defective if it does not comply with the characteristics specified in the data sheet.

The defects are classified as inoperatives, electrical defectives, and mechanical defectives. Unless otherwise agreed upon, the AQL values in section 5 apply to the various defect types.

Definition of defects

Inoperatives:
- opens and shorts
- missing or incorrect marking
- broken case or leads
- incorrect pin identification marks
- intermixing with other device types
- alternating orientation of components in tubes, rails, or tape

Electrical defectives:
- exceeding electrical maximum ratings

Mechanical defectives:
- defects on the package surface
- type marking hard to identify
- bent pins
- wrong dimensions

1) Inspection for a characteristic for which only two mutually exclusive properties are specified (good/bad).

2.6.5 **AQL table**

AQL values	MSI/SSI	LSI/VLSI
Inoperatives	0.1	0.25
Sum of electrical defectives	0.4	0.40
Sum of mechanical defectives	0.4	0.40

For switching times and noise figures, the AQL is 1.5.
SSI/MSI (< 250 Gate/IC): bipolar ICs with some exceptions
LSI/VLSI (≧ 250 Gate/IC): all MOS ICs.

2.6.6 **Incoming inspection**

The tests carried out by the manufacturer are intended to render expensive incoming inspection by the user unnecessary. If the user, however, wants to carry out such inspections, we recommend the use of a sampling inspection plan as decribed in section 2.6.7. The test method used must be agreed upon between customer and supplier.

The following information is required to adjust a possible claim: test circuit, sample size, number of defective items found, sample of evidence, packing list.

2.6.7 Sampling inspection plan for normal inspection

in accordance with DIN 40080 or ABC-Std 105 D, inspection level II

Lot size	Sample size	AQL-value										
		0,065	0,10	0,15	0,25	0,40	0,65	1,0	1,5	2,5	4,0	6,5
		A R	A R	A R	A R	A R	A R	A R	A R	A R	A R	A R
2 to 8	2											0 1
9 to 15	3										0 1	
16 to 25	5									0 1		
26 to 50	8								0 1			1 2
51 to 90	13							0 1			1 2	2 3
91 to 150	20						0 1			1 2	2 3	3 4
151 to 280	32					0 1			1 2	2 3	3 4	5 6
281 to 500	50				0 1			1 2	2 3	3 4	5 6	7 8
501 to 1200	80			0 1			1 2	2 3	3 4	5 6	7 8	10 11
1201 to 3200	125		0 1			1 2	2 3	3 4	5 6	7 8	10 11	14 15
3201 to 10000	200	0 1			1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22
10001 to 35000	315			1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	
35001–150000	500		1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22		
150001–500000	800	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22			
500001 and more	1250	2 3	3 4	5 6	7 8	10 11	14 15	21 22				

A = acceptance number, i.e. the maximum number of defective sample units up to which the lot is accepted.

R = rejection number, i.e. the minimum number od defective sample units which a sample must contain if the lot is to be rejected.

Additional requirement

As the combination »Acceptance 0 and Rejection 1« has a low degree of significance, the next highest size should be sampled

2.7 Summary of terms and symbols in alphabetical order

A, B	Indices for limit value
AC	Alternating current
AF	Audio frequency
AM	Amplitude modulation
B	Bandwidth
C	Capacitance
C_i, C_I	Input capacitance
C_{CLK}, $C_Ø$	Clock capacitor
CLK	Clock
DC	Direct current
D	Differential
f	Frequency
Δf	Frequency deviation
FM	Frequency modulation
f_i, f_I	Input frequency
f_q, f_Q	Output frequency
G	Gain
G	giga (10^9)
GND	Ground
Hy	Hysteresis
Hz	Cycles per second (Hertz)
i, I	Input
I, *i*	Current
I_S	Current consumption
IF	Intermediate frequency
k	kilo (10^3)
K	Kelvin
L	Inductance
m	Milli (10^{-3})
M	Mega (10^6)
m	Modulation factor
MW	Medium wave
N, n	Noise
o	offset
OSC	Oscillator
P, P_V	Power dissipation
P_{tot}	Max. perm. power dissipation
pp	Peak-to-peak
q, Q	Output
Q, Q_B	Q-factor
R	Resistance
$R_{th\ JC}$	Thermal resistance (junction-case)
$R_{th\ SC}$	Thermal resistance (system-case)
$R_{th\ SA}$	Thermal resistance (system-air)
RF	Radio frequency

$\frac{S+N}{N}$	Signal-to-noise ratio
T	Cycle time
T	Temperature
TC	Temperature coefficient
t	Time
T_{amb}	Ambient temperature in operation
T_{stg}	Storage temperature
T_j	Junction temperature
t_H	Hold time
t_I	Input pulse duration
t_n	Instant prior to clock pulse
t_{n+1}	Instant after clock pulse
t_P	Average pulse transit time
t_{pd}	Pulse delay time
$t_{P\,HL}$	HL pulse transit time
$t_{P\,LH}$	LH pulse transit time
t_{pI}	Input pulse duration
$t_{p\,Q}$	Output pulse duration
$t_{p\,R}$	Reset pulse duration
$t_{p\,S}$	Set pulse duration
$t_{p\,CLK}$	Clock pulse duration
$t_{p\,Z}$	Count pulse duration
t_s	Set-up time
t_T	Signal transition time
t_t	Dead time
t_Q	Output pulse duration
$t_{T\,HL}$	HL transition time
$t_{T\,LH}$	LH transition time
THD	Total harmonic distortion
V	Volt
V, v	Voltage, general
V_{Hy}	Hysteresis voltage
V_i, V_I	Input voltage
V_q, V_Q	Output voltage
V_R	Reverse voltage
V_S	Supply voltage
W	Watt
Z	Impedance
Z	Zener

Technical Data

Type	Ordering code	Package outline
S 041 E	Q67000-A694	5 J10 DIN 41873/TO-100
S 041 P	Q67000-A529	DIP 14

S 041 E and S 041 P are symmetrical, six-stage amplifiers with symmetrical coincidence demodulator for amplifying, limiting, and demodulating frequency-modulated signals. The ICs are particularly suited for sets where low current consumption is of importance, or where major supply voltage fluctuations occur.

The pin configuration corresponds to the well-known TBA 120. Pin 5 of S 041 P, however, is not connected internally. These types are especially suited for applications in narrow-band FM systems (455 kHz) and in conventional or standard FM IF systems (10.7 MHz).

Features

- Good limiting properties
- Wide voltage range
- Low current consumption
- Few external components

Maximum ratings

Supply voltage	V_S	15	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air) S 041 E	$R_{th\ SA}$	190	K/W
S 041 P	$R_{th\ SA}$	90	K/W

Operating range

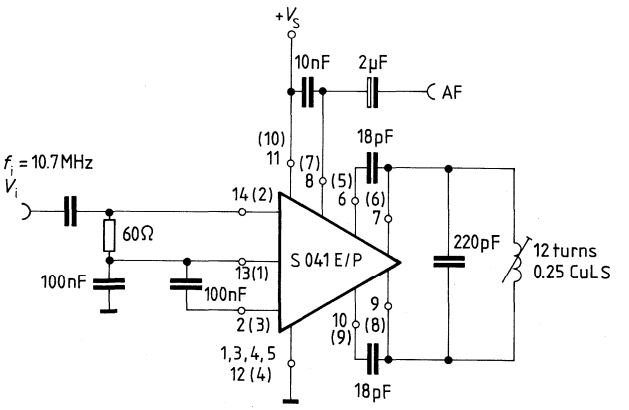
Supply voltage range	V_S	4 to 15	V
Frequency range	f_i	0 to 35	MHz
Ambient temperature range	T_{amb}	−25 to 85	°C

Characteristics ($V_S = 12$ V, Q approx. 35, $f_{mod} = 1$ kHz, $T_{amb} = 25°C$)

		min	typ	max	
Current consumption	I_S	4.0	5.4	6.8	mA
AF output voltage ($f_i = 10.7$ MHz, $\Delta f = \pm 50$ kHz, $V_i = 10$ mV)	$V_{q\,rms}$	100	170		mV
Total harmonic distortion ($f_i = 10.7$ MHz, $\Delta f = \pm 50$ kHz, $V_i = 10$ mV)	THD		0.55	1.0	%
Deviation of AF output voltage ($V_S = 15$ V → 4 V, $f_i = 10.7$ MHz, $\Delta f = \pm 50$ kHz)	ΔV_q		1.5		dB
Input voltage for limiting ($f_i = 10.7$ MHz, $\Delta f = \pm 50$ kHz)	$V_{i\,lim}$		30	60	µV
IF voltage gain ($f_i = 10.7$ MHz)	G_v		68		dB
IF output voltage for limiting (each output)	$V_{q\,pp}$		130		mV
Input impedance $f_i = 10.7$ MHz	Z_i		20/2		kΩ/pF
$f_i = 455$ kHz	Z_i		50/4		kΩ/pF
Output resistance (pin 8)	R_q	3.5	5	8.5	kΩ
Voltage drop at AF ballast resistance	V_{11-8}		1.5		V
AM suppression ($V_i = 10$ mV, $\Delta f = \pm 50$ kHz, $m = 30\%$)	a_{AM}		60		dB

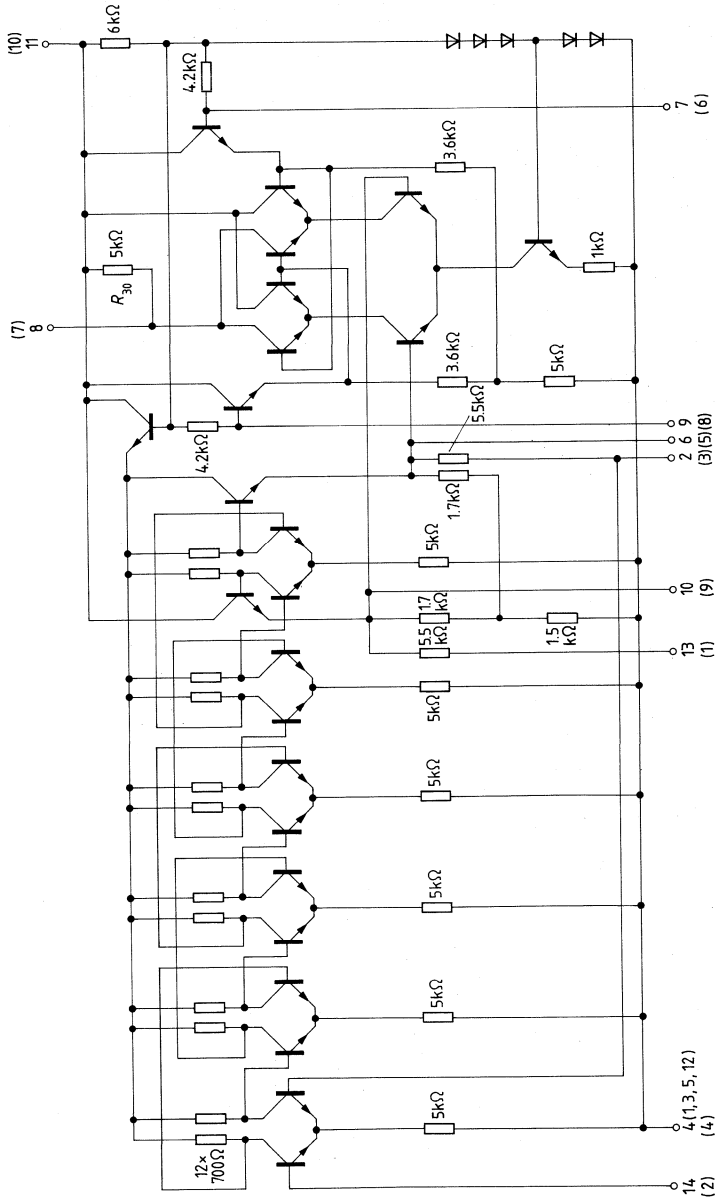
All connections mentioned in the index refer to S 041 P (e.g. V_{11})

Test circuit



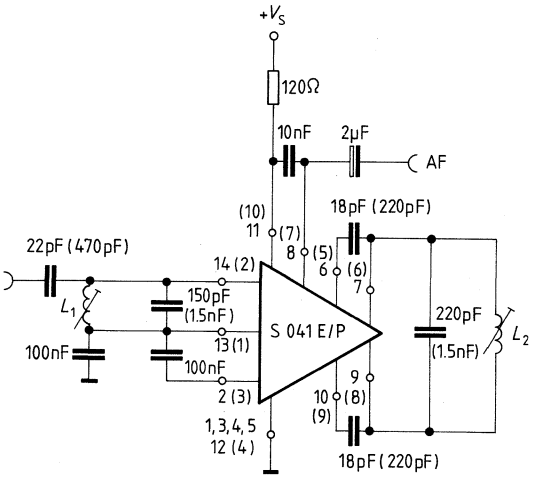
Connections in parentheses apply to S 041 E

Circuit diagram



Connections in parentheses apply to S 041 E

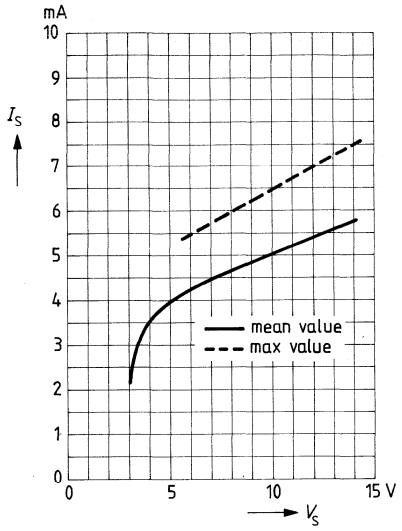
Application circuit for 10.7 MHz (FM IF)
and 455 kHz (narrow-band FM)



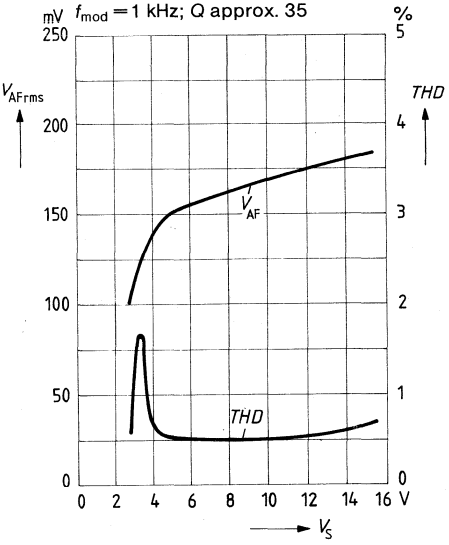
Data in parentheses for 455 kHz (narrow-band FM)
Connections in parentheses apply to S 041 E

Coils	10.7 MHz	455 kHz
L_1	15 turns/0.15 CuLS	71.5 turns/12 x 0,04 CuLS
L_2	12 turns/0.25 CuLS	71.5 turns/12 x 0.04 CuLS
Coil set	D 41-2165	D 41-2393 of Messrs. Vogt

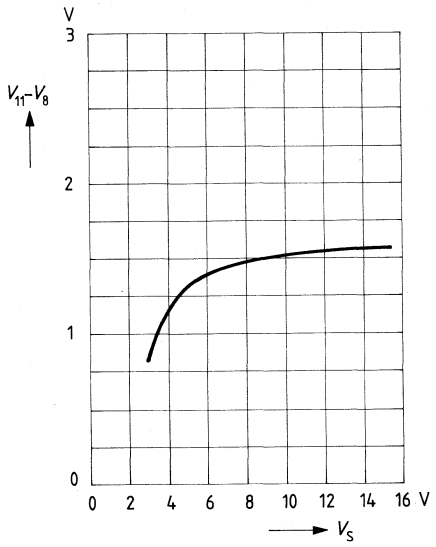
Current consumption versus supply voltage



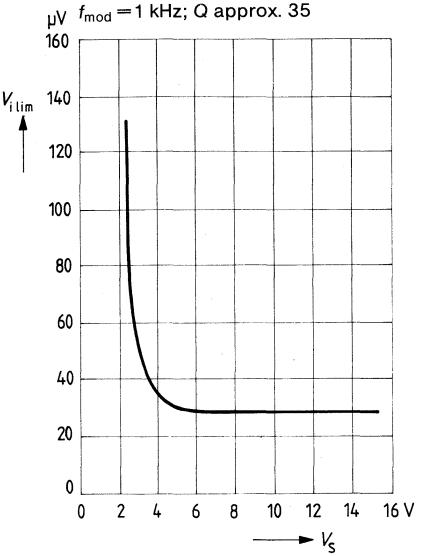
AF output voltage and total harmonic distortion versus supply voltage
$f_i = 10.7$ MHz; $\Delta f = \pm 50$ kHz
$f_{mod} = 1$ kHz; Q approx. 35



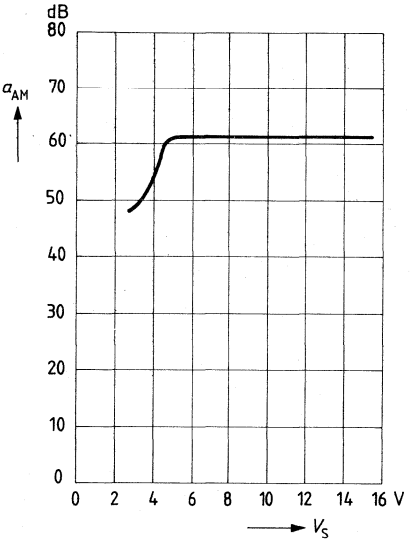
DC output voltage difference versus supply voltage
(without signal)



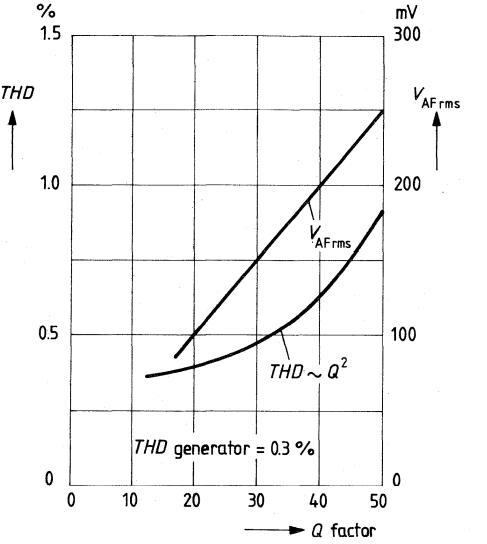
Input voltage for limiting versus supply voltage
$f_i = 10.7$ MHz; $\Delta f = \pm 50$ kHz
$f_{mod} = 1$ kHz; Q approx. 35



AM suppression versus supply voltage
$f_i = 10.7$ MHz; $\Delta f = \pm 50$ kHz;
$V_i = 10$ mV, $f_{mod} = 1$ kHz, $m = 30\%$



AF output voltage and total harmonic distortion versus Q-factor
$V_S = 12$ V; $f_i = 10.7$ MHz,
$\Delta f = \pm 50$ kHz, $f_{mod} = 1$ kHz



Bipolar circuit

Type	Ordering code	Package outline
S 042 E	Q67000-A627	5 J 10 DIN 41873/sim. to TO 100
S 042 P	Q67000-A335	DIP 14

Symmetrical mixers for frequencies up to 200 MHz. They can be driven by an external source or by the built-in oscillator. The input signals are suppressed at the outputs. In addition to the usual mixer applications in receivers, converters, and demodulators for AM and FM, the S 042 E and S 042 P can also be used as electronic polarity switches, multipliers etc.

Features

- Versatile application
- Wide range of supply voltage
- Few external components
- High conversion transconductance
- Low noise figure

Maximum ratings

Supply voltage	V_S	15	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air) S 042 E:	$R_{th\ SA}$	190	K/W
S 042 P:	$R_{th\ SA}$	90	K/W

Operating range

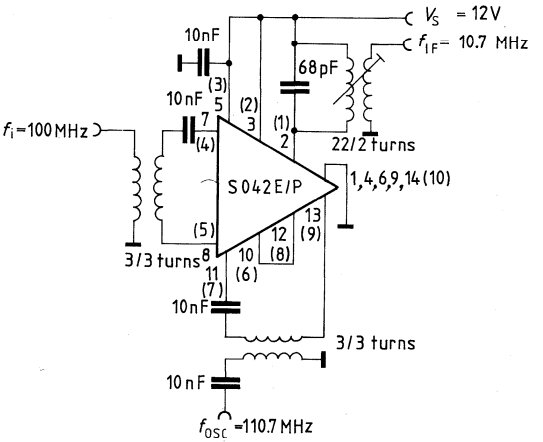
Supply voltage range	V_S	4 to 15	V
Ambient temperature range	T_{amb}	−15 to 70	°C

Characteristics ($V_S = 12$ V, $T_{amb} = 25$ °C)

		min	typ	max	
Current consumption	$I_S = I_2 + I_3 + I_5$	1.4	2.15	2.9	mA
Output current	$I_2 = I_3$	0.36	0.52	0.68	mA
Output current difference	$I_3 - I_2$	−60		60	mA
Supply current	I_5	0.7	1.1	1.6	mA
Power gain ($f_i = 100$ MHz, $f_{OSC} = 110.7$ MHz)	G_p	14	16.5		dB
Breakdown voltage ($I_{2,3} = 10$ mA; $V_{7,8} = 0$ V)	V_2, V_3	25			V
Output capacitance	$C_{2\text{-M}}$, $C_{3\text{-M}}$		6		pF
Conversion transconductance ($f = 455$ kHz)	$S = \frac{I_2}{V_7 - V_8} = \frac{I_3}{V_7 - V_8}$		5		mS
Noise figure	NF		7		dB

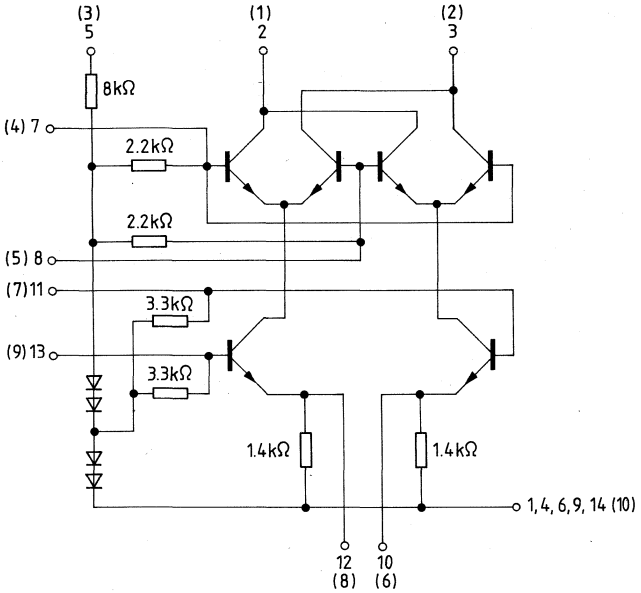
All connections mentioned in the index refer to S 042 P (e.g. I_2)

Test circuit



Connections in parentheses apply to S 042E

Circuit diagram

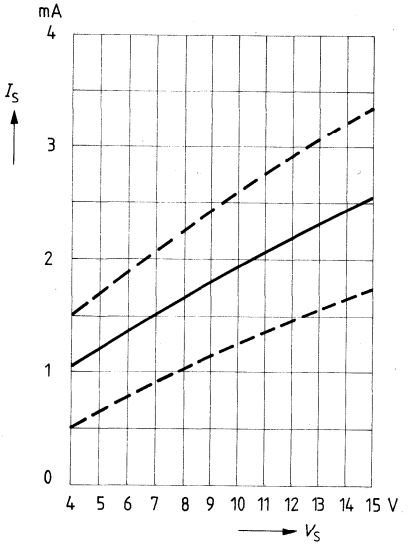


Connections in parentheses apply to S 042 E

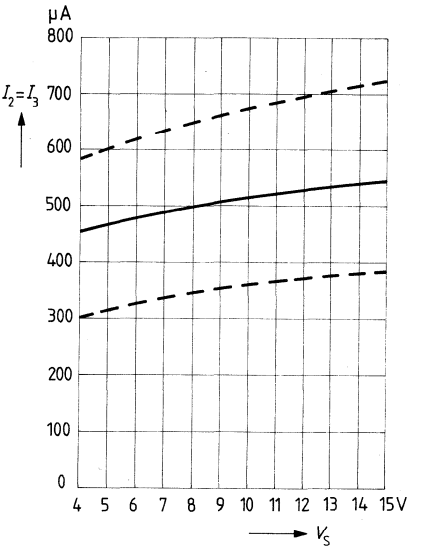
A galvanic connection between pins 7 and 8 and pins 11 and 13 through coupling windings is recommended.

Between pins 10 and 14 (ground) and between pins 12 and 14, one resistance each of at least 220 Ω may be connected to increase the currents and thus the conversion transconductance. Pins 10 and 12 may be connected through any impedance. In case of a direct connection between pins 10 and 12, the resistance from this pin to 14 may be at least 100 Ω. Depending on the layout, a capacitor (10 to 50 pF) may be required between pins 7 and 8 to prevent oscillations in the VHF band.

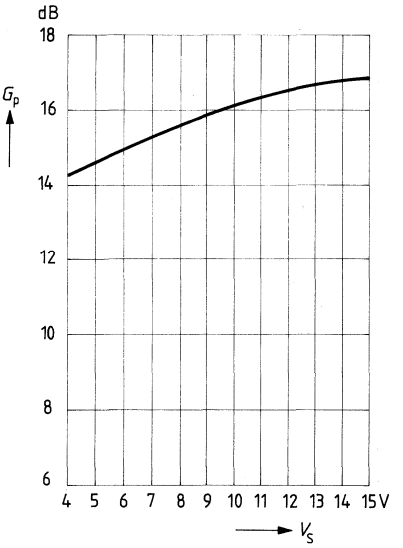
Total current consumption versus supply voltage



Output current versus supply voltage

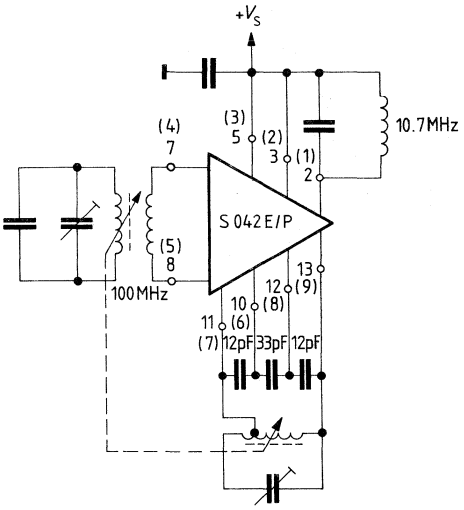


Power gain versus supply voltage



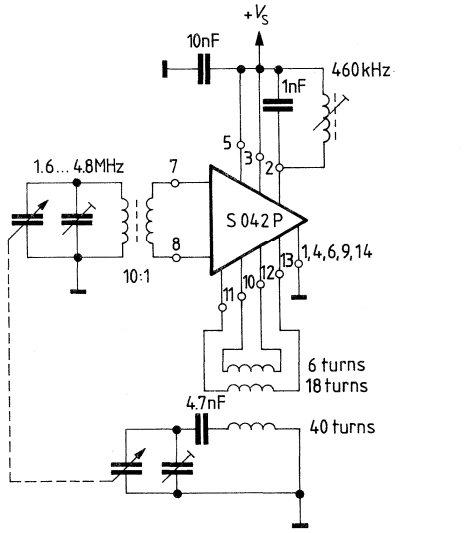
Application circuits

VHF mixer with inductive tuning

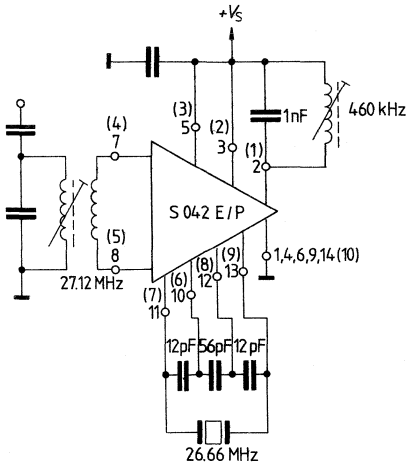


Connections in parentheses apply to S 042 E

Mixer for short-wave application
in self-oscillating operation



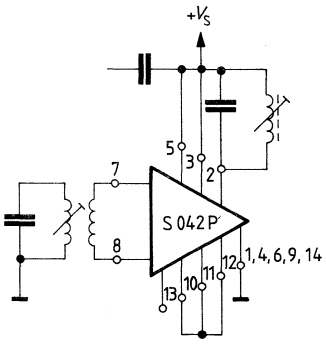
Mixer for remote control receivers
without oscillator



Connections in parentheses apply to S 042 E

For overtone crystals an adequate inductance is recommended between pins 10 and 12 to avoid oscillations to the fundamental tone.

Differential amplifier with internal neutralization, also suited for use as limiter for frequencies up to 50 MHz or at higher currents up to 100 MHz



Bipolar circuit

Type	Ordering code	Package outline
S 0280	Q 67000-A1264	DIP 16

The S 0280 IC includes a PLL circuit, an AM demodulator and an electronic AF switch for switching an MPX signal.

The IC delivers the station identification frequency (57 kHz) as square-wave voltage (pin 6) for subsequent operation in the S 551 and S 552 ICs and the station decoding trigger for the S 551. At pin 7 of the S 0280 the message identification frequency (125 Hz) and the area identification frequency (23.75 to 53.98 Hz) are available. After the message has been decoded in the S 551, the message AF is switched in the S 0280 to pin 5 by means of a logic control signal.

Features

- Minimal adjustment
- Minimal DC voltage jump at the AF volume switch

Maximum ratings

Supply voltage	V_{16}	18	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\ SA}$	90	K/W

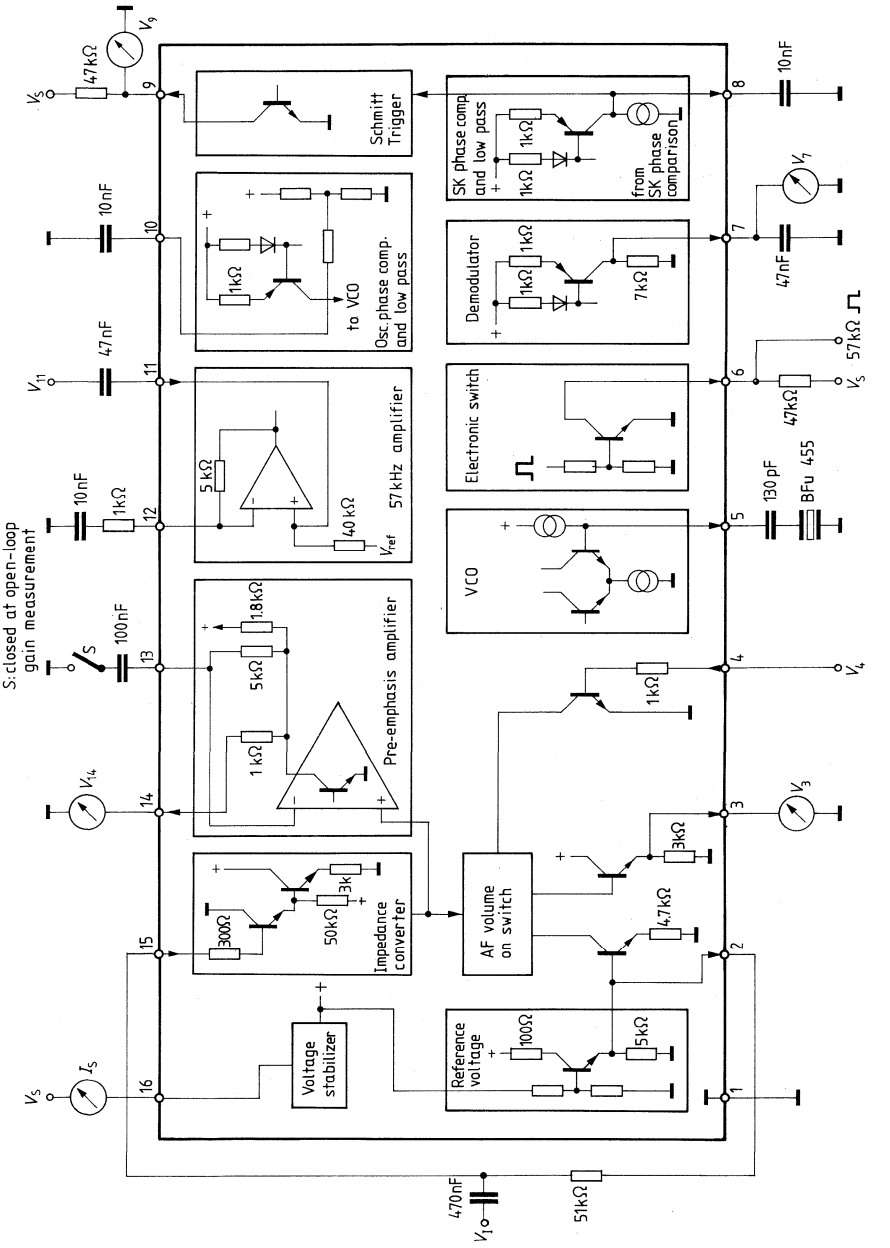
Operating range

Supply voltage range	V_{16}	10 to 16	V
Ambient temperature range	T_{amb}	−20 to 85	°C

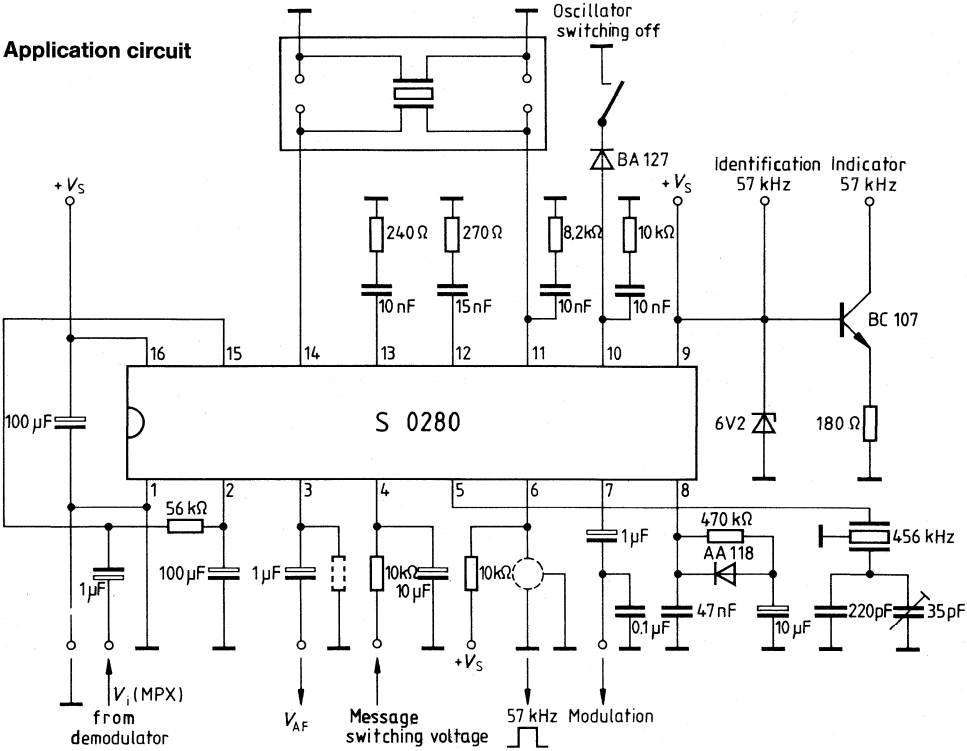
Characteristics (V_{16} = 14 V, T_{amb} = 25 °C, referred to test circuit)

		min	typ	max	
Current consumption	I_{16}		25	35	mA
Input voltage (peak-to-peak) (THD = 10%)	V_{i15}			2.5	V
Input resistance	R_{i15}	300			kΩ
Pre-emphasis amplifier					
Output resistance	R_{q14}	1.6	2	2.4	kΩ
Voltage gain (open loop)	G_{vo}	30			dB
Internal GK resistance	R_{13}		5		kΩ
57 kHz amplifier					
Voltage gain (open loop)	G_{vo}		35		dB
Internal GK resistance	R_{12}		5		kΩ
Input resistance	R_{i11}	20			kΩ
SK information					
SK switching threshold (switching at pin 9) V_{11}, f = 57 kHz	$V_{SK\,rms}$	6		18	mV
BK-OK output voltage $V_{11\,rms}$ = 50 mV, 57 kHz + 125 Hz, m = 30%	$V_{7\,rms}$	24			mV
Load voltage SK = H	V_8	3			V
($R_{9/10}$ = 10 kΩ) SK = L	V_8			2	V
Hysteresis voltage	ΔV_8		1		V
Output current	I_{q9}			5	mA
Output current/frequency divider	I_{q6}			5	mA
Volume switch					
Bandwidth	B	60			kHz
Transmission loss	a	−1	0	+1	dB
Rejection loss	a_{rej}	50	80		dB
Output resistance	R_{q3}		380	500	Ω
Switching threshold	V_4		0.65		V
Noise voltage at pin 3 at decrease of 3 dB (f = 100 Hz to 10 kHz, short-circuited input)	V_3		15		µV

Block diagram and test circuit



Application circuit



Pin configuration

Pin No.	Function
1	Ground
2	Reference voltage
3	MPX output signal
4	Control voltage input for MPX signal
5	Oscillator wiring (*LC*, *RC*)
6	57 kHz output
7	57 kHz demodulator output
8	SK phase comparator, integration C
9	SK output
10	PLL phase comparator
11	57 kHz amplifier input +
12	57 kHz amplifier input −
13	Pre-emphasis amplifier input −
14	Pre-emphasis amplifier output
15	Impedance converter input
16	Supply voltage +V_S

Bipolar circuit

Type	Ordering code	Package outline
S 0281	Q 67000-A1265	DIP 18

The S 0281 IC is used for preparing message and area decoding of VRF transmitters.

The S 0281 contains two double operational amplifiers which are used as filter and limiter amplifier. Moreover, 3 AF switches are included for switching the message signal.

Features

- High cross talk rejection
- High rejection loss
- Min. dc voltage change when switching the signals

Maximum ratings

Supply voltage	V_{17}	18	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\ SA}$	90	K/W

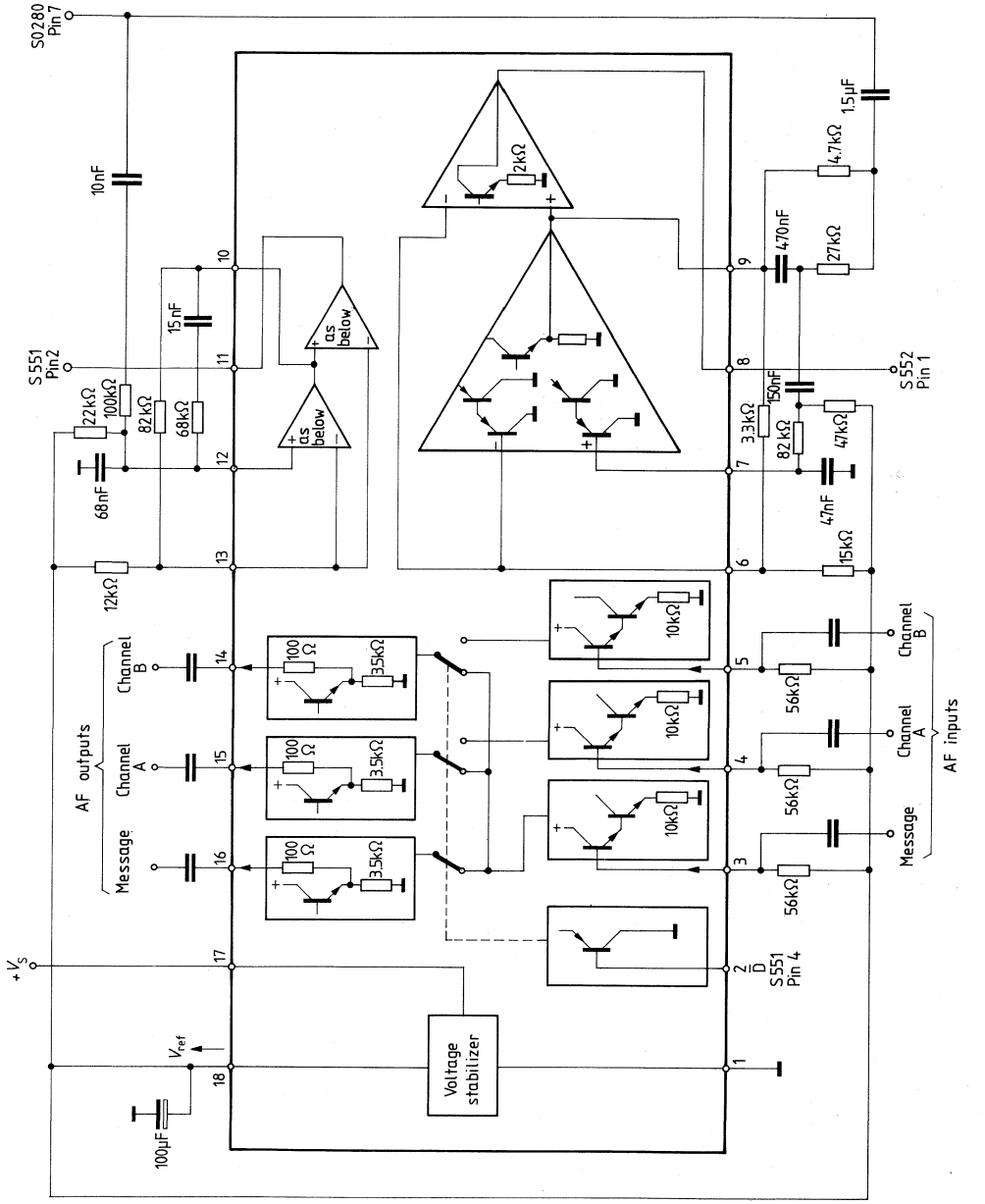
Operating range

Supply voltage range	V_{17}	10 to 16	V
Ambient temperature range	T_{amb}	−20 to 85	°C

Characteristics (V_{17} = 14 V, T_{amb} = 25 °C)

		min	typ	max	
Current consumption	I_{17}		15	30	mA
Band filter amplifier					
Voltage gain (open loop) (f = 150 Hz)	G_{vo}	50	64		dB
Dynam. output resistance at open loop voltage gain	$R_{9/10}$	1.2			kΩ
Limiter amplifier					
Voltage gain (open loop)	G_{vo}	50			dB
Input voltage (peak-to-peak)	$V_{6/9}$; $V_{10/13}$			4	V
H output leakage current	$I_{8/11}$			50	µA
DK switch, control input D					
L input voltage	V_{i2}			0.8	V
L input current (V_2 = 0.8 V)	$-I_{i2}$			1.0	µA
H input voltage	V_{i2}	2.8			V
H input current (V_2 = 2.8 V)	$-I_{i2}$			0.5	µA
Switches					
Forward gain	G	2	3	4	dB
Rejection loss	a_{rej}	50	60		dB
Cross talk rejection from channel to channel					
f = 1 kHz	a_{cr}	50			dB
f = 10 kHz	a_{cr}	40			dB
Large signal behavior of the inputs (peak-to-peak)					
THD = 1%	$V_{3/4/5}$		2	3	V
THD = 10%	$V_{3/4/5}$		2.5		V
Input resistance	R_{i3}; R_{i4}; R_{i5}	500			kΩ
Input current	I_{i3}, I_{i4}, I_{i5}			0.1	µA
Output resistance	R_{q14}; R_{q15}		0.3	2	kΩ
	R_{q16}		175		Ω
Interference voltage at the output f = 10 Hz to 10 kHz, 3 dB down	V_{14}; V_{15}; V_{16}		12	20	µV
Reference voltage	V_{18}	3.1	3.4	3.7	V

Block diagram



Message Decoder for FM Road Traffic Information Service

S 551

MOS circuit

Type	Ordering code	Package outline
S 551	Q 67100-Z109	DIP 18

The MOS circuit S 551 is built up in depletion-load-technology. It constitutes in connection with the two bipolar circuits S 0280 (Station Decoder) and S 0281 (Message Decoder) and the MOS circuit S 552 (Area Decoder) the main portion of a traffic broadcast decoder used for car radios.

The traffic broadcast decoder (VRF decoder) recognizes a VRF station and the traffic messages (VDS) transmitted by it. An additional unit, the area decoder, identifies the regional identity of a station. The VRF decoder also permits automatic search for a VRF station.

The S 551 is intended to recognize traffic broadcast messages. As a technical prerequisite, the same identification frequencies should be used by the various broadcasting stations.

VRF frequency: 57 kHz
VDS frequency: 125 Hz

Maximum ratings (all voltages referred to $V_{DD} = 0$ V)

		min	max	
Supply voltage	V_{SS}	−0.3	18	V
Input voltage	V_i	0	V_{SS} +0.3	V
Power dissipation	P_{tot}		360	mW
Power dissipation per output (one output at a time)	P_q		100	mW
Storage temperature	T_{stg}	−40	125	°C

Operating range

Supply voltage range	V_{SS}	9 to 16		V
Ambient temperature range	T_{amb}	−25 to 85		°C

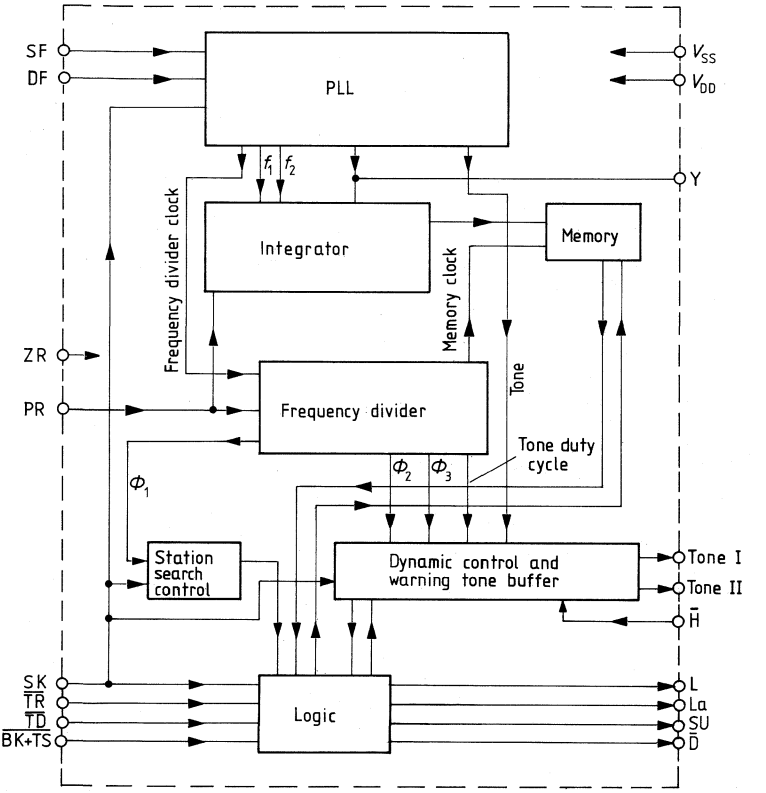
Characteristics (all voltages referred to $V_{DD} = 0$ V)

		min	typ	max	
Supply current	I_{SS}			15	mA
Inputs					
Transmission frequency SF (57 kHz) (Internal pull-high resistor)					
Message frequency DF (125 Hz)					
(internal pull-high resistor)					
H pulse width	t_{WH}				
(duty cycle approx 1:2)					
L pulse width	t_{WL}				
(duty cycle approx. 1:2)					
HL transition time	t_{THL}			3.5	µs
LH transition time	t_{TLH}			3.5	µs
Harmless H input current	I_{iH}			1	µA
L input source resistance (to V_{DD})	$R_{i\,QL}$			10	kΩ
L input source resistance (to $V_{DD}+1$ V)	$R_{i\,QL}$			6	kΩ
Key radio $\overline{TR}$ (see fig. 1) **Key message $\overline{TD}$** (see fig. 2) (internal pull-high resistor)					
Transmission identification SK					
(from DK analog circuit)					
(internal pull-high resistor)					
Harmless H input current	I_{iH}			1	µA
L input source resistance (to V_{DD})	$R_{i\,QL}$			5	kΩ
L input source resistance (to $V_{DD}+1$ V)	$R_{i\,QL}$			3	kΩ
Area identification $\overline{BK}+\overline{TS}$ **Warning tone suppression $\overline{H}$** (see fig. 3)					
H input voltage	V_{iH}	$V_{SS}-1.5$		V_{SS}	V
L input voltage	V_{iL}			2	V
Required input current	I_i			10	µA
Reset input ZR (see fig. 4)					
H input voltage (reset)	V_{iH}	$V_{SS}-1.3$		V_{SS}	V
L input voltage (release)	V_{iL}			2	V
H pulse width	t_{WH}	20			µs
Required input current	I_i			10	µA

Characteristics (all voltages referred to $V_{DD} = 0$ V)

		min	typ	max	
Outputs					
Station search SU					
Loud-circuit La					
H output voltage (at $\lvert I \rvert = 0.05$ mA)	V_{qH}	$V_{SS}-5$		V_{SS}	V
L output voltage (at $\lvert I \rvert = 1$ µA)	V_{qL}			0.35	V
Short-circuit current	$\lvert I_{SC\,max} \rvert$			10	mA
Lamp L					
H output voltage (at $\lvert I \rvert = 0.5$ mA)	V_{qH}	$V_{SS}-7$		V_{SS}	V
L output voltage (at $\lvert I \rvert = 1$ µA)	V_{qL}			0.35	V
Short-circuit current	$\lvert I_{SC\,max} \rvert$			10	mA
Message $\overline{D}$					
H output voltage (at $\lvert I \rvert = 0.2$ mA)	V_{qH}	$V_{SS}-3$		V_{SS}	V
L output voltage (at $\lvert I \rvert = 1$ µA)	V_{qL}			0.35	V
Short-circuit current	$I_{SC\,max}$			10	mA
Tone I (see fig. 5)					
H output voltage (loud) (see test circuit 1)	V_{qHl}	$\frac{6}{10}\,V_{SS}$	$\frac{9}{10}\,V_{SS}$	V_{SS}	V
L output voltage (see test circuit 1)	V_{qL}			100	mV
H output voltage (medium) (see test circuit 1)	V_{qHm}		$\frac{3}{10}\,V_{SS}$		V
H output voltage (soft)	V_{qHs}		$\frac{1}{10}\,V_{SS}$		V
Turn-off damping (referred to operating level)	a	60	80		dB
Sequence frequency	$\frac{1}{T}$		appr. 2		Hz
Tone frequency	f_{tone}		appr. 1.7		kHz
Duty cycle	t_1/T		appr. 1/4		
Tone II (see fig. 6)					
H output voltage (see test circuit 2)	V_{qH}	$\frac{1}{2}\,V_{SS}$	$\frac{3}{4}\,V_{SS}$	V_{SS}	V
L output voltage (see test circuit 2)	V_{qL}			100	mV
H output voltage (soft) (see test circuit 2)	V_{qHs}		$\frac{1}{4}\,V_{SS}$		V
Turn-off damping (referred to operating level)	a	60	80		dB
Sequence frequency	$\frac{1}{T}$		appr. 2		Hz
Tone frequency	f_{tone}		appr. 1.7		kHz
Duty cycle	t_1/T		appr. 1/4		

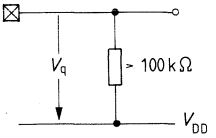
Block diagram



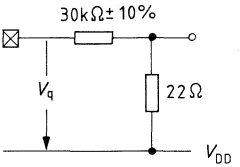
Pin configuration

Pin. No.	Function	Pin No.	Function
1	Transmission frequency SF	10	V_{SS}
2	Message frequency DF	11	Warning tone suppression $\overline{H}$
3	Loud-circuit La	12	Station search SU
4	Message $\overline{D}$	13	Tone II (undelayed)
5	Lamp L	14	V_{DD}
6	Key radio $\overline{TR}$	15	Tone I (delayed)
7	Key message $\overline{TD}$	16	Y for testing purposes
8	Area identification $\overline{BK+TS}$	17	Reset ZR
9	Transmission identification SK	18	Test pin PR

Test circuit 1
tone I



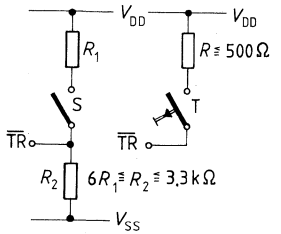
Test circuit 2
tone II



Measuring the turn-off damping

1. The supply voltage is kept constant during the measurement.
2. The measurement is taken with respect to the V_{DD} pin.
3. The measurement is taken selectively for the basic frequency.

Connection of the $\overline{TR}$ input



Key T: Reset of the function by reapplying the supply voltage

Figure 1

Connection of the $\overline{TD}$-input

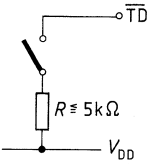


Figure 2

Suggested connection of the H-Input

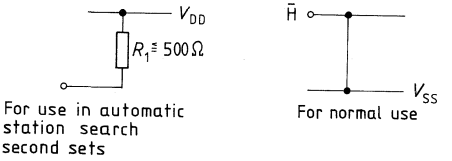


Figure 3

Circuit for automatic reset upon turn-on

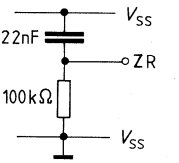


Figure 4

Output signals of the tone I output

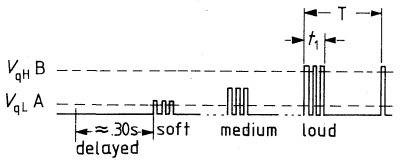


Figure 5

Output signals of the tone II output

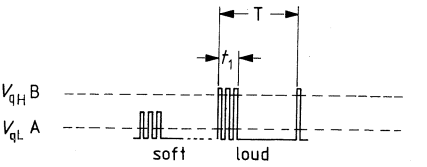


Figure 6

Functional description of the S 551

The S 551 contains 7 function blocks. The 4 blocks used for the recognition of the 125 Hz VDS tone constitute the largest portion of the circuit. They comprise a PLL-circuit (phase-locked loop), an integrator, a memory, and a frequency divider. The PLL-circuit is a 2-stage synchronous counter, the first portion of which can be switched between 28 and 29 counting steps. The subsequent divider has a 3-bit and a 4-bit output. A 57 kHz rectangular signal is used as the clock frequency for the block. The two portions of the counter are interconnected in such a way that a 125 Hz signal appears at the 4-bit output as mean value. An incoming DF is applied to an Exclusive-OR-gate by means of this signal; the output of this gate causes the switching of the counting steps of the first PLL-divider stage. The frequency at the 4 bit output is thereby displaced in time, until a stable divider ratio is produced at the output of the Exclusive-OR-gate. However, this is only possible when the DF amounts to approximately 125 Hz.

As an indicator whether the PLL has recognized a DF as correct, the output of a second Exclusive OR-gate (Y) is used. It has, as its input signals, the DF and also a reference frequency from the PLL divider for comparison, which has been phase-shifted by 90°. The output Y is consistently at an H-potential as long as the DF is proper. Small deviations of the DF with respect to the reference frequency are indicated by "low"-times within a Y-period. In the case of major frequency deviations, the PLL is continuously trying to adjust the reference frequency to the DF, which results in a Y signal appearing to be irregular at first.

For the evaluation of the Y-signal, the integrator is used. It is an 11-bit synchronous up-down counter, which is defined in its counting direction by "Y". As clock frequencies, two clocks derived from the PLL circuit are available (f_1 = 57 kHz 2^{-2} and f_2 = 57 kHz 2^{-3}). These clock signals are also selected by the Y-signal. The integrator is constructed in such a way, that due to Y = high — for incrementing slowly — and Y = low — for decrementing fast — the two possible counting combinations are achieved. For this reason a full-counting of the integrator is only possible when the L-portion within a Y-period is smaller than 1/3. An evaluation of the counter contents is done through a hysteresis circuit, with thresholds at the counter contents 1/4 full and 3/4 full. In order to make the DK less sensitive to short-time turn-offs of the VRF-broadcasting frequencies, the integrator is followed by a memory. The memory is a 4-bit synchronous incrementer/decrementer. Its clock frequency is about 57 kHz 2^{-14} and is derived from a central frequency divider. The counting direction of the memory is defined by a hysteresis circuit. When the hysteresis circuit indicates a full integrator, the memory will still be empty, but its output "DK" (internal signal) already indicates a message. From this point on, the counter increments until it is full and remains that way. At this counting position, the memory is able to compensate for a gap in the VDS frequency of approximately 4.6 s. After this time the memory is empty and the DK signal goes high. A 9-bit counter serves as a central frequency divider. It has been constructed for the first 5 bits as a synchronous counter and for the rest as an asynchronous counter. The various input clocks used in the IC are taken from the appropriate divider stages or are decoded. As input clock the reference frequency of 125 Hz from the PLL is used.

An additional block consists of logic circuits which are not directly related to each other.

The inputs $\overline{TR}$, $\overline{TD}$, $\overline{BK + TS}$, SK and $\overline{H}$ and the internal signal DK determine the output functions L (lamp), La (loud circuit), $\overline{D}$ (message decoding), SU (station searching).

A low level at input $\overline{TR}$ (key broadcast) indicates that no VRF operation is intended. The input operates in a bistable way and a low resistance drive is applied to the switching mode. When the supply voltage is turned on again, the input is automatically set to VRF operation.

A low level at input $\overline{TD}$ (key message) indicates that only road traffic information messages are to be reproduced.

A low level at input $\overline{BK + TS}$ (area identification or key "only broadcast recognition") indicates that either the area identification circuit (BK IC) has recognized the wanted area identification signal or that area distinguishing is not wanted.

A high level from the SK analog IC at input SK (transmission identification) indicates that a VRF station has been received.

Through a low level at input $\overline{H}$, the circuit can be reprogrammed for the use in a station-searching second set. This function acts upon the warning tone.

The lamp output L shows a high level when the requested kind of operation may be performed. For this purpose the SK (transmission identification) input must receive an H-signal which means that a station with the proper transmission identification is being received. In addition, the $\overline{BK + TS}$ (area identification or transmission identification only) input must receive an L-signal which means that a station of the requested area is being received or that no area identification is requested.

The same applies if no VRF function has been requested. Depress "broadcast key". ($\overline{TR} = 0$).

$L = SK\ \overline{BK + TS}$

Output La from the loud-switch controls the loudspeaker amplifier. With a high level it sets the loudness to:

$La = D + TR + L \cdot \overline{TD}$

The message-identification output $\overline{D}$ indicates with a low level that a message is being recognized and the station received is located in the requested area. With the key "broadcast" this signal is suppressed.

$D = DK \cdot L \cdot \overline{TR}$

Station search output SU controls the automatic VRF station searching motion.
(High level: search, low level: stop).

$\overline{SU}$ = TR + L + stop pulse (SK)

The stop pulse lasts about 0.5 s. It is produced every time a VRF station has been found (SK = high). At the same time the BK IC checks the accuracy of the area identification.

(Own 4-bit asynchronous counter with frequency 57 kHz 2^{-12}). Station search is started with a delay to avoid response to brief noise signals received.

The output tone 1 produces a warning when no VRF station is received from the wanted area.

Tone 1 = $\overline{TR + L}$

However, the tone will not be activated until approx. 30 s after this condition has been established. Through a dynamic stage it is producted at first four times soft then four times medium and finally loud.

(The delay and the dynamic control consist of a 5-bit asynchronous counter with a clock frequency of approx. 57 kHz 2^{-17}).

The output tone II differs from tone I by generating a non-delayed warning tone in not more than two dynamic stages (four times soft and then loud). For this function a resistor to V_{DD} is required.

In connection with station search second sets a warning tone will be useless if it is not possible to receive a VRF station (poorly covered area). In this case the station search second set should continue searching to discover a VRF station as soon as possible. Only after having found a VRF station, which, however, does not belong to the wanted area, will the warning tone enable improved operations.

Operation

If no VRF station can be received, the SU signal remains low. As soon as a VRF station has been found during the periodic searches, periodic pulses with SU = high occur. When the $\overline{H}$-input is low, the warning tone is blocked if SU remains low for a period exceeding 20 s.

Note

Inputs PR and Y are intended for testing. They must not be externally connected for other purposes.

Area Decoder for FM Road Traffic Information Service

S 552

MOS circuit

Type	Ordering code	Package outline
S 552	Q 67100-Z110	DIP 16

The MOS circuit S 552, built up in depletion load technology, is an extension of the two bipolar circuits S 0280 (station decoder), S 0281 (message decoder) and the MOS circuit S 551 (message decoder). These circuits constitute the main portion of a traffic broadcast decoder used in car radios.

The S 552 recognizes the identification frequency of a VRF station of a specific region and switches only traffic messages of this station to the loudspeaker. The S 552 has been designed for 6 different area frequencies, which can be pre-selected at inputs $\overline{A}$ to $\overline{F}$.

Maximum ratings (all voltages referred to $V_{DD} = 0$ V)

		min.	max.	
Supply voltage	V_{SS}	−0.3	18	V
Input voltage	V_i	0	V_{SS} +0.3	V
Total power dissipation	P_{tot}		400	mW
Power dissipation per output	P_q		100	mW
Storage temperature	T_{stg}	−40	125	°C

Operating range (referred to $V_{DD} = 0$ V)

Supply voltage range	V_{SS}	9 to 16		V
Ambient temperature range	T_{amb}	−25 to 85		°C

Characteristics (all voltages referred to $V_{DD} = 0$ V)

		min	typ	max	
Supply current	I_{SS}			15	mA
Inputs					
Transmission frequency SF					
(57 kHz)					
(internal pull-high resistor)					
Area frequency BF					
(internal pull-high resistor)					
(A = 23.79 Hz, B = 28.32 Hz,					
C = 34.98 Hz, D = 39.65 Hz,					
E = 45.75 Hz, F = 54.04 Hz)					
H pulse width	t_{WH}				
(Duty cycle approx. 1:2)					
L pulse width	t_{WL}				
(Duty cycle approx. 1:2)					
H L transition time	t_{THL}			3.5	µs
L H transition time	t_{TLH}			3.5	µs
Harmless H-input current	I_{iH}			1	µA
L input source resistance (to V_{DD})	R_{iQL}			10	kΩ
L input source resistance (to $V_{DD}+1$ V)	R_{iQL}			6	kΩ
Transmission identification SK					
(from DK analog circuit)					
(internal pull-high resistor)					
Harmless H input current	$\lvert I_{iH} \rvert$			1	µA
L input source resistance (to V_{DD})	R_{iQL}			5	kΩ
L input source resistance (to $V_{DD}+1$ V)	R_{iQL}			3	kΩ

Characteristics (all voltages referred to $V_{DD} = 0$ V)

		min	typ	max	
Programming inputs $\overline{A}$...$\overline{F}$ (see fig. 1) (Internal pull-high resistor)					
Harmless H input current	$\lvert I_{iH} \rvert$			1	µA
L input source resistance (to V_{DD})	R_{iQL}			5	kΩ
L input source resistance (to $V_{DD}+1$ V)	R_{iQL}			3	kΩ
Reset input ZR (see fig. 2)					
H input voltage (Reset)	V_{iH}	$V_{SS}-1.3$		V_{SS}	V
L input voltage (released)	V_{iL}			2	V
H pulse width	t_{WH}	20			µs
Required input current	I_i			10	µA
Area identification $\overline{BK}$					
H output voltage (at $\lvert I \rvert < 10$ µA)	V_{qH}	$V_{SS}-1.3$		V_{SS}	V
L output voltage (at $\lvert I \rvert < 10$ µA)	V_{qL}			1.5	V
Short-circuit current (Continuously short-circuit-resistant)	$I_{SC\,max.}$			1	mA

Connection of programming inputs $\overline{A}$...$\overline{F}$

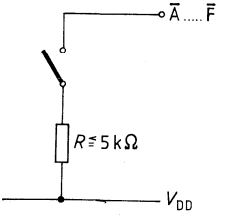


Figure 1

Circuit for automatic reset upon turn-on

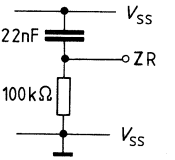
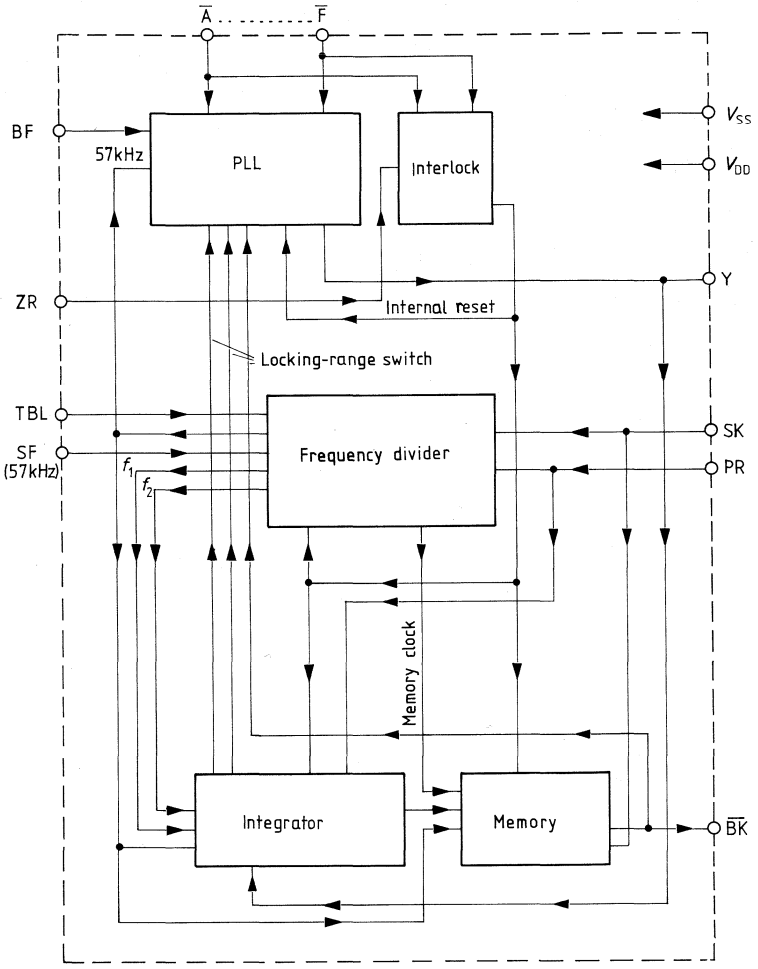


Figure 2

Block diagram



Pin configuration

Pin No.	Function	
1	Area frequency BF	
2	Transmission identification SK	
3	Reset ZR	for testing purposes
4	Testing PR	
5	Y input/output	
6	Clock blocking TBL	
7	Station frequency SF	
8	V_{SS}	
9	V_{DD}	
10	Area selection $\overline{F}$	
11	Area selection $\overline{E}$	
12	Area selection $\overline{D}$	
13	Area selection $\overline{C}$	
14	Area selection $\overline{B}$	
15	Area selection $\overline{A}$	
16	Area identification BK	

Functional description of the S 552

The area decoder circuit S 552 is an extension of the VRF decoder system. It is used to recognize the area frequency (identification frequency of the VRF station of a region). The S 552 has been designed for 6 different area frequencies (BF), which are preselected by means of an L-level at the programming inputs $\overline{A}$-$\overline{F}$. Preselection may be performed by either operating a switch, which briefly opens all inputs when turned, or a switch which bridges several inputs simultaneously.

The circuit contains a PLL portion like the S 551. It consists of three synchronous counters in series. The first of these counters can be switched between the two counting positions 23 and 25. Furthermore, two additional counter combinations 21/27 and 19/29 can be used to extend the locking range. The locking range is switched by an integrator following the PLL. The second divider of the PLL circuit can be switched externally through the $\overline{A}$-$\overline{F}$ inputs. With an L-level at $\overline{A}$ it divides by 25, at $\overline{B}$ by 21, at $\overline{C}$ by 17, at $\overline{D}$ by 15, at $\overline{E}$ by 13 and at $\overline{F}$ by 11. In order to convert a 57 kHz SF-signal into a BF-signal, the PLL contains an additional 2-bit divider. Corresponding to the programming inputs $\overline{A}$...$\overline{F}$ used, the PLL generates an internal BF signal. An externally applied BF (at the BF input) is applied to an exclusive-OR-gate together with the internal signal. The output of this gate causes switching of the counting steps at the first divider stage (e.g. 23/25). Thereby the internal BF is shifted in phase until a stable switching ratio has been obtained.

As an indication that the PLL has recognized a BF properly, the output of a second exclusive OR (Y-signal) gate is used; the inputs of this gate are the internal reference frequency, shifted by 90°, and the BF.

In case of a stable switching ratio mentioned above, Y has a high level and thereby indicates the recognition of a proper BF. If the BF received is wrong, the Y output shows an irregular signal.

As the S 551, the S 552 also contains an integrator and a memory. Both blocks receive their clock frequency from an internal frequency divider. This frequency divider essentially consists of a synchronous counter, which generates the integrator clock, and an asynchronous divider operated in series, which supplies the memory clock.

The integrator is an 8-bit synchronous up-down counter. Its clock frequency depends on the PLL output. At Y = high it reaches approx. 2370 Hz and at Y = low 4750 Hz. In addition, the counting direction of the integrator is determined by the level of the Y signal. At high clock frequency it counts down (at Y = low) and at low frequency it counts up (Y = high). The minimum duty cycle of the Y signal for upcounting of the integrator is $<1:3$ for Y = low.

The contents of the counter are evaluated by means of a hysteresis circuit with thresholds at counter contents 1/4 full and 3/4 full. In addition, the integrator stages with the highest significance determine a change of the locking range in the first PLL divider stage.

When the integrator is empty (0 to 1/4), the PLL-divider can be switched between 19 and 29 counting steps, when the integrator has been partially filled (1/4 to 1/2) between 21 and 27 steps and if it is filled more than 1/2 or if $\overline{BK}$ = low between 23 and 25 counting steps.

When the integrator is full or when the memory is not entirely empty, the output $\overline{BK}$ = low. The memory will bridge a brief disappearance of SK or BF. It consists of a 4-bit synchronous up/down counter and the maximum storage time amounts to approx. 6 s. Its clock frequency is approx. 2.3 Hz. When the hysteresis output shows a full integrator, the memory counts up and for an empty integrator down. The hysteresis signal and the Q1 outputs of the individual memory bits form the $\overline{BK}$-signal through a gate. Therefore the $\overline{BK}$ output remains low for additional 6 s after the integrator has counted down to zero.

Note

The inputs TBL, PR, and Y are intended for testing purposes. They must not be connected externally.

MOS circuit

Type	Ordering code	Package outline
SAB 3209	Q 67100-Y 395	DIP 18

The receiver circuit SAB 3209, developed in MOS depletion technology, evaluates the IR signals coming from the transmitter circuit SAB 3210. Through a serial interface, which is externally accessible, the instructions are forwarded to the program memory and the analog memory. The SAB 3209 permits control of 16 programs and three analog functions. The circuit additionally contains two spare outputs and one input or output for the ON/OFF function.

Features

- At the serial interface (I-bus) 30 instructions can be applied in addition to those intended for the SAB 3209, i.e. for teletext.
- Through the serial interface, instructions can be transferred into the SAB 3209 directly, whereby these instructions have an absolute priority over IR signals coming from the transmitter.
- The program outputs are short-circuit-resistant and can be set externally.
- The SAB 3209 can be operated with the built-in oscillator as well as with an external clock.

Maximum ratings (referred to $V_{DD} = 0$ V)

		min.	max.	
Supply voltage	V_{SS}	−0.3	18	V
Input voltage	V_I	−18	0.3	V
Total power dissipation	P_{tot}		500	mW
Power dissipation per output	P_q		100	mW
Storage temperature range	T_{stg}	−55	125	°C

Operating range (referred to $V_{DD} = 0$ V)

Supply voltage range	V_{SS}	11 to 16	V
Ambient temperature range	T_{amb}	0 to 70	°C

■ Not for new design

Characteristics (referred to $V_{DD} = 0$ V)

		min	typ	max	
Current consumption (outputs not connected)	I_{DD}		5	10	mA
Inputs					
Clock input CLKI					
L input voltage	V_{iL}	0		$V_{SS}-7$	V
H input voltage	V_{iH}	$V_{SS}-1$		V_{SS}	V
Input current	I_i			15	µA
Transition times	t_{THL}, t_{TLH}			4	µs
Frequency	f	20	60	70	kHz
Remote control signal input RSIG					
Input alternating voltage	V_{iH}	$V_{SS}-1$		V_{SS}	V
	V_{iL}	0		$V_{SS}-3.5$	V
Input resistance	R_i	0.2			MΩ
Serial interface inputs DLEN and DATA					
L input voltage	V_{iL}	0		$V_{SS}-7$	V
H input voltage	V_{iH}	$V_{SS}-1$		V_{SS}	V
H input current ($V_i = V_{SS}$) (internall pull-low resistor)	I_{iH}			2	mA
Delay time + transition time	$(t_D + t_T)_{HL}$		1		µs
	$(t_D + t_T)_{LH}$		1		µs
Program stepping input PC					
H input voltage	V_{iH}	$V_{SS}-1.5$		V_{SS}	V
L input voltage	V_{iL}	0		$V_{SS}-7$	V
H input current ($V_i = V_{SS}$) (internall pull-low resistor)	I_{iH}			10	µA

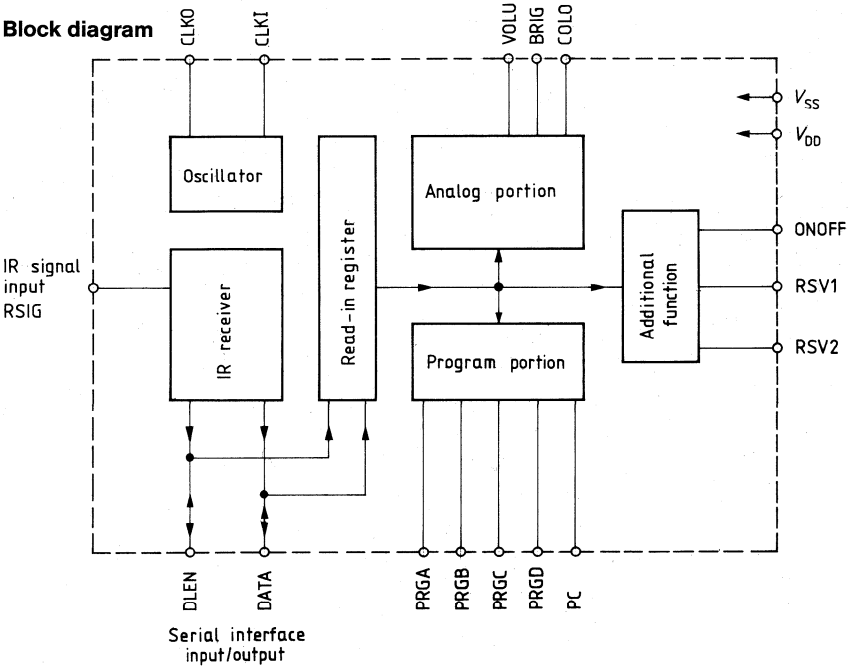
■ Not for new design

Characteristics (referred to $V_{DD} = 0$ V)

		min	typ	max	
Outputs					
Serial interface outputs					
H output voltage ($I_{load} \leqq 200$ mA)	V_{qH}	V_{SS} –1.5		V_{SS}	V
L output voltage ($I_q = 10$ µA)	V_{qL}	0		0.35	V
Delay and transition time ($C_L = 50$ pF referred to CLKO, V_{iLP})	$t_{DH} + t_{THL}$ and $t_{DL} + t_{TLH}$			5	µs
Program memory outputs PRGA, PRGB, PRGC, PRGD					
H output voltage ($I_q = 0.1$ mA)	V_{qH}	V_{SS} –0.5		V_{SS}	V
L output voltage ($I_q = 10$ µA)	V_{qL}	0		1.0	V
Program stepping output PC					
H output voltage ($I_q = 0.3$ mA)	V_{qH}	V_{SS} –1.5		V_{SS}	V
L output voltage (no load)	V_{qL}	0		2	V
Analog function outputs COLO, BRIG, VOLU					
H output voltage ($I_q = 1$ mA)	V_{qH}	V_{SS} –1.5		V_{SS}	V
L output voltage ($I_q = 1$ µA)	V_{qL}	0		0.35	V
Standby and spare outputs ONOFF, RSV 1, RSV 2					
H output voltage ($I_q = 0.3$ mA)	V_{qH}	V_{SS} –1.5		V_{SS}	V
L output voltage ($I_q = 1$ µA)	V_{qL}	0		0.35	V
Clock output CLKO					
H output voltage (no load)	V_{qH}	V_{SS}–1		V_{SS}	V
L output voltage (no load)	V_{qL}	0		1	V

■ Not for new design

Block diagram



Pin configuration

Pin No.	Function
1	V_{SS}, +supply voltage
2	CLKO, clock output
3	CLKI, clock input
4	PRGD, program control output
5	PRGC, program control output
6	PRGB, program control output
7	PRGA, program control output
8	PC, program change strobe input/output
9	RSV2, spare output
10	RSV1, spare output
11	VOLU, volume control output
12	ONOFF, standby output
13	BRIG, brightness output
14	COLO, color contrast output
15	RSIG, signal input, remote control
16	DLEN, I-bus input/output
17	V_{DD}, – supply voltage
18	DAT, I-bus input/output

■ Not for new design

Description of functions

1 Infrared receiver (pin RSIG)

The infrared receiving portion accepts the IR signal, processes it and transfers the instructions received to the serial interface. The IR-signal consists of alternating current pulses with a frequency of approx. 30 kHz and a duration of approx. 0.5 ms per cycle. The instructions are transferred as 7-bit words (1 start bit, 6 information bits) in the biphase code. See timing diagram.

The infrared signals are repeated approx. every 120 ms. All instructions are issued by the receiving portion as repeat-instructions, with a sequence-frequency equal to that of the incoming IR-signals.

2 Serial interface (I-BUS) as an output and input (pins DLEN, DATA)

Output at the serial interface (I-BUS) is performed as shown in the timing diagram 2. The outputs are open-drain stages with built-in load resistors, which may also be used as inputs. All instructions may also be entered via the serial interface, (the infrared instructions will not be processed in the circuit after they have passed the serial interface).

The input is tested to protect the transfer of the instructions against capacitive and inductive noise pulses. Therefore, the leads at the serial interface must be kept close together.

Entries via the serial interface have absolute priority over infrared entries.

It is possible to read out instructions through the serial interface and change them at the same time through an external circuit in such a way that they cannot be interpreted any longer by the receiver portions. For example, the pin DLEN of the instructions for direct program selection can be kept on high level for two clock pulse periods beyond the output time, whereby the program memory is no longer addressed and the program instructions can be used as digit-instructions for other purposes (e.g. teletext page selection).

■ Not for new design

3 Analog-value memory (outputs VOLU, BRIG, COLO)

The SAB 3209 contains 3 analog-value memories for setting volume, brightness and color saturation.

The analog values can be altered in approx. 64 steps. The speed of alteration corresponds to the sequence-frequency of the repeat instructions (approx. 8 Hz). The analog values are put out as square pulses with a frequency of approx. 1 kHz, whereby the duty cycle corresponds to the analog value. The analog voltage value originates in an external low-frequency passing filter through formation of the mean values of timing.

By means of the instruction "normal position", the analog memories are set to a mask-programmed basic position ($\nu_{VOLU} = 1/3$, $\nu_{BRIG} = \nu_{COLO} = 1/2$, whereby $\nu = t_{High}/T$). When the supply voltage rises starting at 0, the analog values are also set to the normal position.

Volume control output VOLU

The volume output is kept internally on a low level

- when the quicktone flipflop is set,
- when the circuit is in a "standby" mode,
- when pin PC is on a high level.

Quicktone

An appropriate instruction sets a flipflop.
The flipflop is reset:

- by instruction "Vol+",
- by condition "standby",
- by an instruction to the program memory,
- by the instruction "normal position".

As long as the quickton flipflop is set, the volume output is kept "low".

As long as the circuit remains in the "standby" condition, the adjustment instructions for the analog memory are ineffective.

■ Not for new design

4 Program memory
(outputs and inputs PRGA, PRGB, PRGC, PRGD)

The program memory consists of a 4-bit ring counter which permits the addressing of 16 programs.

The 16 programs may be addressed through remote control by selecting 1...16 or through up- and downcounting of the ring counter.

When the supply voltage rises starting at zero, the program outputs are set to LLLH. By changing one mask it is possible to set a different program. The outputs of the program memory are also effective as inputs and may be set or reset externally through a low-resistance control.

Strobe output, stepping sequence input
(pin PC)

When the program counter receives an instruction via remote control, or the supply voltage rises starting at zero, a positive pulse is produced at output PC. For the duration of a positive potential the volume output is kept "low" (muting).

The output may be connected to a capacitor to extend the muting (up to approx. 0.5 s).

By means of the same capacitor, changes at the program memory outputs will be completed when the strobe signal occurs.

Pin connection PC may also be used as an input. If a positive potential is applied externally, the program counter proceeds by one step. Thereby, the external capacitor will have a debouncing effect. During "standby" condition the output "PC" is on a static positive level.

■ Not for new design

5 Additional control functions

Standby output/input (pin ONOFF)

This pin controls the power supply by means of a transistor. When a program is called up — and also in connection with some other instructions specified in table 1 – the set is turned on via this output.

In = low, standby = high

Through the instruction "standby" the set is put into a "standby" mode. When the supply voltage rises starting at zero, the set is also switched to „standby".

Pin connection ONOFF also acts as an input when controlled from a low resistance source, e.g. with a wiping contact at the mains-switch.

Spare outputs

Pin RSV1

The output is controlled by a toggle-flipflop. With each depression of the corresponding button of the transmitter the output changes into the opposite condition.

The preference position is high.

The position is set:

— when the supply voltage is turned on,
— when condition "standby" exists,
— when the instruction "normal position" is issued.

Pin RSV2

The output is controlled by a toggle-flipflop. With each depression of the corresponding button of the transmitter the output changes into the opposite condition.

The preference position is low

The position is set:

— when the supply voltage is turned on,
— when condition "standby" exists,
— when the instruction "normal position" is issued.

■ Not for new design

Table 1
Coding of instructions on the I BUS and for IR transmission

No.	Code	Instruction
	FED CBA	
0	000 000	Normal position/ON
1	001	Quicktone (muting)
2	010	Standby
3	011	Spare 1
4	100	Program step + /ON
5	101	Program step −/ON
6	110	ON
7	111	Spare 2/ON
40	101 000	Volume +
41	001	Volume −
42	010	Brightness +
43	011	Brightness −
44	100	Color +
45	101	Color −
46	110	
47	111	reserved for the 4th analog function

■ Not for new design

Table 1, continued
Coding of instructions on the I BUS and for IR transmission

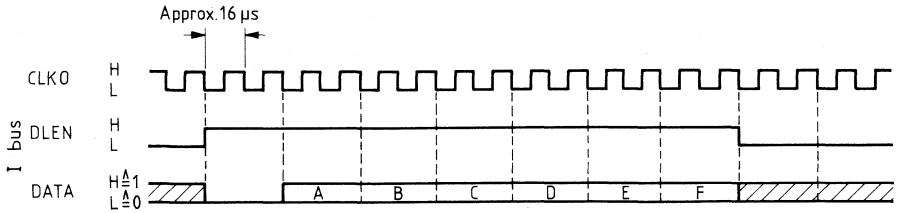
No.	Code	Instruction
	FED CBA	D C B A (PRG output)
16	010 000	L L L L /ON
17	001	L L L H /ON preferred position
18	010	L L H L /ON
19	011	L L H H /ON
20	100	L H L L /ON
21	101	L H L H /ON
22	110	L H H L /ON
23	111	L H H H /ON
24	011 000	H L L L /ON
25	001	H L L H /ON
26	010	H L H L /ON
27	011	H L H H /ON
28	100	H H L L /ON
29	101	H H L H /ON
30	110	H H H L /ON
31	111	H H H H /ON

Instructions 8 to 15, 32 to 39, and 48 to 61 are not evaluated by the circuit, but only edited through the serial interface.

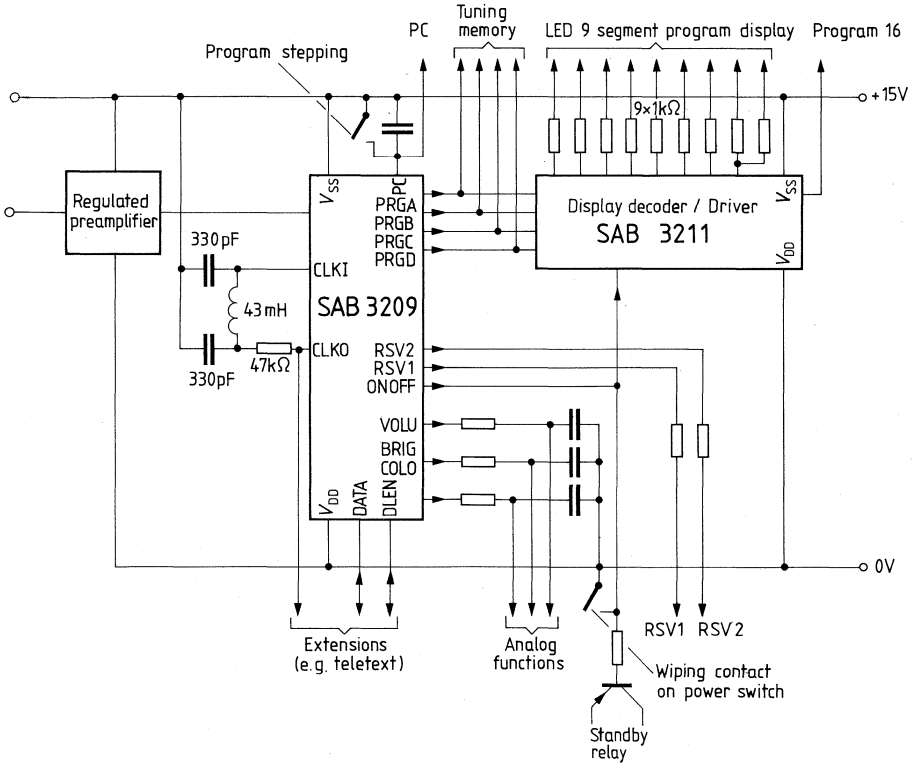
Instruction 63 (= 111 111) must be kept free (see timing diagram).
Instruction 62 (= 111 110) is the end instruction (see data sheet of SAB 3210)

■ Not for new design

Timing diagram
Serial interface (I BUS) for the input and output of instructions



External connections



■ Not for new design

MOS circuit

Type	Ordering code	Package outline
SAB 3210	Q 67100-Y 396	DIP 18

The transmitter circuit SAB 3210, developed in P-MOS depletion technology converts the instructions obtained from a matrix to a 6-bit biphase code. By means of this code a maximum of 60 instructions can be transferred via an infrared transmitting stage, to a receiver equipped with the IC SAB 3209.

Features

- 32 instructions are possible without special means – an extension to 60 is possible connecting additional diodes.
- Low power consumption of typically 3 mA (5 mA max.).
  An external npn transistor, driven by the transmitter circuit, disconnects the battery during quiescent periods, thereby extending its life period considerably.
- Large supply voltage range from 5 V to 16 V.
- A mask-programmed starting bit preceding each instruction makes an additional discrimination possible for the receiver. This feature enables the use of two independent remote control systems in the same room (e.g. for TV and radio sets).

Maximum ratings (referred to $V_{DD} = 0$ V)

Supply voltage range	V_{SS}	0.3 to 18	V
Input voltage range	V_i	V_{SS} −18 to V_{SS} +0.3	V
Total power dissipation	P_{tot}	500	mW
Power dissipation per output	P_q	100	mW
Storage temperature range	T_{stg}	−55 to 125	°C

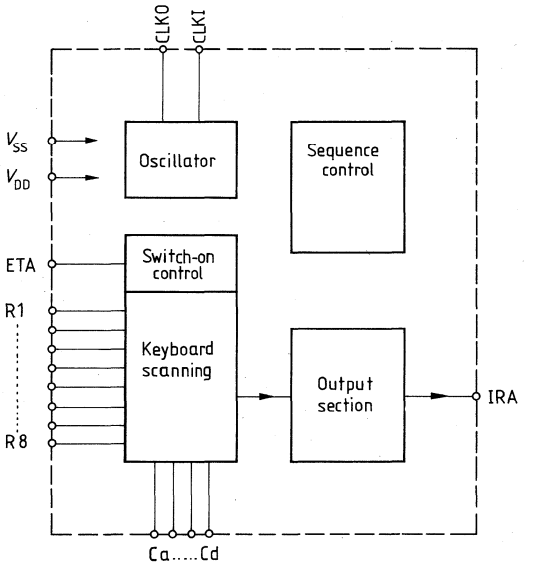
Operating range (referred to $V_{DD} = 0$ V)

Supply voltage range	V_{SS}	5 to 16	V
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics (referred to $V_{DD} = 0$ V)

		min	typ	max	
Current consumption (outputs not connected)	I_{DD}		3	5	mA
Oscillator: Clock input CLKI					
H input voltage	V_{iH}	$V_{SS}-1$		V_{SS}	V
L input voltage	V_{iL}	0		$V_{SS}-4$	V
Clock output CLKO					
H output voltage	V_{qH}	$V_{SS}-1$		V_{SS}	V
L output voltage	V_{qL}	0		$V_{SS}+1$	V
Leakage current, total current of column outputs Ca, Cb, Cc, Cd, ETA, IRA ($V_q = 10$ V; $V_{DD} = 0$ V)					
Column resistors R_a, R_b, R_c, R_d, towards – V_S	R_C	33		47	kΩ
Remote control signal – output IRA ($I_{qH} = 4$ mA; $V_{DD} \leqq -6$ V) H output voltage	V_{qH}	$V_{SS}-5$		V_{SS}	V
Switch-on transistor – output ETA H output current ($V_q = V_{SS}-4$ V)	I_{qH}	0.1		0.5	mA

Block diagram



Pin configuration

Pin No.	Function
1	V_{SS}
2	Column a
3	Column b
4	Column c
5	Column d
6	V_{DD}
7	ETA (switch-on trans. output)
8	IRA (Infrared output)
9	Row 1
10	Row 2
11	Row 3
12	Row 4
13	Row 5
14	Row 6
15	Row 7
16	Row 8
17	CLKI (oscillator input)
18	(CLKO (oscillator output)

Description of functions

The SAB 3210 operates in a wide range of supply voltages and with a very low current consumption. It is therefore suited for battery operation and for operation in a television set as a keyboard scanner from a 12 V supply. The circuit contains a control output for an npn transistor which separates the circuit from the battery as long as none of the keys has been activated.

Input keyboard

The transmitter contains an input matrix consisting of 4 columns and 8 rows. In order to enter an instruction a column output must be connected with a row input. Thereby the transmitter is turned on and a corresponding instruction is issued. Without further steps it is possible to enter 32 instructions with simple switching contacts.

With additional diodes, the instruction set can be expanded to 60. For this purpose 2 diodes are required for every additional 4 instructions. As protection against an unintended double-actuation (pushing 2 keys simultaneously) the SAB 3210 contains a column interlock. For example, 1a + 1c are recognized as an erroneous operation. Instead of a wrong instruction only the end-command is transmitted. The circuit is not interlocked against a multiple-key operation within one column (e.g. 8a + 5a = 85a) because this combination is used for extending the input capabilities from 4 x 8 instructions to 4 x (8+7) instructions.

End instruction

After release of a key, the instruction selected is repeated no more than once, depending on the exact timing of the release. After the last transmission of the selected instruction, an end instruction is transmitted which signals to the receiver that the key has been released.

Output

The transmitter converts the received instruction to a biphase code (timing diagram 1). Prior to the 6 information bits, a startbit is transmitted. This startbit permits an additional discrimination for the receiver.

Through mask-programming the startbit can be changed from 1 to 0. Therefore the same control system can be used for separate control of a television and radio set located in the same room.

The output signal is keyed with half the clock frequency ($f_{CLK}/2 \approx 30$ kHz); with this signal an infrared transmitter stage can be controlled. At rest, the output is on a high-resistance low-level.

Prior to the output of an IR instruction a pre-signal is output which facilitates gain control on the receiver side.

Timing

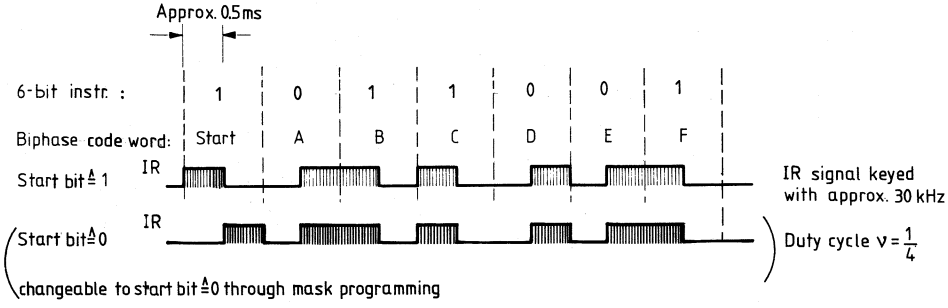
During normal operations the clock frequency is approx. 60 kHz. The instructions are issued in a time interval of approx. 120 ms, the duration of an instruction being approx. 7 ms (see timing diagram 1). Before scanning the matrix there is a debounce-delay of approx. 20 ms.

Instruction set with assignment of the instructions to the keys

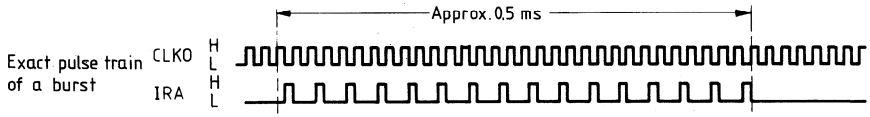
Basic instructions			Extension instructions		
Instr. No.	Code FED CBA	Key	Instr. No.	Code FED CBA	Key
0	000 000	1a	32	100 000	81a
1	000 001	1b	33	100 001	81b
2	000 010	1c	34	100 010	81c
3	000 011	1d	35	100 011	81d
4	000 100	2a	36	100 100	82a
5	000 101	2b	37	100 101	82b
6	000 110	2c	38	100 110	82c
7	000 111	2d	39	100 111	82d
8	001 000	3a	40	101 000	83a
9	001 001	3b	41	101 001	83b
10	001 010	3c	42	101 010	83c
11	001 011	3d	43	101 011	83d
12	001 100	4a	44	101 100	84a
13	001 101	4b	45	101 101	84b
14	001 110	4c	46	101 110	84c
15	001 111	4d	47	101 111	84d
16	010 000	5a	48	110 000	85a
17	010 001	5b	49	110 001	85b
18	010 010	5c	50	110 010	85c
19	010 011	5d	51	110 011	85d
20	010 100	6a	52	110 100	86a
21	010 101	6b	53	110 101	86b
22	010 110	6c	54	110 110	86c
23	010 111	6d	55	110 111	86d
24	011 000	7a	56	111 000	87a
25	011 001	7b	57	111 001	87b
26	011 010	7c	58	111 010	87c
27	011 011	7d	59	111 011	87d
28	011 100	8a	60	111 100	} not used
29	011 101	8b	61	111 101	
30	011 110	8c	62	111 110	end instruction
31	011 111	8d	63	111 111	not permitted[1]

1) because of ambiguity of the biphase code

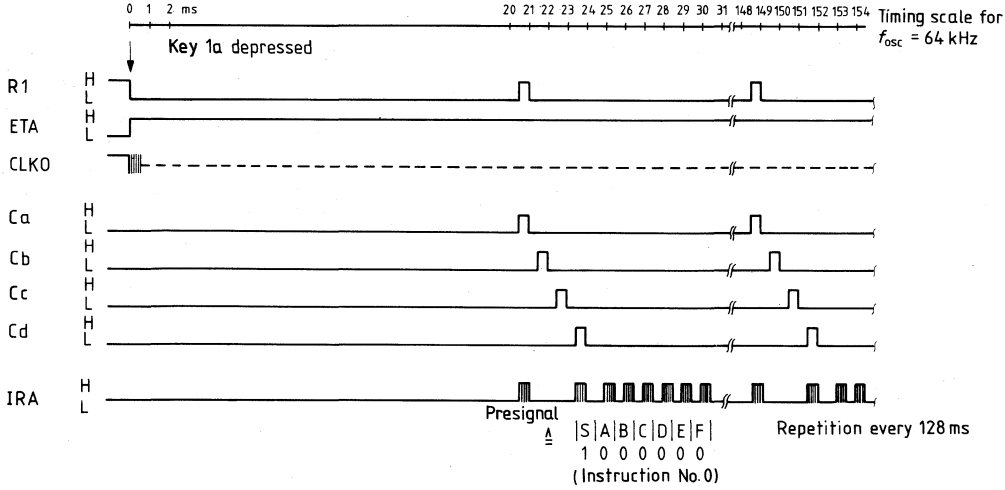
Timing diagram 1 (biphase coding, plotted without presignal)



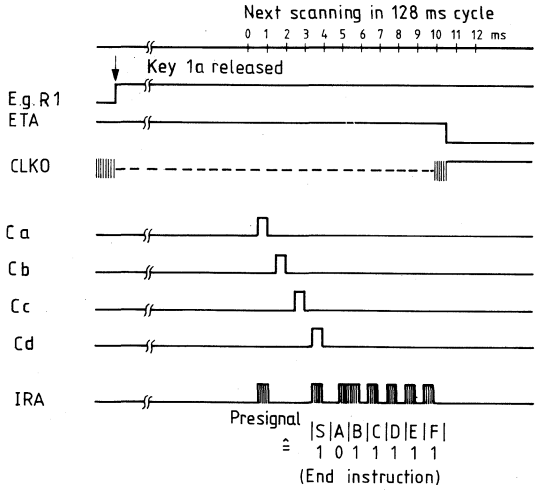
Instruction 111 111 with start bit 1 may not be programmed in order to avoid mixup with the already programmed instruction 000 000 with start bit 0



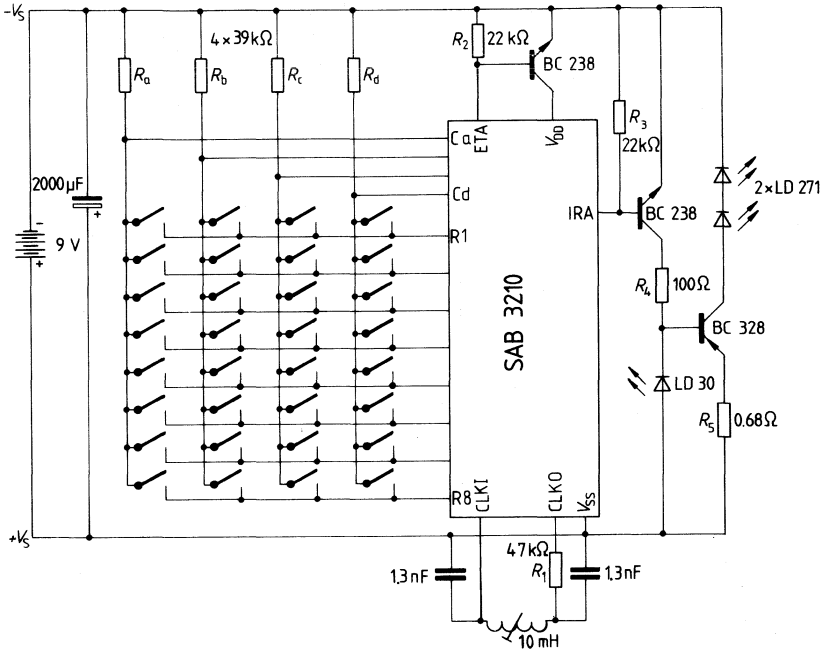
Timing diagram 2 (pushing a key)



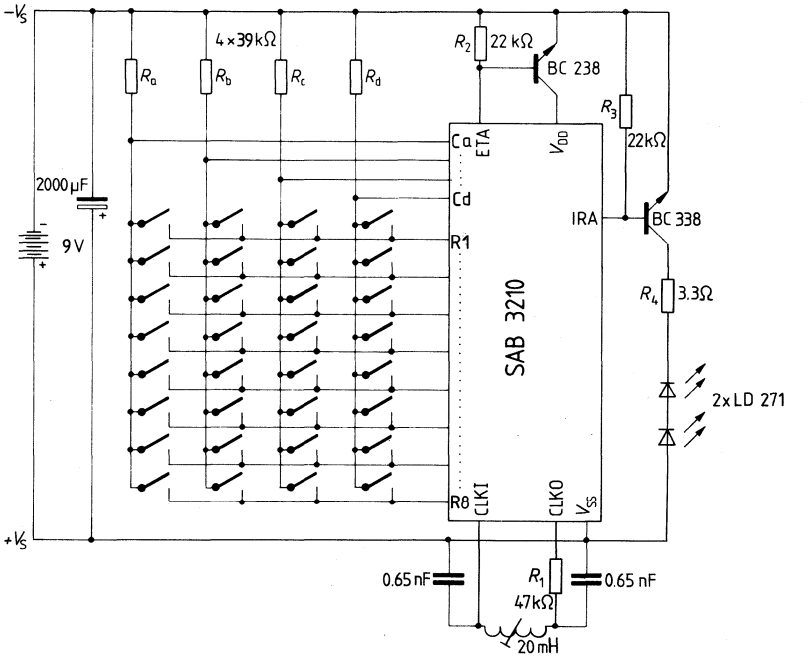
Timing diagram 3 (releasing a key)



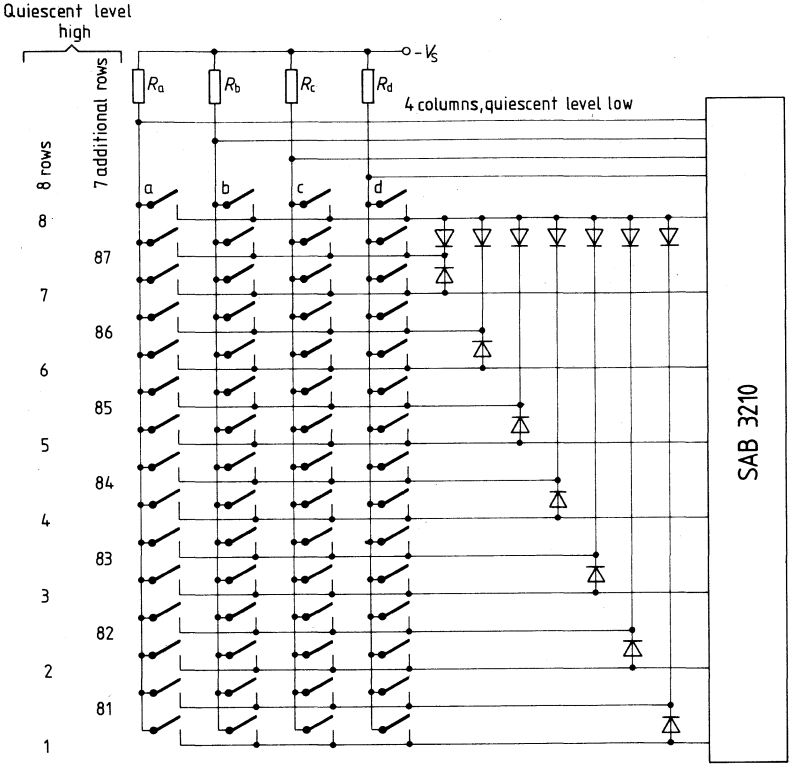
External connection of the SAB 3210 (example)



Another example of the external connection of the SAB 3210
(simplified final stage and changed oscillator circuitry)



Expanded external connection of the SAB 3210 for 60 instructions
(example)



MOS circuit

Type	Ordering code	Package outline
SAB 4209	Q 67100-Y460	DIP 18

The receiver circuit SAB 4209, developed in MOS depletion technology, evaluates the IR signals coming from the transmitter circuit SAB 3210 or SDA 2008. Through a serial interface, which is externally accessible, the instructions are forwarded to the program memory and the analog memory. The SAB 4209 permits the control of 16 programs and four analog functions. In addition, the circuit includes a keyboard changeover and one input or output for the ON/OFF function.

Features

- At the serial interface (I-bus) 30 instructions can be applied in addition to those intended for the SAB 4209, i.e. for teletext.
- Through the serial interface, instructions can be transferred into the SAB 4209 directly, whereby these instructions have an absolute priority over IR signals coming from the transmitter.
- The program outputs are short-circuit-resistant and can be set externally.
- The SAB 4209 can be operated with the built-in oscillator as well as with an external clock.

Maximum ratings (referred to $V_{DD} = 0$ V)

Supply voltage range	V_{SS}	−0.3 to 18	V
Input voltage range	V_i	V_{SS} −18 to V_{SS} +0.3	V
Total power dissipation	P_{tot}	500	mW
Power dissipation per output	P_q	100	mW
Storage temperature range	T_{stg}	−40 to 125	°C

Operating range (referred to $V_{DD} = 0$ V)

Supply voltage range	V_{SS}	11 to 16	V
Ambient temperature range	T_{amb}	0 to 70	°C

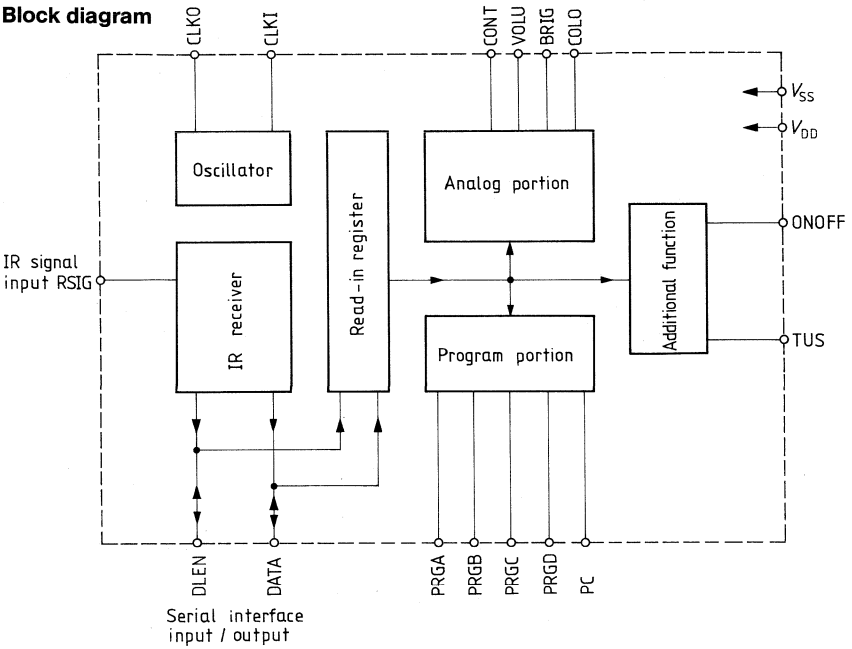
Characteristics (referred to $V_{DD} = 0$ V, $T_{amb} = 0$ to 70 °C)

		min	typ	max	
Current consumption (outputs not connected)	I_{DD}		5	10	mA
Inputs					
Clock input CLKI					
L input voltage	V_{iL}	0		V_{SS} −7	V
H input voltage	V_{iH}	V_{SS} −1			V
Input current	I_i			V_{SS} 15	µA
Transition times	t_{THL}, t_{TLH}			4	µs
Frequency	f	20	60	70	kHz
Remote control signal input RSIG					
Input alternating voltage	V_{iH}	V_{SS} −1		V_{SS}	V
	V_{iL}	0		V_{SS} −3.5	V
Input resistance	R_i	0.2			MΩ
Serial interface inputs					
DLEN and DATA					
L input voltage	V_{iL}	0		V_{SS} −7	V
H input voltage	V_{iH}	V_{SS} −1		V_{SS}	V
H input current ($V_i = V_{SS}$) (internal pull-low resistor)	I_{iH}			2	mA
Delay time + transition time	$(t_d + t_T)_{HL}$			1	µs
	$(t_d + t_T)_{LH}$			1	µs
Program stepping input PC					
H input voltage	V_{iH}	V_{SS} −1.5		V_{SS}	V
L input voltage	V_{iL}	0		V_{SS} −7	V
H input current ($V_i = V_{SS}$) (internal pull-low resistor)	I_{iH}			10	µA
Outputs					
Standby output ONOFF					
H input voltage ($I_{iH} < 1$ mA)	V_{iH}	V_{SS} −1		V_{SS}	V

Characteristics (referred to $V_{DD} = 0$ V, $T_{amb} = 0$ to 70 °C)

		min	typ	max	
Serial interface outputs					
H output voltage ($I_{load} \leq 200$ µA)	V_{qH}	V_{SS} −1.5		V_{SS}	V
L output voltage ($I_q = 10$ µA)	V_{qL}	0		0.35	V
Delay and transition time	$t_{dH} + t_{THL}$			5	µs
($C_L = 50$ pF referred to CLKI)	$t_{dL} + t_{THL}$			5	µs
Program memory outputs PRGA, PRGB, PRGC, PRGD					
H output voltage ($I_q = 0.1$ mA)	V_{qH}	V_{SS} −0.5		V_{SS}	V
L output voltage ($I_q = 10$ µA)	V_{qL}	0		1	V
Program stepping output PC					
H output voltage ($I_q = 0.3$ mA)	V_{qH}	V_{SS} −15		V_{SS}	V
L output voltage (no load)	V_{qL}	0		2	V
Analog function outputs COLO, BRIG, VOLU, CONT					
H output voltage ($I_q = 1$ mA)	V_{qH}	V_{SS} −1.5		V_{SS}	V
L output voltage ($I_q = 1$ µA)	V_{qL}	0		0.35	V
Standby and spare outputs ONOFF, TUS					
H output voltage ($I_q = 0.3$ mA)	V_{qH}	V_{SS} −1.5		V_{SS}	V
L output voltage ($I_q = 1$ µA)	V_{qL}	0		0.35	V
Clock output CLKO					
H output voltage (no load)	V_{qH}	V_{SS} −1		V_{SS}	V
L output voltage (no load)	V_{qL}	0		1	V

Block diagram



Pin configuration

Pin No.	Function
1	V_{SS}, supply voltage
2	CLKO, clock output
3	CLKI, clock input
4	PRGD, program control output
5	PRGC, program control output
6	PRGB, program control output
7	PRGA, program control output
8	PC, program change, strobe input/output
9	TUS, keyboard changeover
10	VOLU, volume control output
11	ONOFF, standby output
12	CONT, contrast output
13	BRIG, brightness output
14	COLO, color contrast output
15	RSIG, IR input
16	DLEN, I-bus input/output
17	V_{DD}, supply voltage
18	DATA, I-bus input/output

Description of functions

1 Infrared receiver (pin RSIG)

The infrared receiving portion accepts the IR signal, processes it and transfers the instructions received to the serial interface. The IR-signal consists of alternating current pulses with a frequency of approx. 30 kHz and a duration of approx. 0.5 ms per cycle. The instructions are transferred as 7-bit words (1 start bit, 6 information bits) in the biphase code. See timing diagram 1.

The infrared signals are repeated approx. every 120 ms. All instructions are issued by the receiving portion as repeat instructions, with a sequence frequency equal to that of the incoming IR signals.

2 Serial interface (I-BUS) as an output and input (pins DLEN, DATA)

Output at the serial interface (I-BUS) is performed according to the timing diagram 2. The outputs are open-drain stages with built-in load resistors, which may also be used as inputs.

In addition, all instructions may be entered via the serial interface, see timing diagram 3 (the infrared instructions will not be processed in the circuit, before they have passed the serial interface).

The input is tested to protect the transfer of the instructions against capacitive and inductive noise pulses. Therefore, the leads at the serial interface must be kept close together. Input through the serial interface has absolute priority over an infrared input. It is possible to read out instructions through the serial interface. However, at the same time they can be changed through an external circuit in such a way that they cannot be interpreted any longer by the receiver portions. For example, pin DLEN of the instructions for direct program selection can be kept on high level for two clock pulse periods beyond the output time, whereby the program memory is no longer addressed and the program instructions can be used as digit-instructions for other purposes (e.g. teletext page-selection).

3 Analog-value memory (outputs VOLU, BRIG, COLO, CONT)

The SAB 4209 contains 4 analog-value memories for setting volume, brightness, color saturation, and contrast.

The analog values can be altered in approx. 60 steps. The speed of alteration corresponds to the sequence-frequency of the repeat instructions (approx. 8 Hz). The analog values are put out as square pulses with a frequency of approx. 1 kHz, whereby the duty cycle corresponds to the analog value. The analog voltage value originates in an external low-frequency passing filter through formation of the mean values of timing.

By means of the command "normal position", the analog memories are set to a mask-programmed basic position ($\nu_{VOLU} = 1/3$, $\nu_{CONT} = \nu_{BRIG} = \nu_{COLO} = 1/2$, whereby $\nu = t_{High}/T$). When the supply voltage rises starting at 0, the analog values are also set to the normal position.

Volume control output VOLU

The volume output is internally kept on a low level

- approx. 128 ms prior to the H pulse appearing at the output after a program change instruction,
- when the quicktone-flipflop is set,
- when the circuit is in a "standby" mode,
- when pin PC is on a high level.

Quicktone

An appropriate command sets a flipflop in the actually complementary state.
The flipflop is reset

- by instruction "Vol +",
- by condition "standby",
- by an instruction to the program memory,
- by the instruction "normal position".

As long as the quicktone flipflop is set, the volume output is kept "low".

As long as the circuit remains in the "standby" condition, the adjustment instructions for the analog memory are ineffective.

After the "standby" condition is ended, the analog outputs move into the basic position.

4 Program memory (outputs and inputs PRGA, PRGB, PRGC, PRGD)

The program memory consists of a 4-bit ring counter which permits the addressing of 16 programs.

The 16 programs may be addressed through remote control by selecting 1...16 or, through up- and downcounting of the ring counter.

When the supply voltage rises starting at zero, the program outputs are set to LLLH. By changing one mask it is possible to set a different program. The outputs of the program memory are also effective as inputs, because they can be set or reset externally through a low-resistance control.

Strobe output, stepping sequence input (pin PC)

When the program counter receives an instruction via remote control, a positive pulse is produced at output PC after a certain time delay. At the start of the delay time the volume output VOLU is muted. Muting can be reverted by means of the trailing edge of the PC pulse (see timing diagram 4). The output PC can be also connected to a capacitor to extend the muting (up to approx. 0.5 s).

The same muting behavior results when the supply voltage rises starting at zero, and pin ONOFF is simultaneously kept on low (see timing diagram 5).

Pin connection PC may also be used as an input. If a positive potential is applied externally, the program counter proceeds by one step. Thereby the external capacitor will have a debouncing effect (see timing diagram 6). During "standby" condition the output "PC" is on a static positive level. With each program change a single PC pulse will be generated.

5 Standby-output/input (pin ONOFF)

This pin controls the power supply by means of a transistor. When a program is called up — and also in connection with some other instructions specified in table 1 — the set is turned on by this output.

In = low, standby = high

Through the instruction "standby" the set is put into a "standby" mode. When the supply voltage rises starting at zero, the set is also switched to "standby".

Pin ONOFF also acts as an input when controlled from a low resistance source, e.g. with a wiping contact at the mains-switch.

6 Keyboard changeover (pin TUS)

The output is controlled by a toggle-flipflop. With each depression of the corresponding key of the transmitter the output changes in the opposite condition.

The preference position is low.

The position is set

- when the supply voltage is turned on,
- when condition "standby" exists,
- when the instruction "normal position" is issued.

The output can be set and reset externally by low-ohmic connections.

When the output is in the high condition, the incoming instructions are no longer evaluated in the receiver module, but only output at the serial interface. Exception: The instructions "Keyboard changeover" (No. 7) and "Standby" (No. 2) are always evaluated.

Table 1
Coding of instructions on the I BUS and for IR transmission

No.	Code	Instruction	After instruction TUS
	FED CBA		
0	000 000	Normal position	Previous condition is maintained
1	001	Quicktone (muting)	
2	010	Standby	Standby + TR (keyboard reset)
3	011		Previous condition is maintained
4	100	Program step + /ON	"
5	101	Program step −/ON	"
6	110	ON	"
7	111	TUS/ON	TR (keyboard reset)
8	001 000	Volume +	Previous condition
9	001	Volume −	is maintained
10	010	Brightness +	"
11	011	Brightness −	"
12	100	Color +	"
13	101	Color −	"
14	110	Contrast +	"
15	111	Contrast −	"

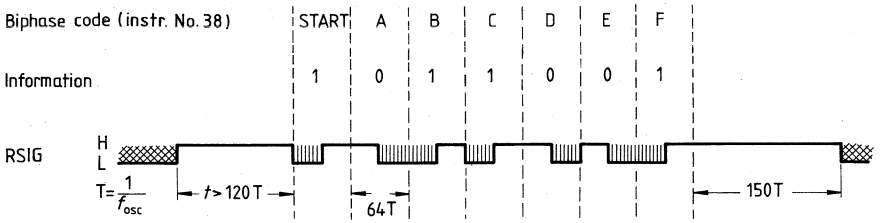
Table 1 continued
Coding of instructions on the I BUS and for IR transmission

No.	Code	Instruction	After instruction 7
	FED CBA	D C B A (PRG output)	Keyboard changeover
16	010 000	L L L L /ON	Previous condition
17	001	L L L H /ON preferred position	isn maintained
18	010	L L H L /ON	"
19	011	L L H H /ON	"
20	100	L H L L /ON	"
21	101	L H L H /ON	"
22	110	L H H L /ON	"
23	111	L H H H /ON	"
24	011 000	H L L L /ON	"
25	001	H L L H /ON	"
26	010	H L H L /ON	"
27	011	H L H H /ON	"
28	100	H H L L /ON	"
29	101	H H L H /ON	"
30	110	H H H L /ON	"
31	111	H H H H /ON	"

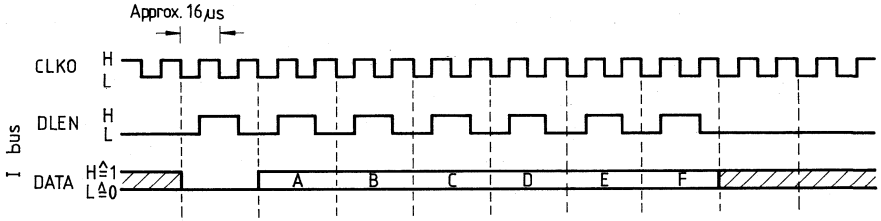
Instructions 32 to 61 are not processed by the circuit but only edited through the serial interface.

Instruction 63 (= 111 111) must remain free (see timing diagram 1).
Instruction 62 (= 111 110) is the end-instruction. (See data sheet of SAB 3210)

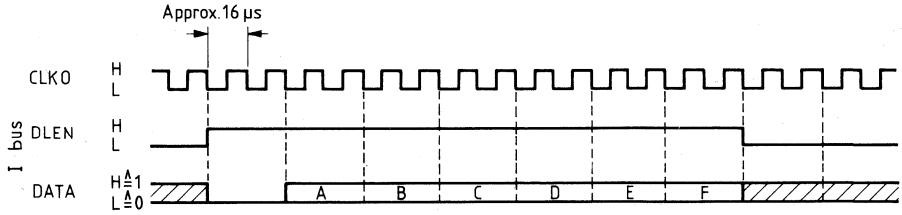
Timing diagram 1
(biphase coding)



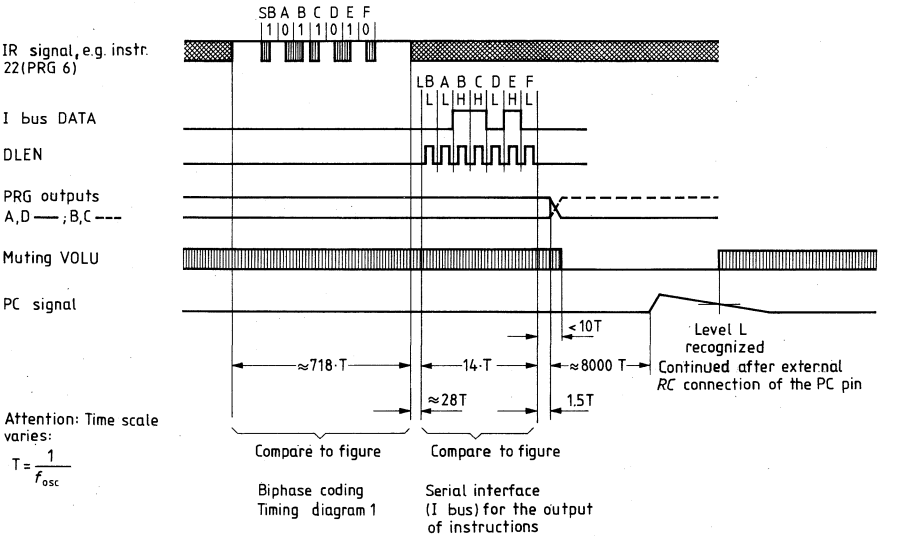
Timing diagram 2
Serial interface (I bus) for the output of instructions



Timing diagram 3
Serial interface (I bus) for the input of instructions

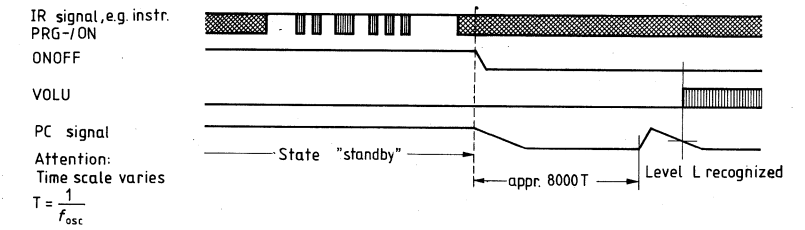


Timing diagram 4

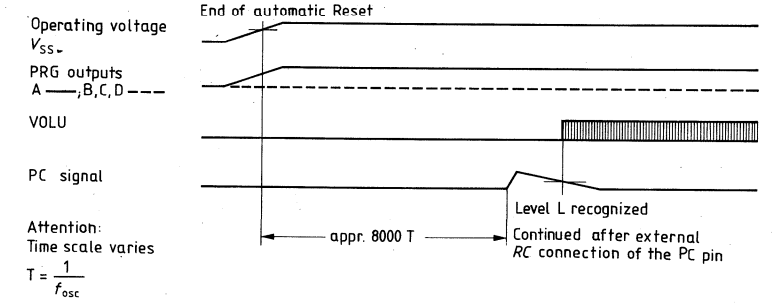


Timing diagram 5

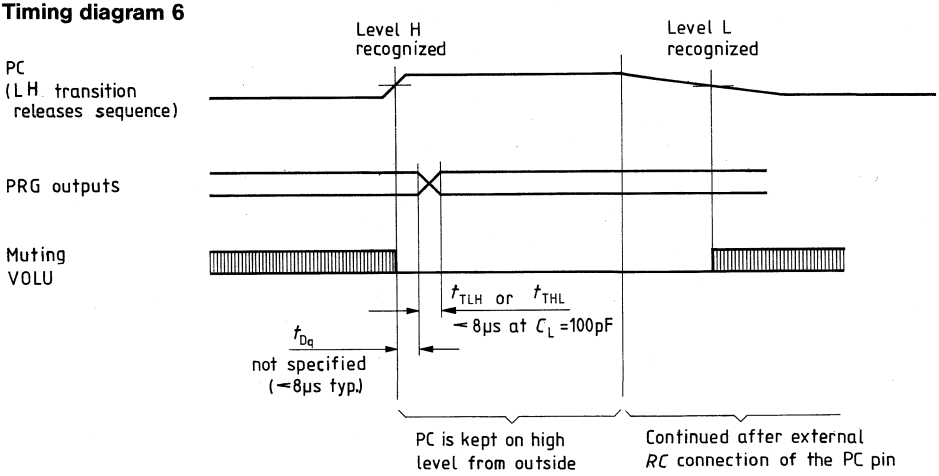
Example a) Switching on by means of an IR instruction



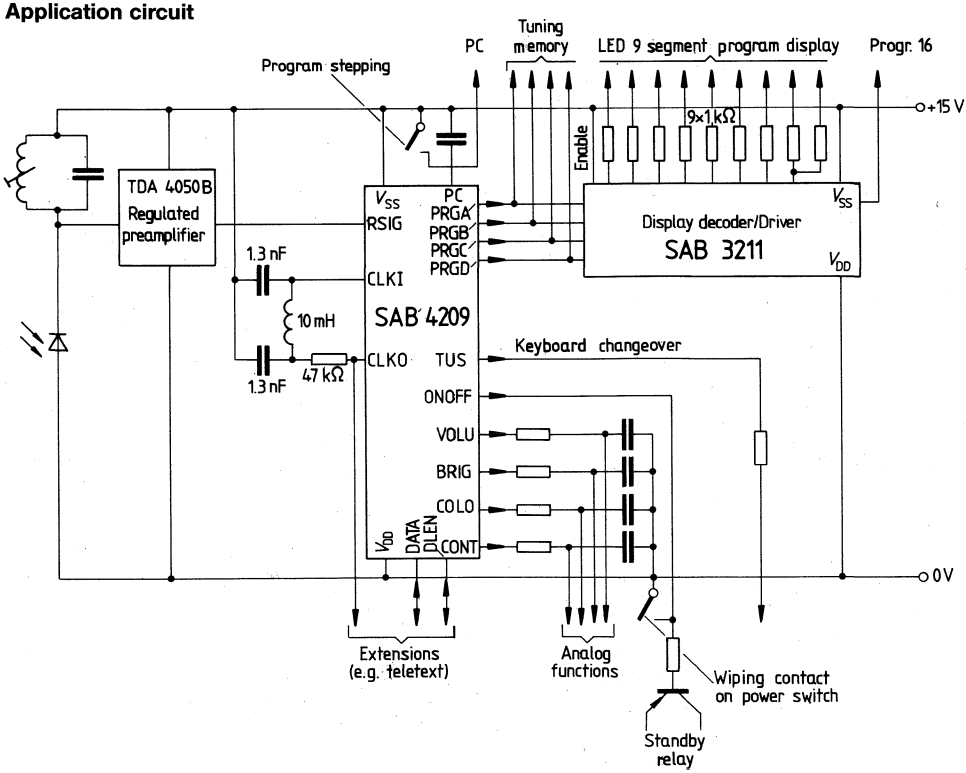
Example b) ONOFF is connected to V_{DD} during the supply voltage rise via wiping contact



Timing diagram 6



Application circuit



Switching Amplifier for 4-Channel Touch Tuning

SAS 560 S
SAS 570 S

Bipolar circuit

Type	Ordering code	Package outline
SAS 560 S	Q 67000-S30	DIP 16
SAS 570 S	Q 67000-S31	

Channel memory for use in radio and TV sets. The four stages can be switched by touching the sensor areas. Each stage is provided with an indicator output and a tuning output. The high input sensitivity allows application in devices without power line separation. Almost any number of ICs can be interconnected.

SAS 560S: after applying V_7, stage 1 switches on.
SAS 570S: after applying V_7, no stage switches on.

Features

- High input sensitivity
- Low saturation voltage of driver outputs
- Low temperature drift of tuning outputs
- Driver outputs for filament lamps and LEDs

Maximum ratings

Supply voltage 1	V_7	36	V
Supply voltage 2	V_8	26.5	V
Voltage	V_2	6	V
Driver current	I_9, I_{11}, I_{13}, I_{15}	55	mA
Max. driver current, $t_{max.} \leqq 2$ s	I_9, I_{11}, I_{13}, $I_{15\,max.}$	100	mA
Tuning current	I_3, I_4, I_5, I_6	1.5	mA
Max. tuning current, $t_{max.} \leqq 2$ s	I_3, I_4, I_5, $I_{6\,max.}$	10	mA
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	90	K/W

Operating range

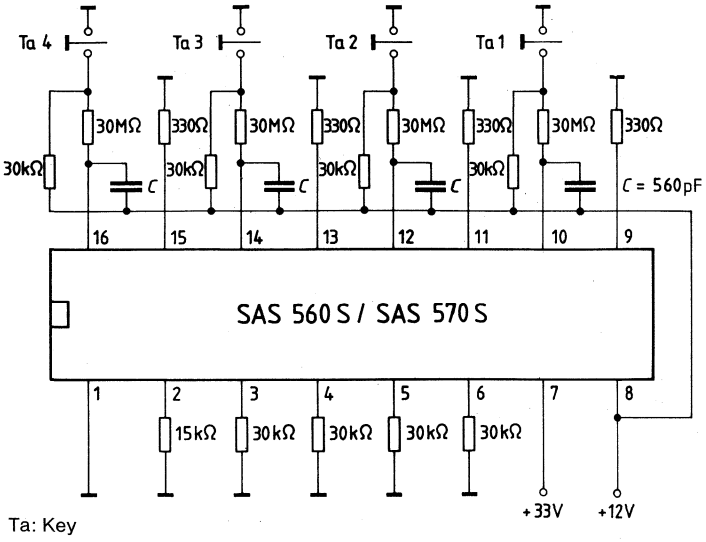
Supply voltage 1 range	V_7	11 to 35	V
Supply voltage 2 range	V_8	5 to 25	V
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics (with reference to test circuit, $V_7 = 33$ V, $V_8 = 12$ V, $T_{amb} = 25°C$)

		min	typ	max	
Voltage at pin 2 ($R_C = 15$ kΩ)					
during touching	V_{2-1}	4.2	4.7	5.5	V
after touching	V_{2-1}	2.6	3.2	3.7	V
Saturation voltage of driver outputs	V_{15-8}, V_{13-8},		0.9	1.5	V
	V_{11-8}, V_{9-8}		0.9	1.5	V
Saturation voltage of tuning voltage outputs	V_{3-7}, V_{4-7}, V_{5-7}, V_{6-7}		0.15	0.5	V
Temperature drift of saturation voltage of tuning outputs ($T_{amb} = 25$ to 55 °C)	V_{3-7}, V_{4-7}, V_{5-7}, V_{6-7}		0.3	1	mV/deg.
Current consumption					
during touching	I_7	3.15	4.3	5.35	mA
after touching	I_7	3.4	4.7	5.75	mA
Current consumption (without load)	I_7	0.5	1.4	2.1	mA
Input current	I_{10}, I_{12}, I_{14}, I_{16}		100	300	nA
Reverse current of driver outputs	I_9, I_{11}, I_{13}, I_{15}			10	µA
Reverse current of tuning voltage outputs	I_3, I_4, I_5, I_6			1	µA

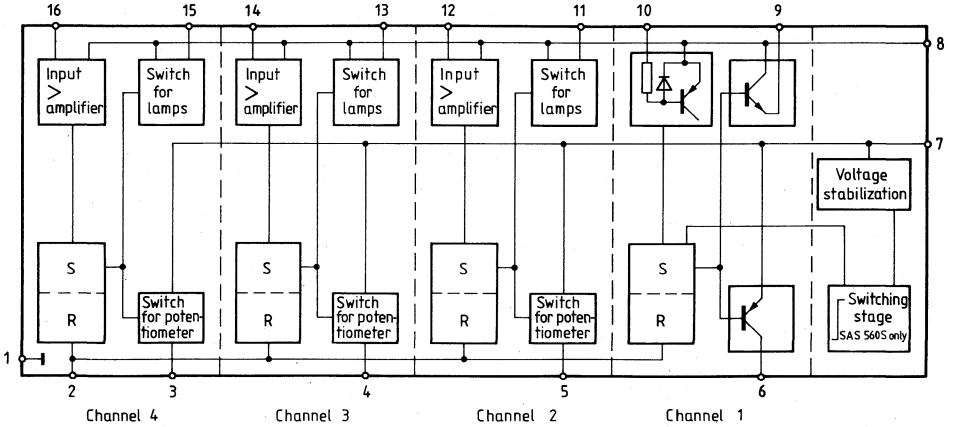
After simultaneous selection of more than one channel, only **one** channel will be selected. This also applies when several ICs are interconnected. After switching off V_8, the last selected channel is stored as long as V_7 supply is maintained.

Test circuit

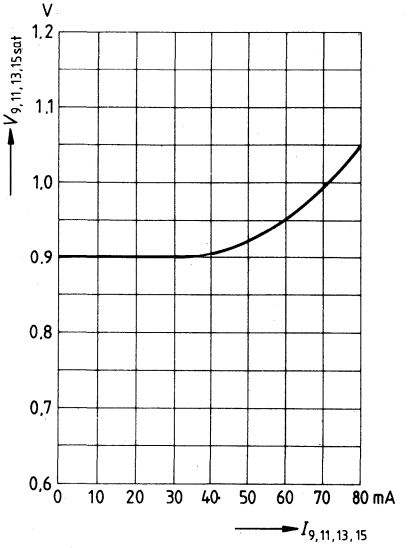


Ta: Key

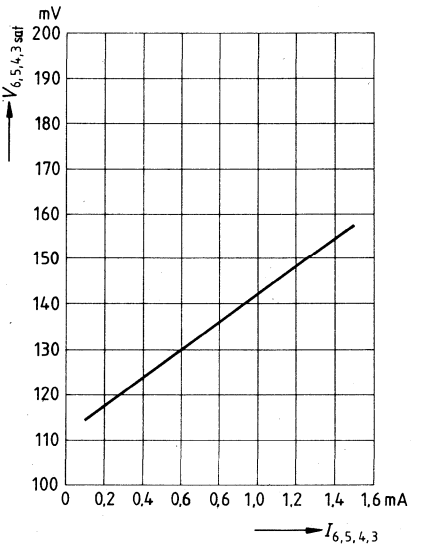
Block diagram



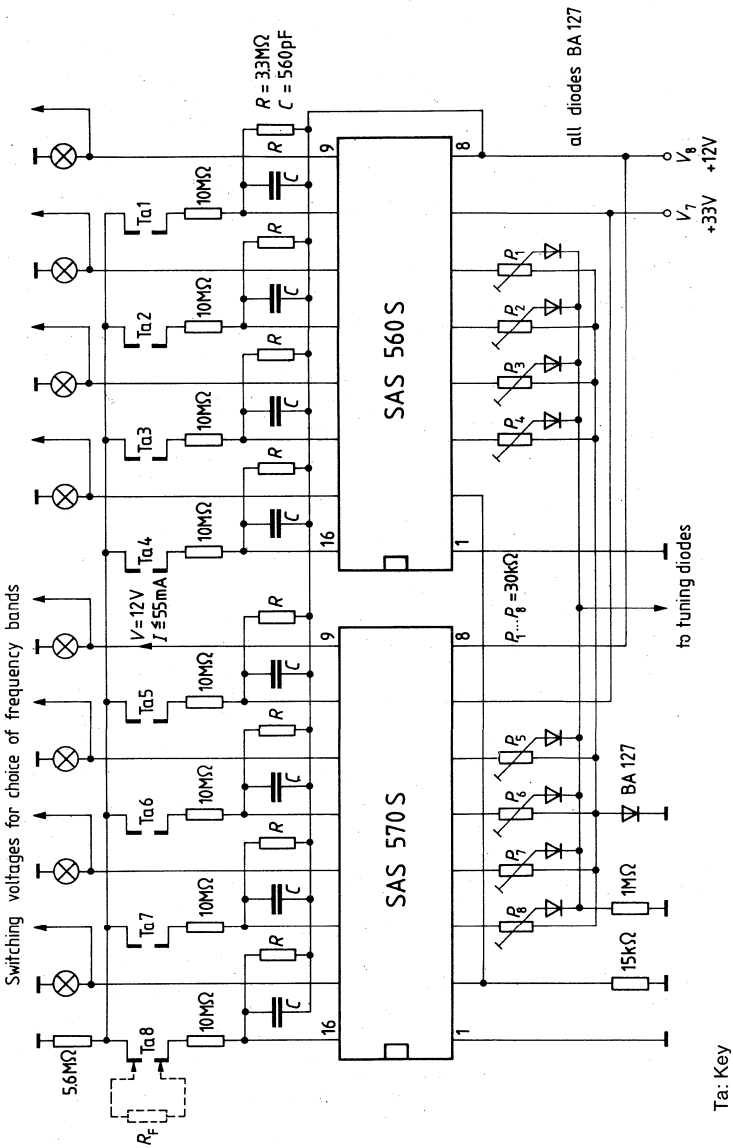
Saturation voltage of driver outputs versus current of these outputs



Saturation voltage of tuning voltage outputs versus current of these outputs



Application circuit



Bipolar circuit

Type	Ordering code	Package outline
SAS 580	Q 67000-S28	DIP 18
SAS 590	Q 67000-S29	

Channel memory for use in radio and TV sets. The four stages can be selected by touching the sensor area. Each stage is provided with an indicator output. The tuning voltage is applied to a common output. SAS 580 is the basic component for the first 4 channels. By adding almost any number of SAS 590, the number of channels can be extended by 4 channels, each.

Features

- High input sensitivity
- Low saturation voltage of the driver outputs
- Low temperature drift of the tuning switches
- Driver outputs to control filament lamps, LEDs, neon lamps, or nixie tubes
- Standby operation possible
- Ring counter up to 10 kHz
- No external diode matrix
- Single power supply

Maximum ratings

Supply voltage (without series resistor)	V_{16}	36	V
Current consumption (for operation with higher voltage, a series resistor is required)	I_{16}	15	mA
Driver current	I_3, I_5, I_7, I_9	55	mA
Max. driver current, $t_{max.} \leqq 2$ s	I_3, I_5, I_7, $I_{9\,max.}$	100	mA
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	90	K/W

Operating range

Supply voltage 1 range	V_{16}	10 to 36	V
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics (with reference to test circuit, $V_{16} = 30$ V, $T_{amb} = 25$ °C)

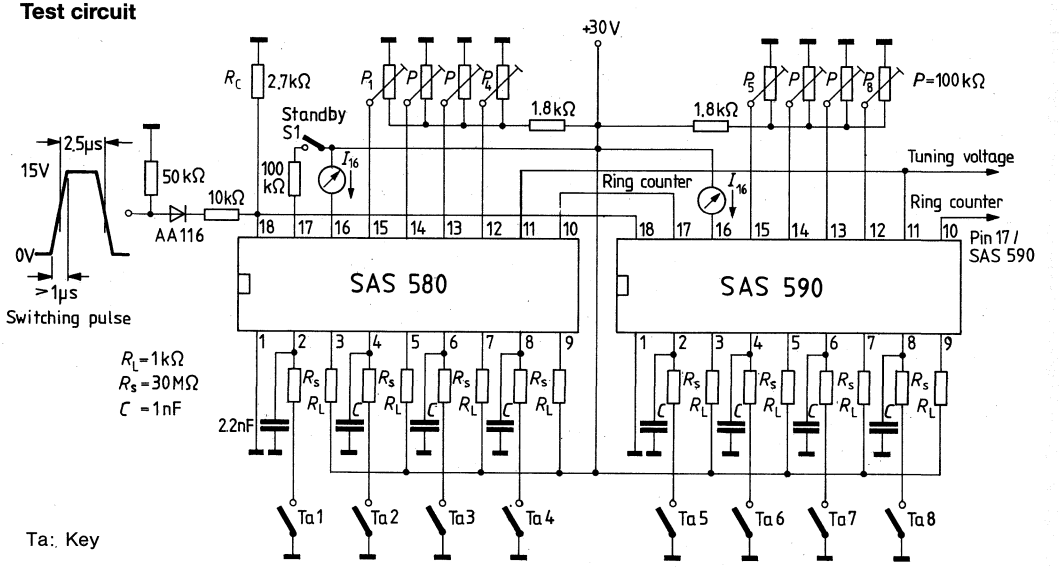
		min	typ	max	
Internal current consumption					
channel switched	I_{16}	4.5	7	9.5	mA
channel not switched	I_{16}	2.9	5	8.5	mA
Voltage at pin 18					
during touching	$V_{18\,s}$	3.25	3.7	4.2	V
after touching	$V_{18\,h}$	2.6	2.9	3.2	V
Saturation voltage of driver outputs					
$R_L = 1$ kΩ	V_3, V_5, V_7, V_9		0.8	1.5	V
$R_L = 30$ kΩ	V_3, V_5, V_7, V_9		30	60	mV
Reverse voltage of driver outputs					
$I_{rev} = 100$ µA	V_3, V_5, V_7, V_9	60			V
$I_{rev} = 5$ µA	V_3, V_5, V_7, V_9	50			V
Tuning voltage	$V_{12}, V_{13}, V_{14}, V_{15}$	0.3		$V_{16} - 2$	V
Input current of tuning voltage inputs	$I_{12}, I_{13}, I_{14}, I_{15}$		150	300	nA
Offset voltage tuning switches[1]	$V_{12\text{-}11}, V_{13\text{-}11}$			±100	mV
	$V_{14\text{-}11}, V_{15\text{-}11}$			±100	mV
Temperature drift of tuning voltage switches ($T_{amb} = 20$ to 50 °C)[1]	V_T			5	mV
Resistance of tuning output ($I_{11} < \pm 30$ µA)	$R_{q\,11}$		3		kΩ
Input current for channel switching amplifiers	I_2, I_4, I_6, I_8	20	80	200	nA
Input threshold voltage of switching amplifiers ($I_2, I_4, I_6, I_8 = 80$ nA)	V_2, V_4, V_6, V_8		5.5		V
Switching frequency of ring counter	f_{rc}		10		kHz
Reset to channel 1					
Switching pulse level	$V_{SI\,18}$		15		V
Switching pulse duration	$T_{SI\,18}$	70			µs
Switching pulse rise time	$t_{SI\,LH\,18}$			1	µs
Switching to the next stage					
Switching pulse level	$V_{SI\,18}$		15		V
Switching pulse duration	$T_{SI\,18}$		2.5		µs
Switching pulse rise time	$t_{SI\,LH\,18}$			1	µs

Characteristics of the Z diode

Z voltage ($I_{16\,(30\,V)} + 3$ mA)	V_Z	34		39	V

[1] measured between connected input and pin 11.

Test circuit



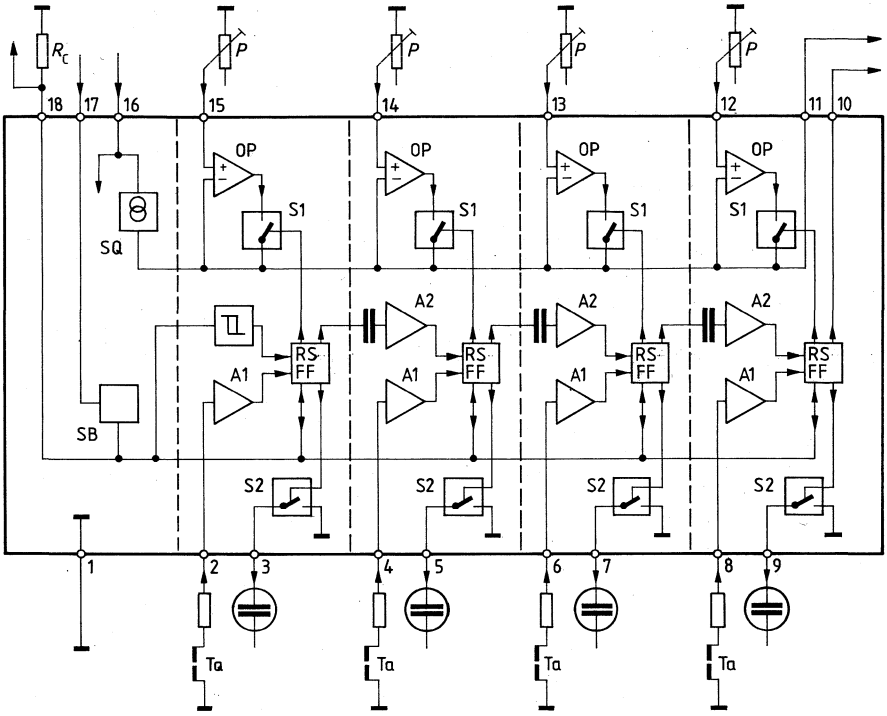
SAS 580 is absolutely necessary for testing SAS 590;
otherwise no function
SAS 580 can be tested individually.

During channel changes, the capacitor operating as a load on pin 11 is reversely charged with a current of approx. ±50 µA.

SAS 580 only: After applying supply voltage V_{16}, channel 1 is selected, i.e. the tuning voltage is switched from pin 15 to pin 11 and the lamp at pin 3 is switched on.

V_{17} < 0.5 V means standby operation, i.e. even when selecting another channel, the previously selected channel remains stored. Selection of a new channel is not possible. A stored channel must be present again after closing S1.

Block diagram SAS 580



SQ: Current source
SB: Standby
OP: Operational amplifiers
Ta: key

Figure 1

Circuit diagram: one channel

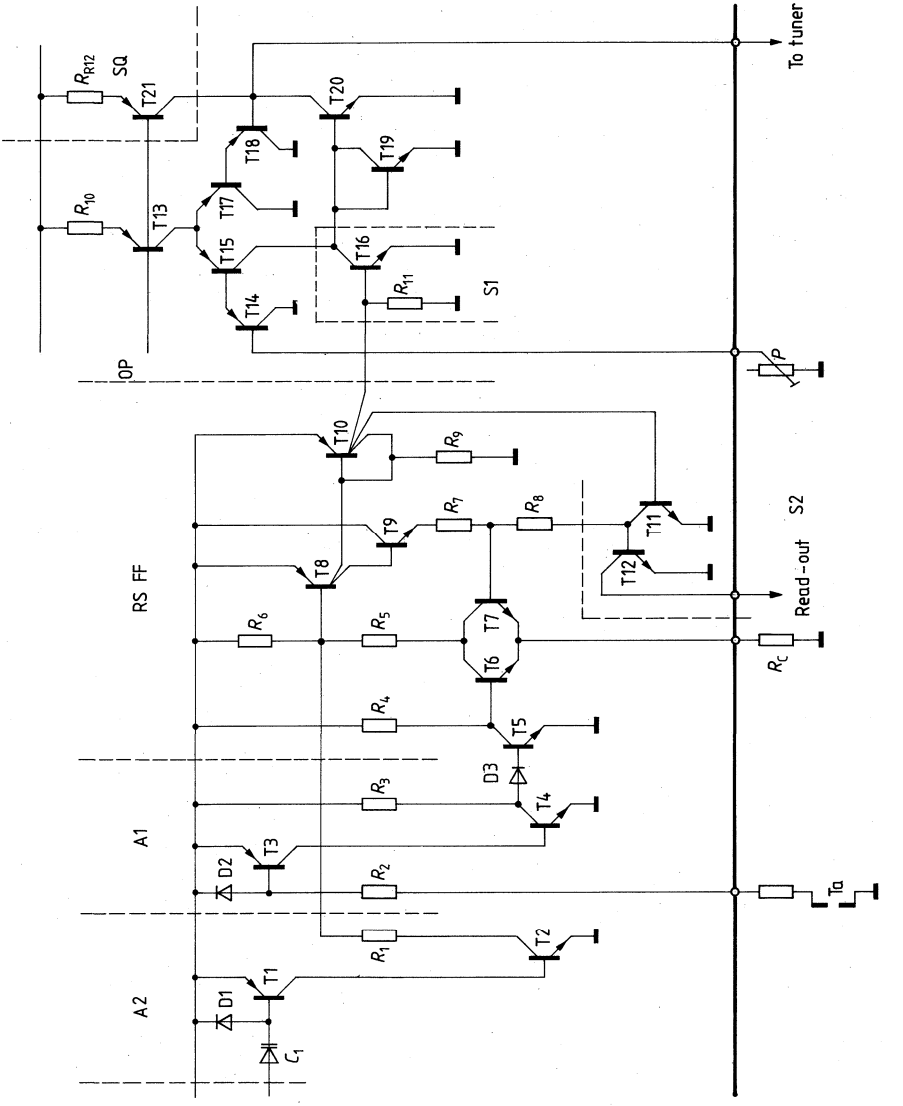


Figure 2

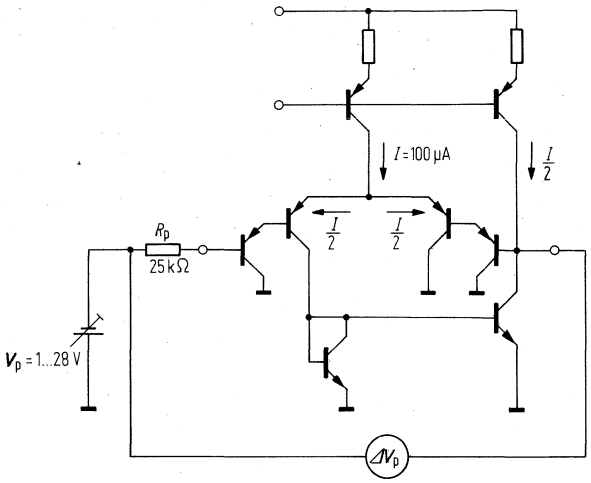


Figure 3

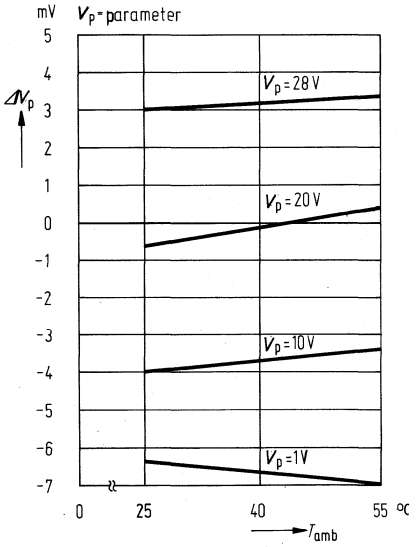


Figure 4

Application circuit 1

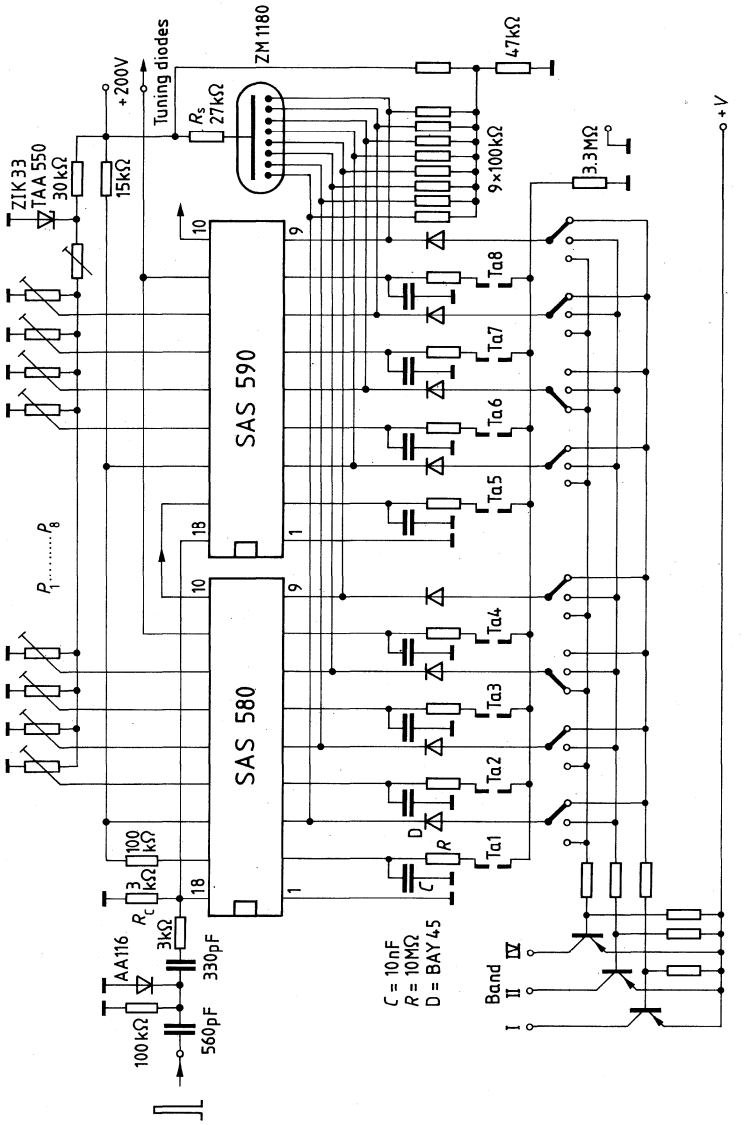


Figure 5

Application circuit 2

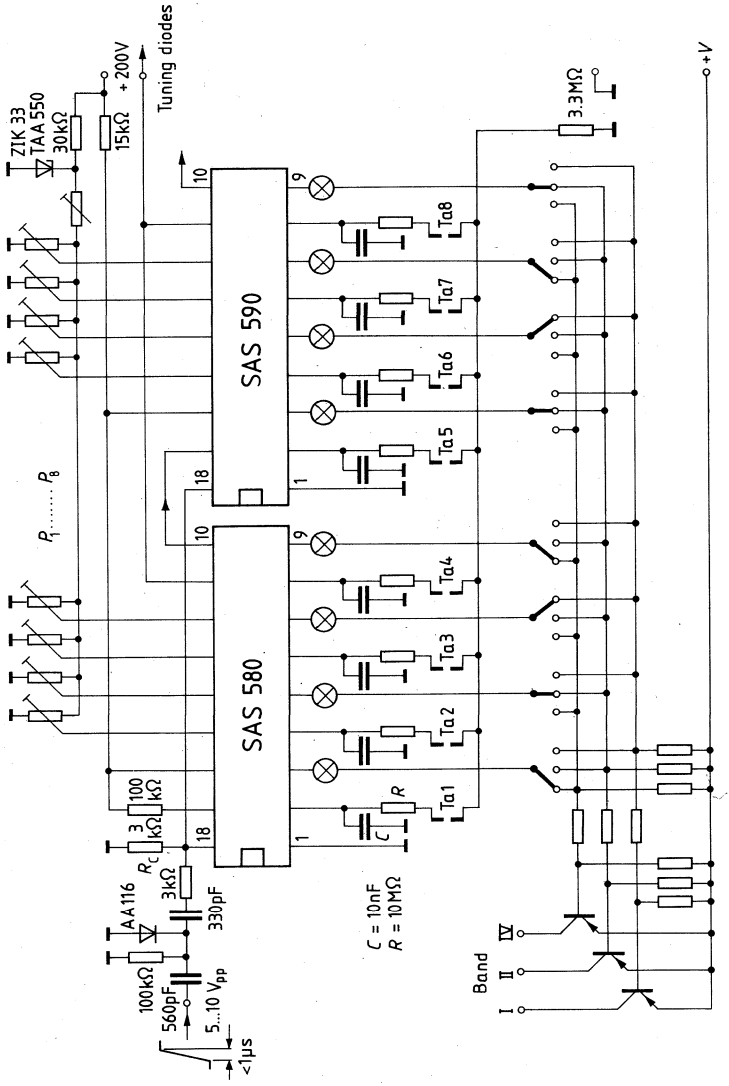


Figure 6

MOS circuit

Type	Ordering code	Package outline
SDA 2005	Q67100-Y502	DIP 18

The integrated circuit SDA 2005 is intended to display the channel and program number on the screen of TV receivers. The digits can be displayed at the top right and at the bottom right of the screen at a height of 21 frame lines.

Maximum ratings (all voltages referred to $V_{SS} = 0$ V)

Supply voltage range	V_{DD}	0 to 12	V
Input voltage range	V_i	0 to 12	V
Total power dissipation	P_{tot}	850	mW
Storage temperature range	T_{stg}	−25 to 125	°C

Operational range

Supply voltage range	V_{DD}	9 to 11	V
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics (all voltages referred to $V_{SS} = 0$ V)

		min	typ	max	
Supply current ($V_{DD} = 11$ V)	I_{18}		45	70	mA
Schmitt trigger inputs LIM, FIM					
H input voltage	$V_{iH14,17}$	5		11	V
L input voltage	$V_{iL14,17}$	0		0.8	V
Input capacitance	$C_{i14,17}$			10	pF
Input resistance	$R_{i14,17}$	1			MΩ
Inputs DATA, CLK 1, ENA 1, CLK 2, ENA 2, TCR					
H input voltage	$V_{iH12,4}$	2.4		11	V
L input voltage	$V_{iL12,4}$	0		0.8	V
Input capacitance	C_{i2-12}			10	pF
Input resistance	R_{i2-12}	1			MΩ
Overlap time	t_{D1}	2			µs
Follow-up time	t_{D2}	2			µs
CLK cycle	t_{CLK}	10			µs
Oscillator frequency OSC 1, OSC 2	$f_{15,16}$		2.4		MHz
Onscreen output EB 1 (open drain output)					
L output voltage	$I_{L13} = 3$mA	0		3	V
H leakage current	I_{H13}			10	µA

Circuit description

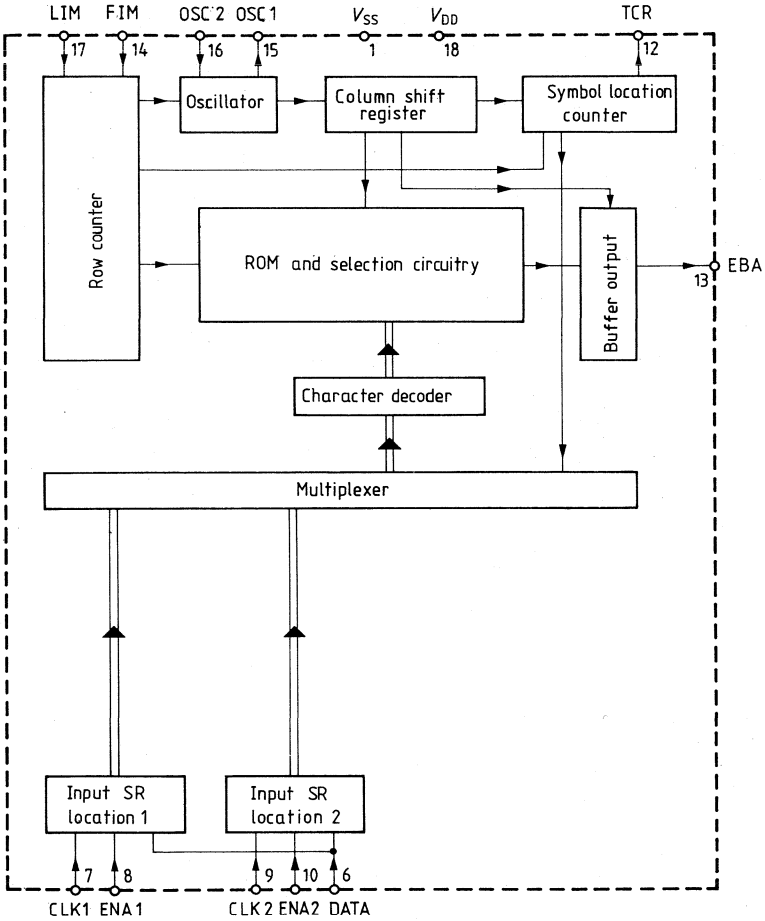
The onscreen component SDA 2005 is used to display the channel and program numbers on the screen of a TV set. It is adapted to the Siemens channel processor SDA 2003. Because of the external wiring display locations and information are freely selectable.

The onscreen IC SDA 2005 comprises 2 display locations each with 2 figures (see description of the location). The information of a digital pair is transferred via 3 lines: DATA (serial data), ENA (enable) and CLK (clock). Although a joined data connection has been provided for both display locations, each location has its own ENA and CLK connection.

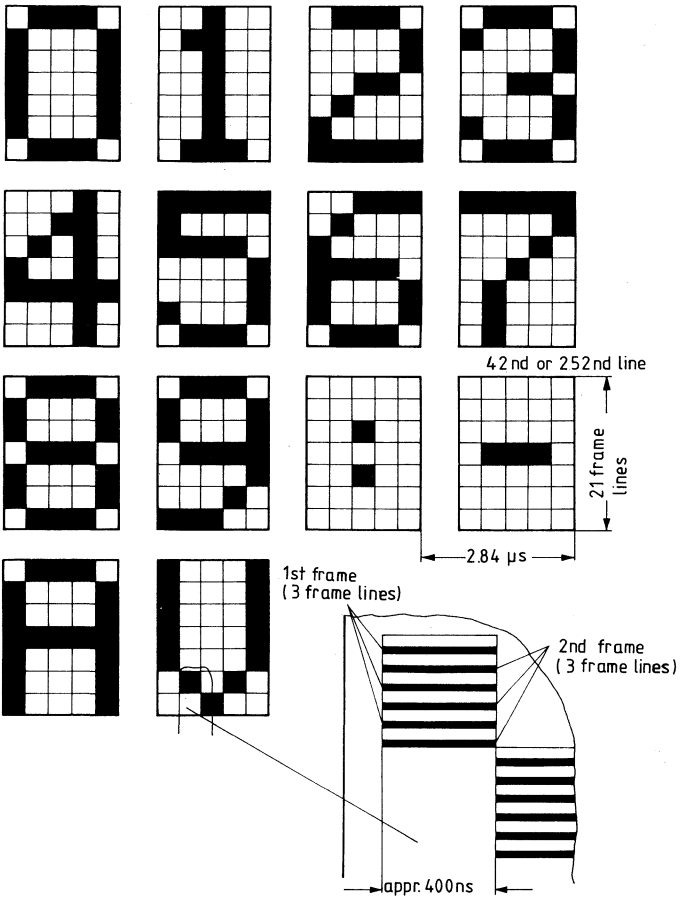
If a display location is not used, these connections are switched to LOW. To display a program or channel number, the connections ENA and CLK must be connected with the corresponding outputs of the channel processor. Example of the coordination of information: If the channel number should be displayed at the bottom right of the screen, the connections ENA1 (SDA 2005) with EG (SDA 2003) and CLK1 (SDA 2005) with CPR (SDA 2003) have to be realized. In this manner the display information channel and program number can be coordinated with any display locations.

The onscreen component SDA 2005 contains an input TCR for suppressing the display on the screen (high = display suppressed) and consequently influencing the display duration of the program or channel number.

Block diagram

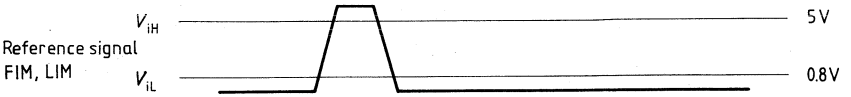


Character set

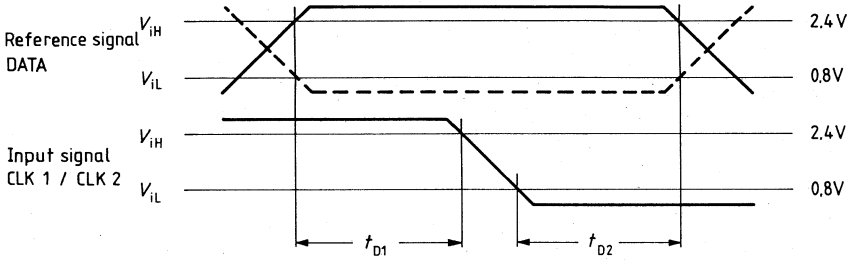


Time diagrams

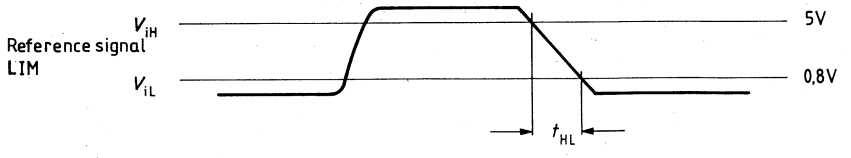
Input signals FIM, LIM



Input signals ENA 1, ENA 2, CLK 1, CLK 2, DATA, TCR

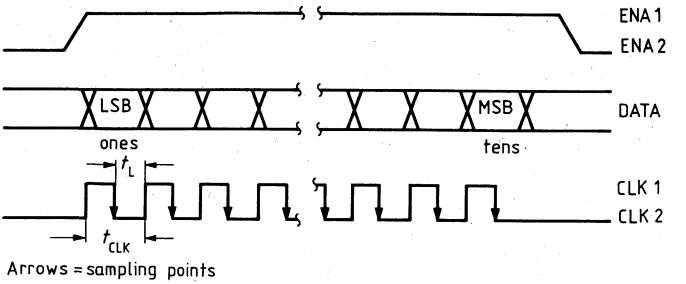


Oncreen output EBA



t_{HL}: tolerance for onscreen output
Low signal at output EBA ≙ onscreening

Data transmission with DATA

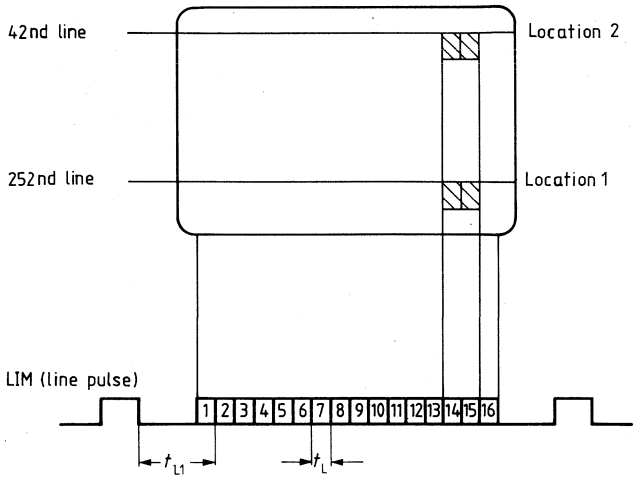


Data channel processor

MSB	LSB	Display
L L L	L	0
L L L	H	1
L L H	L	2
L L H	H	3
L H L	L	4
L H L	H	5
L H H	L	6
L H H	H	7
H L L	L	8
H L L	H	9
H L H	L	:
H L H	H	blank
H H L	L	V
H H L	H	A
H H H	L	—
H H H	H	blank

As long as "Enable" is high, there is no display. If the "Enable" was temporarily high, but without any clock pulses during this time, then the previous contents are displayed. Only data and clock pulses during "Enable" high are considered. After switching on, "blank" is displayed at all display locations.

Localization of the onscreening on the screen



$t_L = 2.81\ \mu s$ (at a dot frequency $f = 2.47$ MHz)
$t_{L1} = 2t_L + t_A$ (t_A approx. 1 µs quiet-up period of the dot oscillator; external dimensioning!)

* 1st line = 1st LIM pulse after H/L slope of FIM

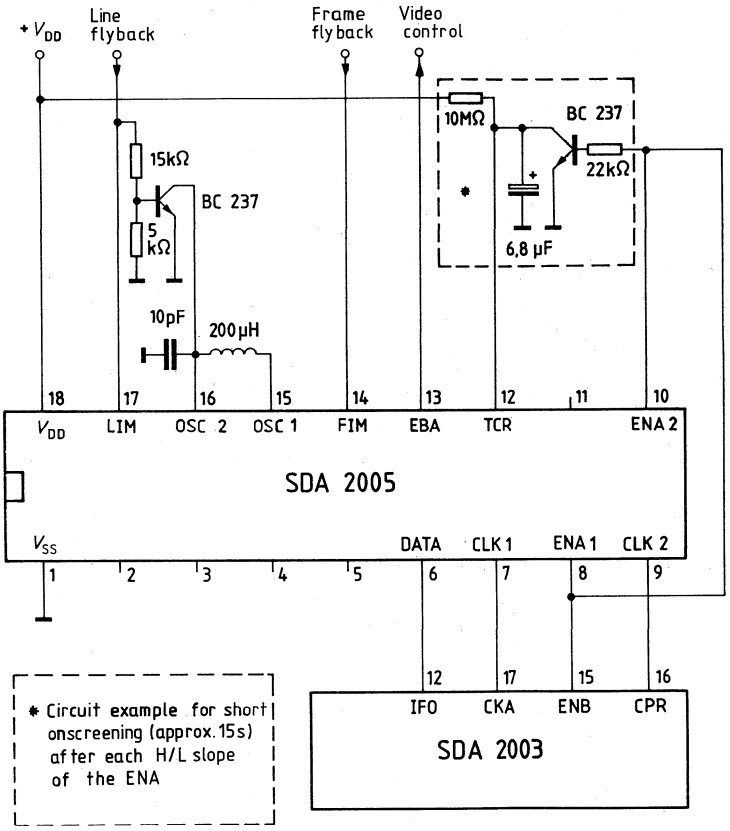
Enable	Clock	Data	Onscreen activation	Onscreen location	Symbol location
ENA 1	CLK 1	DATA	TCR = low	1	14, 15
ENA 2	CLK 2	DATA	TCR = low	2	14, 15
			if TCR = high no onscreening		

Pin configuration

Pin No.	Symbol	Function
1	V_{SS}	− supply voltage
2	N.C.	N.C.
3	N.C.	N.C.
4	N.C.	N.C.
5	N.C.	N.C.
6	DATA	Data
7	CLK 1	Clock 1
8	ENA 1	Enable 1
9	CLK 2	Clock 2
10	ENA 2	Enable 2
11	N.C.	N.C.
12	TCR	Time constant right
13	EBA	Onscreen output
14	FIM	Frame flyback pulse
15	OSC 1	Oscillator connection 1
16	OSC 2	Oscillator connection 2
17	LIM	Line flyback pulse
18	V_{DD}	+ supply voltage

Application circuit

For the display of program and channel number when used in the SDA 200 frequency synthesis system with processor SDA 2003.



MOS circuit

Type	Ordering code	Package outline
SDA 2006	Q67100-Q264	DIP 18

Features

- Nonvolatile memory of electrical, word-organized reprogrammability, in n channel floating gate technology
- 512-bit storage capacity (32 words of 16 bits, each)
- Serial word address, chip select, and instruction input via an 8-bit or 12-bit control word (switchable by means of external components)
- Erase and write duration determined with the aid of chip-internal control
- Signal outputs with open-drain stages
  active signal inputs and outputs can be inverted by terminal wiring
- Number of reprogrammings $> 10^4$
- Unlimited number of read-out procedures without refresh
- Min. 10 years storage time

Maximum ratings

Supply voltage	$V_{DD\ 2\text{-}1}$	22	V
Supply voltage	$V_{PI\ 18\text{-}1}$	22	V
Supply voltage	$V_{PP\ 3\text{-}1}$	41	V
Input voltage	$V_{i\text{-}17}$	16	V
Total power dissipation	P_{tot}	400	mW
Storage temperatur range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\ SA}$	90	K/W

Operating range (referred to $V_{SS} = 0$ V)

Supply voltage range	$V_{DD\ 2}$	14 to 16	V
Ambient temperature range	T_{amb}	0 to 70	°C

Static characteristics (all voltages are referred to $V_{SS} = 0$ V)

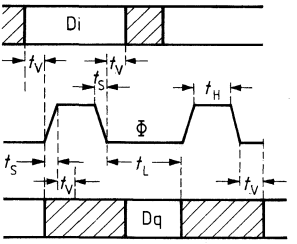
		min	typ	max	
Supply current	I_{DD2}		10	20	mA
Substrate bias	$-V_{BB1}$	4		6	V
Substrate current					
Substrate current, average current	$-I_{BB1a}$*)		0.5	2	mA
Substrate current, peak pulse current	$-I_{BB1p}$*)			10	mA
Programming voltage	V_{PP3}*)		33	35	V
Programming current, quiescent current	I_{PP3}		0.1		mA
Programming current, average current	I_{PP3a}		2	5	mA
Programming current, peak pulse current	I_{PP3p}		5	10	mA
Write voltage	V_{PI18}*)		15	16	V
Write current, quiescent current	I_{PI18}		0.1		mA
Write current, average current	I_{PI18a}		5	20	mA
Write current, peak pulse current	I_{PI18p}		15	50	mA
Inputs					
Di	$V_{L8,12,16}$	0		0.5	V
$\Phi/\overline{\Phi}$	$V_{H8,12,16}$	4		V_{DD}	V
REC/$\overline{\text{REC}}$	$I_{H8,12,16}$			10	µA
($V_H = V_{DD}$)					
STWL					
($-I_L = 100$ µA, pull-up resistors)	$V_{L4,15,9,11,10}$	0		0.5	V
INV	$V_{H4,15,9,11,10}$	4		V_{DD}	V
CS3	$I_{H4,15,9,11,10}$			10	µA
CS1, CS2					
(with a control word of 12 bits only; $V_H = V_{DD}$)	$I_{H4,15,9,11,10}$			10	µA
($V_L = 0$ V; $V_H = V_{DD}$)	$I_{L4,15,9,11,10}$			300	µA
$\overline{\text{RES}}$	V_{L6}	0		0.5	V
	V_{H6}	4		V_{DD}	V
($V_L = 0$ V)	$-I_L$			200	µA
($V_H = V_{DD}$)	I_H			200	µA
Outputs					
Dq/$\overline{\text{D}_q}$, $\overline{\text{L}}$/L	$V_{L14,13}$			0.5	V
($I_L = 1$ mA; open-drain stages)					
($V_H = V_{DD}$)	$I_{H14,13}$			10	µA

* only necessary during programming

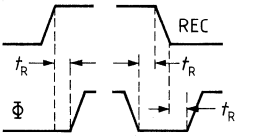
Dynamic characteristics

		min	typ	max	
Data bus					
Φ – clock	t_H	5			µs
INV on low	$-t_L$	10			µs
Φ – clock	t_H	10			µs
INV on high	t_L	5			µs
	t_V	5			µs
	t_S			2	µs
Signal edge distance	t_R	5			µs
INV on low or high					
Programming duration	t_{prog}		0.1	1	s
(V_{PP} = 33 V, V_{PI} = 15 V)					
Programming frequency	f_{prog}			1	Hz

INV on low



Signal edge distance



Circuit description

Data transfer

Data transfer with the SDA 2006 is performed serially via a 5-line bus, consisting of:

- Data input Di
- Data output Dq/$\overline{\text{Dq}}$
- Data input signal REC/$\overline{\text{REC}}$ (receive data)
- Clock input $\Phi/\overline{\Phi}$
- Programming output signal $\overline{\text{L}}$/L (load)

The active input or output levels, respectively, may be inverted via the input INV. They are switchable, as a group, in order to facilitate adaptation to different external circuits.

Terminal	Potential		Notes
INV	low (V_{SS})	high (V_{DD})	
Di/$\overline{\text{Dq}}$	Di = Dq	Di = $\overline{\text{Dq}}$	
REC/$\overline{\text{REC}}$	high	low	During data input
$\Phi/\overline{\Phi}$	high	low	Active shift pulse
$\overline{\text{L}}$/L	low	high	In the case of reprogramming

Chip control

The control information is entered via data input Di in the form of a control word, the length of which may be set via input STWL:

Terminal STWL	low	high (open or V_{DD})
Control word length	8 bits	12 bits

The control words contain information with respect to word address, chip address, and instruction, and have the following formats (A0 as LSB at first):

8-bit control word	A0 A1 A2 A3 A4 B1 B2 C3
12-bit control word	A0 A1 A2 A3 B0 B1 B2 B3 A4 C1 C2 C3

with A0.....A4 Word address bits
B0.....B3 Instruction bits
C1.....C3 Chip select bits

Instruction coding

12-bit control word				
B0	B1	B2	B3	Instruction
low	high	high	high	Read out, D9 as LSB
low	low	high	high	Read out, D1 as LSB
low	low	low	high	Programming
	8-bit control word			

Chip select

An instruction is only decoded in a memory, if the information of the chip select bits matches that of the chip select inputs.

Chip select — Terminal		Chip select — Bit	
	CS1 ◄——►	C1	
	CS2 ◄——►	C2	12-bit control word
8-bit control word	CS3 ◄——►	C3	

CS1 and CS2 remain unconnected in the case of the 8-bit control word.

Read-out (figure 1a and 1b)

Prior to the read operation of the memory the 8-bit or 12-bit control word must be serially clocked into the data input Di. 8 or 12 clock pulses, respectively, are necessary to enter the control word at the input $\Phi/\overline{\Phi}$. During input, the REC/$\overline{\text{REC}}$ input is active (active high for low at INV, active low for high at INV).

Information input is ended by means of the trailing edge of the REC/$\overline{\text{REC}}$ signal and the read-out instruction is decoded at chip select. As a result the data output Di/$\overline{\text{Dq}}$ changes into a low-ohmic state.

With the aid of a further clock pulse S, the read-out operation is initialized. The data is shifted with the trailing edge of additional clock pulses. The LSB arrives at the data output with the first of these pulses. During the read-out operation via the control word either the first data bit D1 or the ninth data bit D9 can be chosen as LSB. The read-out operation can be discontinued after any number of shift pulses. Thus, every stored 16-bit data word can also be read as two separated 8-bit data words.

Reprogramming (figure 2a and 2b)

Prior to programming, the 16-bit data word (D1 as LSB, first), then the 8-bit or 12-bit control word at the data input Di must be clocked in by means of the active REC/$\overline{\text{REC}}$ signal. The trailing edge of the REC/$\overline{\text{REC}}$ signal decodes the programming instruction at chip select. The reprogramming operation, however, only starts with the trailing edge of a further clock pulse and is forwarded to the memory controller via the $\overline{\text{L}}$/L signal.

The duration t_{prog} of the reprogramming mode is determined by chip-internal control. Independent of the external operating voltages V_{PP} and V_{PI}, erase and write operations are only completed after each memory has reached the desired state. During rewriting, the memory cannot be influenced externally, because the inputs REC/$\overline{\text{REC}}$, $\Phi/\overline{\Phi}$ and Di remain blocked. Premature termination of the operation can only be caused by zero level at the input $\overline{\text{RES}}$.

Reset function

A low level voltage at the input $\overline{\text{RES}}$ moves the memory into the reset state. A voltage divider is internally connected to the input and completes the reset state for $V_{DD} > 11$ V. In case of undefined signal and supply voltage levels during turn-on and turn-off, the input of the $\overline{\text{RES}}$ must be maintained on low during the entire turn-on and turn-off phase to avoid undesired decoding of a programming or read instruction. If the L status is not externally adjustable, it is advisable to connect the input $\overline{\text{RES}}$ (pin 6) via a 12 V Z diode to V_{DD} (pin 2) and via a 3 kΩ resistance to ground (pin 17).

Voltage supply

The SDA 2006 includes four extended voltage inputs V_{PP}, V_{PI}, V_{DD}, V_{BB} with respect to V_{SS} (ground). Normally, V_{DD} and V_{PI} are externally interconnected. The voltages V_{PP} and V_{PI} are only required during programming operations. During read out or in the quiescent state, they may also be open or grounded. The values of these voltages only influence the duration, but not the reliability of the nonvolatile storage operation. **Figure 3** shows an appropriate circuit configuration as tuning memory in TV sets.

Inverted level (input INV on high or open)

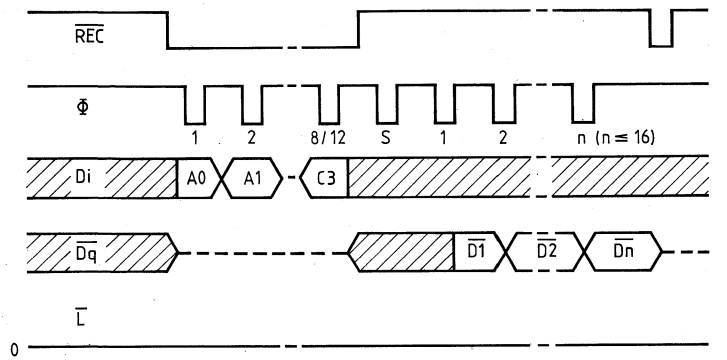


Figure 1a

Non-inverted level (input INV on low)

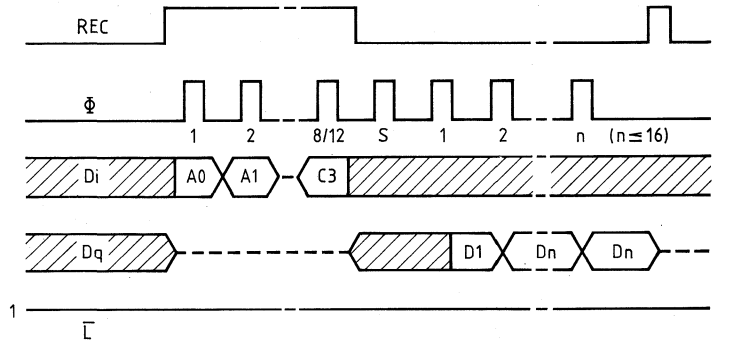


Figure 1b

Figures 1a and 1b **Read operation** (only pertinent active levels are indicated)

Inverted level (input INV on high or open)

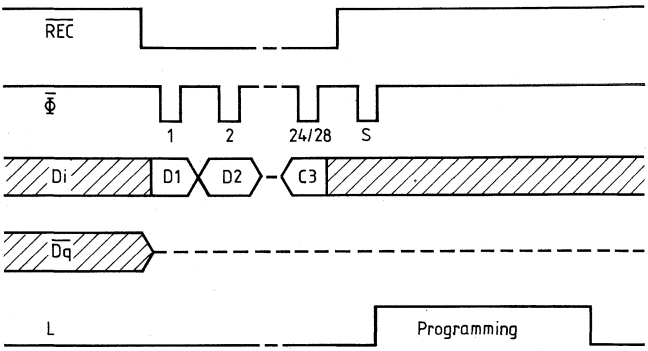


Figure 2a

Non-inverted level (input INV on low)

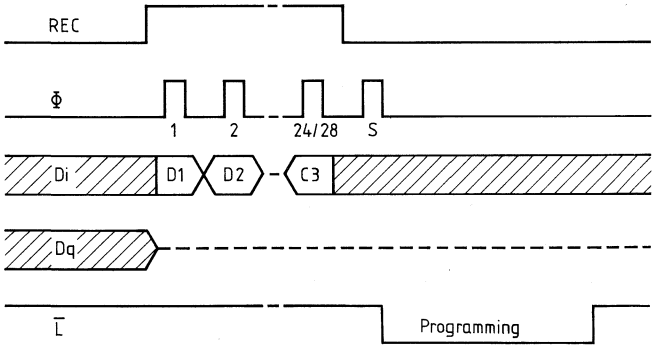


Figure 2b

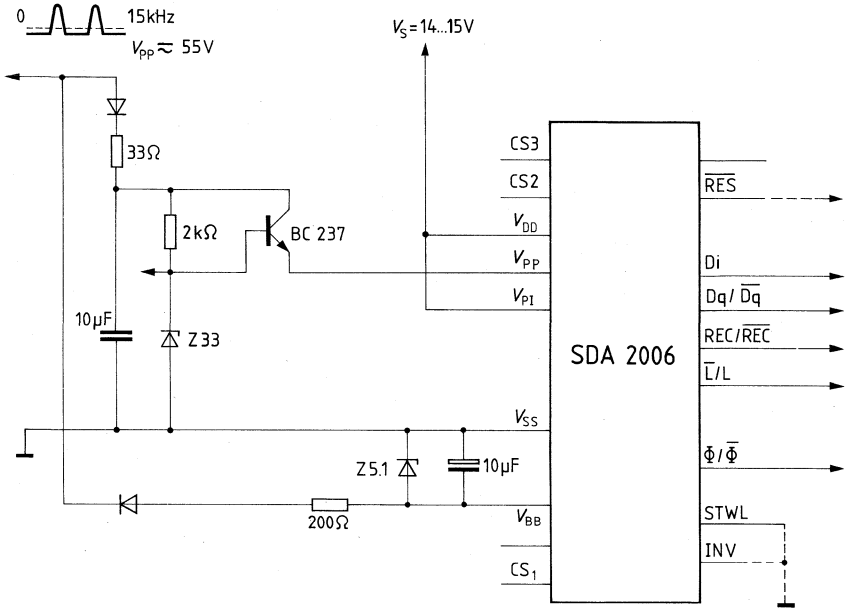
Figures 2a and 2b **Programming operation** (only pertinent active levels are indicated)

Pin configuration

Pin No.	Symbol	Function
1	V_{BB}	Substrate bias
2	V_{DD}	Supply voltage
3	V_{PP}	Programming voltage
4	STWL	Control word length 12 or 8 bits (input) (12 bits for high or open)
5		Remains open
6	$\overline{RES}$	Reset input
7		Remains open
8	Di	Data input
9	CS3	Chip select input (8-bit or 12-bit control word)
10	CS2	Chip select input (12-bit control word)
11	$\overline{CS1}$	Chip select input (12-bit control word)
12	$\Phi/\overline{\Phi}$	Clock input*
13	$\overline{L}/L$	Programming signal output (load)*
14	$Dq/\overline{Dq}$	Data output*
15	INV	Signal inverting (input)
16	$REC/\overline{REC}$	Data input control input (receive)*
17	V_{SS}	Ground
18	V_{PI}	Write voltage

*) First polarity for INV on low; second polarity for INV on high.

Figure 3: SDA 2006 as tuning memory in TV sets



MOS circuit

Type	Ordering code	Package outline
SDA 2008	Q 67100-Y 503	DIP 18

The SDA 2008 IC is a further development of the infrared transmitter IC SAB 3210. It includes a disconnectable 8-stage divider, thus enabling the oscillator to operate up to 500 kHz with a ceramic oscillator instead of an *LC* circuit.

Features

- Complete security of the keyboard against operating errors
- Instruction extension up to 60 instructions is possible by using diodes and by means of a shift key (keyboard changeover)
- Programmable start bit by external voltage
- Wide supply voltage range between 5 V and 16 V
- Low current consumption, typically 3 mA. The battery can be switched off by an external transistor
- With the aid of special contacts, ASC II transmission with 64 instructions is possible
- No external column resistors necessary

Maximum ratings (all voltages referred to $V_{DD} = 0$ V)

Supply voltage	V_{SS}	18	V
Input voltage	V_i	18	V
Power dissipation per output	P_q	100	mW
Total power dissipation	P_{tot}	500	mW
Storage temperature range	T_{stg}	−55 to 125	°C

Operating range (referred to $V_{DD} = 0$ V)

Supply voltage range	$V_{SS\,1}$	5 to 16	V
Supply voltage range[1])	$V_{SS\,1}$	5.5 to 16	V
Ambient temperature range	T_{amb}	0 to 70	°C

1) Instruction extension with diodes

Characteristics (all voltages referred to V_{DD})

		min	typ	max	
Supply current (outputs not connected)	I_6		3	7	mA
Leakage current, total current of outputs Ca, Cb, Cc, Cd, ETA, IRA (refer to test circuit)	$I_{2,3,4,5,7,8}$			1	µA
Inputs					
Oscillator input CLK I					
Operating frequency with prescaler	f_{17}	160		560	kHz
Operating frequency for external clock with disconnected prescaler	f_{17}	20		70	kHz
IRA remote control signal output					
H output voltage (refer to test circuit) $I_{qH} = 4$ mA; $V_{SS} = 6$ V	V_{qH8}	V_{SS}–5			V
H resistor with respect to V_{SS}	R_{qH8}	100			Ω
ETA switch-on transistor output					
H output current $V_{q7} = V_{SS}$–4 V	I_{qH7}	100		10,000	µA

Row input 1 to 8 (internal pull-high resistors)

Instructions can be transmitted by connecting the respective row input with the corresponding column output (refer to instruction set). Operating errors, such as connecting more than one respective row and column are recognized and transmission is interrupted. Only exception: instruction extension with row 8 (see input, keyboard).

The connection can include as max. resistance a silicon diode junction in forward direction and a 100 Ω resistance in series. Minimum resistance is zero.

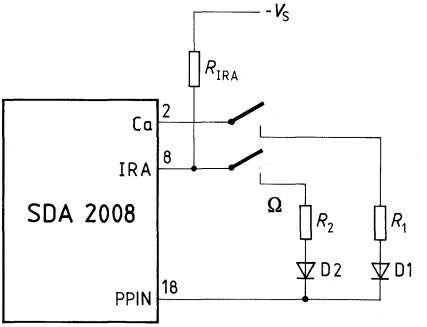
ETA input

The ETA input is connected to the supply voltage via the base-emitter diode of the NPN switching transistor for normal transmitting operations.

PPIN program input

If the PPIN input is joined with the corresponding column output or with the IRA output (in this case = 33 kΩ $\leqq R_{IRA} \leqq$ 47 kΩ) the output mode can be changed in accordance with the table "PPIN circuitry".

Example



33 kΩ $\leqq R_{IRA} \leqq$ 47 kΩ
$R_1R_2 \leqq$ 100 Ω
D1, D2 = $V_1 \leqq$ 0-8 V at I_F = 0.1 mA
and $T_{amb\ min}$

Description of function

The SDA 2008 IC operates as a transmitter for the infrared remote control system IR 60.

The PMOS circuit contains a control output for an NPN transistor which deactivates the supply voltage if the keyboard is not activated (i.e. no row is in "low" state).

Input, keyboard

The transmitter contains an input matrix of 8 rows and 4 columns. In order to input an instruction, a row must be connected to a column. Thus, the transmitter is switched on and the appropriate instruction is sent. Without further measures it is possible to issue up to 32 instructions. The instruction set can be extended up to 60 either with the aid of additional diodes (for this purpose 2 diodes are required for each 4 additional instructions) or up to 62 instructions with a shift key. In both cases the additional connection (diodes to row 8 or shift key) is necessary prior to issuing the first instruction — after that the originally allocated instruction is sent independent of the additional connection.

As a fifth matrix column, — V_S can be used to input the instructions 40 to 47 (without external diode connection using only one key, each).

Operating error

The circuit includes a security lock against multi-operations (several keys are depressed simultaneously). An exception is the double operation inside a column with one of the rows 1 to 7 and row 8, since this combination is used in order to extend the instruction set with the aid of diodes. After transmission of the first infrared instruction after the startbit, this double operation is locked as well.

Start instruction, end instruction

After the switch-on, the instruction No. 62 is issued as start instruction thus indicating to the receiver the start of the instruction transmission.

In case of an operating error, this instruction is generated by the security lock. If the key or keys are released, the selected instruction is sent once more (depending upon the exact instant of release) while the instruction No. 62 is sent once as stop before the supply voltage is switched off. Safety measures prevent to change an instruction to any other than instruction No. 62.

Output

The transmitter encodes the input in bi-phase code (refer to timing diagram). Prior to the 6 information bits, a presignal and a startbit which can be selected via PPIN, are sent. The presignal enables proper control of the preamplifier on the receiver side, whereas the startbit is used for receiver discrimination. Thus it is possible to control a TV set and a radio in one room independently of each other with the same remote control system.

The output signal is carried at 1/16 of the clock frequency ($f_{CLKI}/16$) and a pulse duty factor of 1:4. With the help of corresponding wiring of the program input PPIN, the carrier can be switched off. Thus any other external carrier can be used.

Instruction interval

The interval between two given instructions (except the start instruction) is approximately 12 times the instruction length (incl. presignal) or 35,536 CLKI clocks, respectively. This interval can be reduced to 30,976 CLKI clocks in order to obtain diminished instruction intervals at lower clock frequencies.

Operation at low clock frequency

The prescaler (divide by 8) can be switched off. Thus, operation is possible at a clock frequency of approx. 500 kHz or 62.5 kHz, as required. The prescaler can only be switched off if — at low resistance — the IRA output is not forced to low (by means of a base-emitter space), e.g. in the case of wiring for front-end control.

Operation without switching transistor

During operations with a fixed supply voltage (ETA = low), the columns a to d are periodically interrogated (H pulse) in the normal sequence (as if an instruction is emitted) in order to permit an external synchronization.

After the supply voltage began to rise at 0 V, the flow of control is brought into a definite state and starts column interrogation. After having recognized a row in the "low" state, the flow of control is reset — then the flow corresponds until disconnection with the flow present during battery operations. After transmission has ended, the flow of control continues column interrogation, however, without any further output to IRA.

Multitransmitter operation

Without great increase in external circuitry, it is possible to cascade two SDA 2008 ICs so that they can be multiplexed to give out the instructions. For this purpose, the automatic resetting of the flow control and the instruction register are utilized which become effective as soon as both columns a and b are on high.

PPIN connections

Connect with:	Function
Column a	Shift into second instruction group (bit F = "1")
Column b	Shortened instruction interval
Column c	Startbit = "0"
Column d	No carrier of the IRA signal
IRA	Bridging the prescaler

(In the case of combinations of these functions, decoupling with diodes according to figure PPIN circuitry is necessary).

ETA circuit:

ETA = V_{DD}	Operation at constant supply voltage. If no row is set to "low", IRA is without output, however permanent column interrogation.
ETA to base of the voltage commutation transistor	Normal battery operation including disconnection of the supply voltage after the end instruction at open row combination.

Instruction set

No diodes at row 8
unshifted

Instr. No.	Code FED	CBA	Key
0	000	000	1a
1	000	001	1b
2	000	010	1c
3	000	011	1d
4	000	100	2a
5	000	101	2b
6	000	110	2c
7	000	111	2d
8	001	000	3a
9	001	001	3b
10	001	010	3c
11	001	011	3d
12	001	100	4a
13	001	101	4b
14	001	110	4c
15	001	111	4d
16	010	000	5a
17	010	001	5b
18	010	010	5c
19	010	011	5d
20	010	100	6a
21	010	101	6b
22	010	110	6c
23	010	111	6d
24	011	000	7a
25	011	001	7b
26	011	010	7c
27	011	011	7d
28	011	100	8a
29	011	101	8b
30	011	110	8c
31	011	111	8d

No diodes at row 8
shifted

Instr. No.	Code FED	CBA
32	100	000
33	100	001
34	100	010
35	100	011
36	100	100
37	100	101
38	100	110
39	100	111
40	101	000
41	101	001
42	101	010
43	101	011
44	101	100
45	101	101
46	101	110
47	101	111
48	110	000
49	110	001
50	110	010
51	110	011
52	110	100
53	110	101
54	110	110
55	110	111
56	111	000
57	111	001
58	111	010
59	111	011
60	111	100
61	111	101
62	111	110 } end instructions
62	111	110 }

With diodes at row 8
unshifted/shifted

Instr. No.	Code FED	CBA	Key
32	100	000	81a
33	100	001	81b
34	100	010	81c
35	100	011	81d
36	100	100	82a
37	100	101	82b
38	100	110	82c
39	100	111	82d
40	101	000	83a
41	101	001	83b
42	101	010	83c
43	101	011	83d
44	101	100	84a
45	101	101	84b
46	101	110	84c
47	101	111	84d
48	110	000	85a
49	110	001	85b
50	110	010	85c
51	110	011	85d
52	110	100	86a
53	110	101	86b
54	110	110	86c
55	110	111	86d
56	111	000	87a
57	111	001	87b
58	111	010	87c
59	111	011	87d

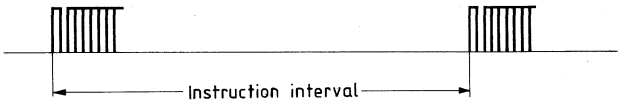
Special group
unshifted/shifted

Instr. No.	Code FED	CBA	Key
40	101	000	1L
41	101	001	2L
42	101	010	3L
43	101	011	4L
44	101	100	5L
45	101	101	6L
46	101	110	7L
47	101	111	8L

Instruction interval (prescaler switched on)

Interval	Interval in CLKI clocks	Interval in ms $f_{CLKI} = 500$ kHz	PPIN connected to column b
Normal	65536	approx. 131	———
Reduced	30976	approx. 62	X

Definition of the instruction interval



Hints for special functions

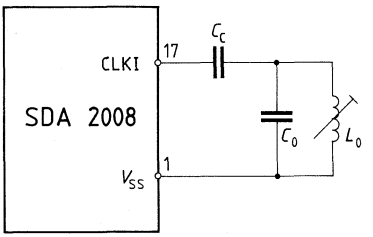
	IR remote control TV/radio sets	Front-end operation TV/radio sets	Transmission via AF cable	Remote control for model rail way	Typewriter keyboard	Time programmable remote control	TV games	Light switch remote control
Start bit changeover	X	X	X	X	X	X	X	
Shift into second group	X	X	X	X		X	X	
Diode matrix	X	X	X	X	X	X	X	
Special instruction group	X	X	X	X	X	X	X	
No carrier		X	X		X			
Bridged prescaler		X						
Shortened instruction interval			X	X				
No debounce delay								X
Special connection			X		X	X		

Pin configuration

Pin No.	Function
1	V_{SS}, +supply voltage
2	Column a
3	Column b
4	Column c
5	Column d
6	V_{DD}, −supply voltage
7	ETA (switch-on transistor output)
8	IRA (infrared output)
9	Row 1
10	Row 2
11	Row 3
12	Row 4
13	Row 5
14	Row 6
15	Row 7
16	Row 8
17	CLKI (oscillator input)
18	PPIN (programming input)

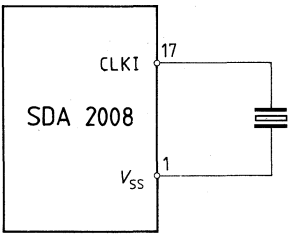
Oscillator connection

1)

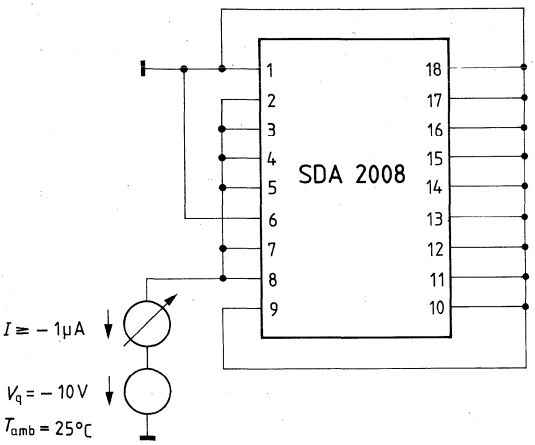


$C_C \geq 10\,nF \quad f_{CLKI} \approx \frac{1}{2\pi\sqrt{L_0 C_0}}$

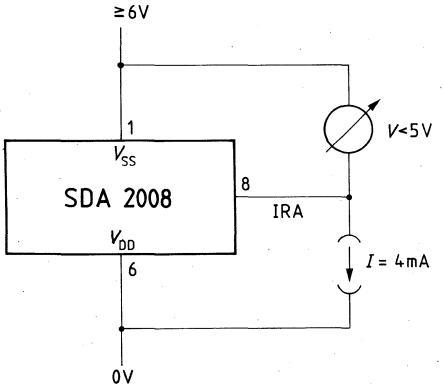
2)



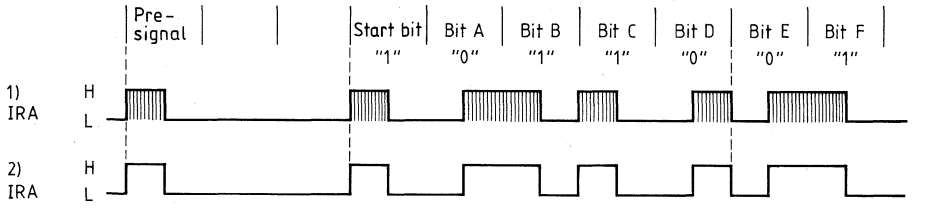
Leakage current, total current (test circuit)



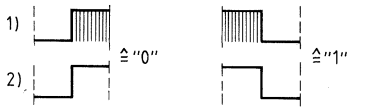
IRA remote control signal output (test circuit)



Biphase coding from instruction 011001

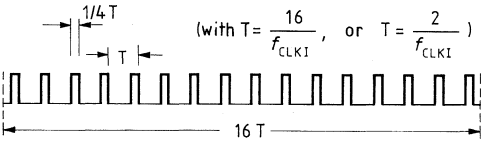


Def: for "0" and "1"

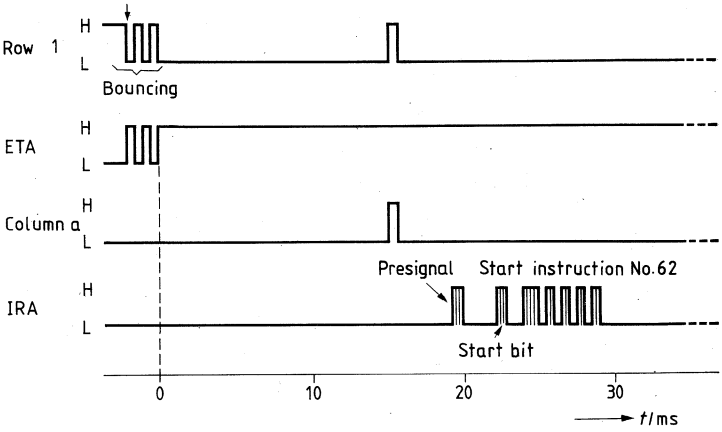


1) with carrier
2) without carrier

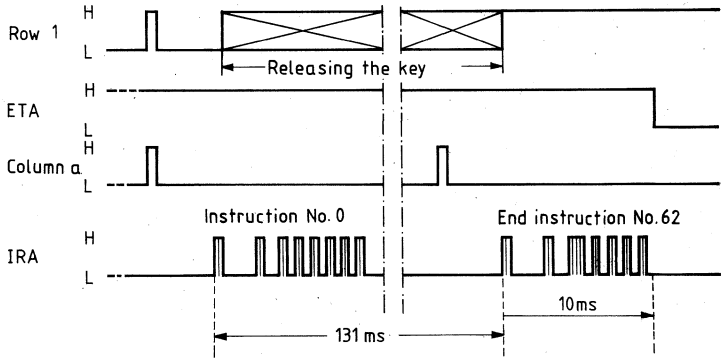
Exact pulse train of a burst for 1):



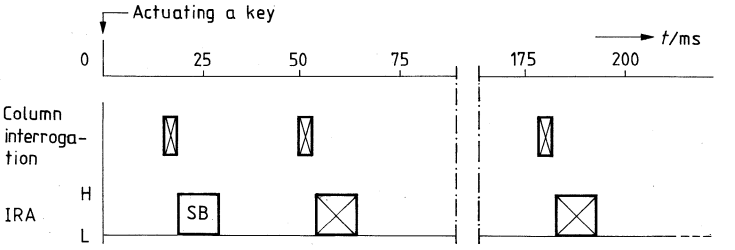
Actuating a key (e.g. 1a), f_{CLKI} = 500 kHz



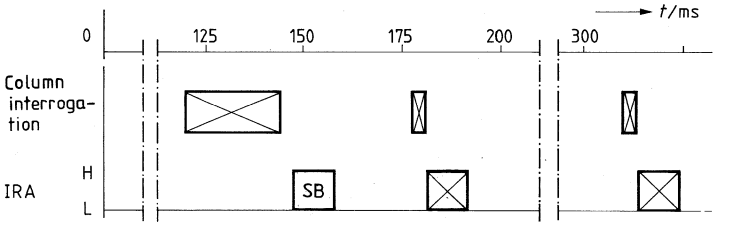
Releasing a key (1a), f_{CLKI} = 500 kHz



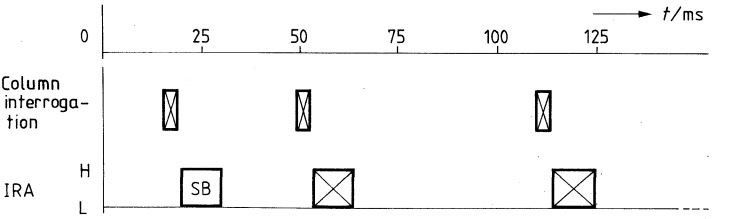
Instruction interval, f_{CLKI} = 500 kHz



PPIN at IRA (bridged prescaler) f_{CLKI} = 62.5 kHz

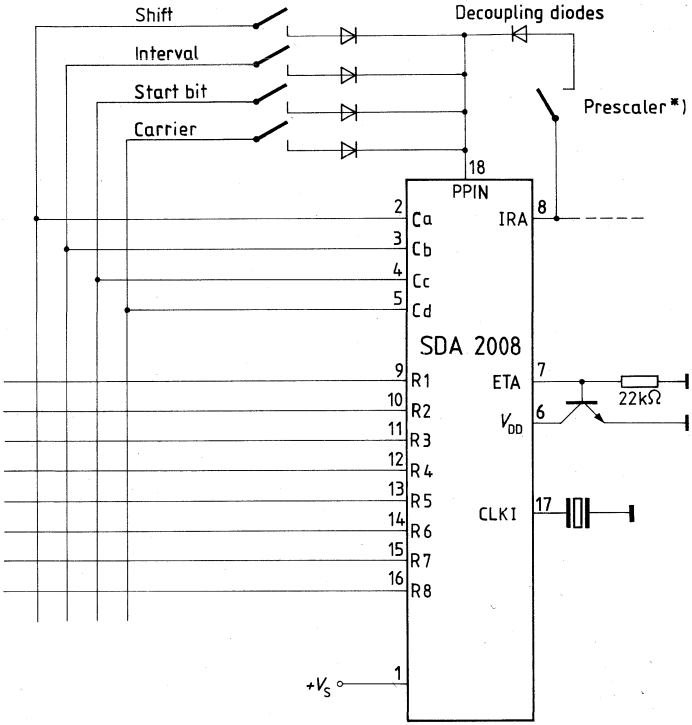


PPIN at column b (shortened instruction interval) f_{CLKI} = 500 kHz



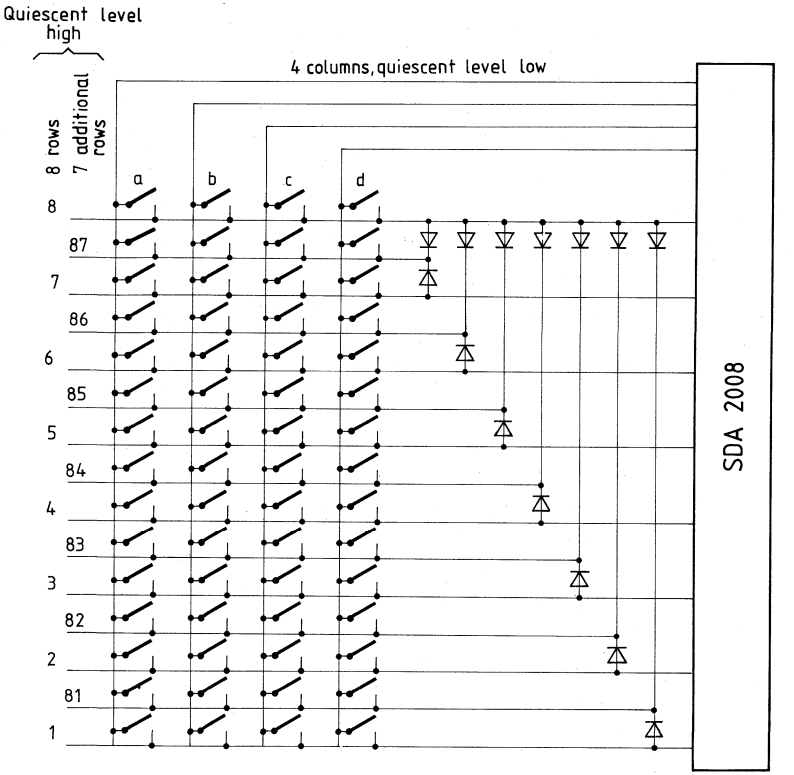
SB:= Instruction No. 62

PPIN connection

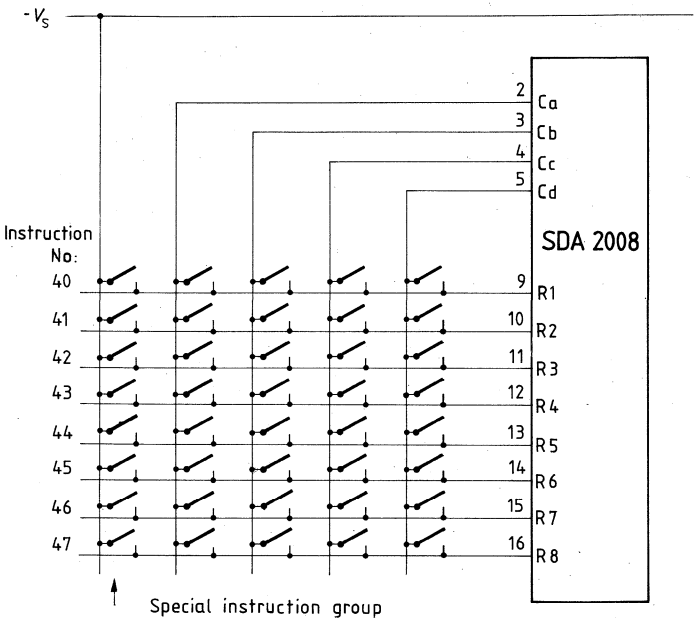


*) Disconnection only possible, if IRA is not set to – V_S at low impedance.

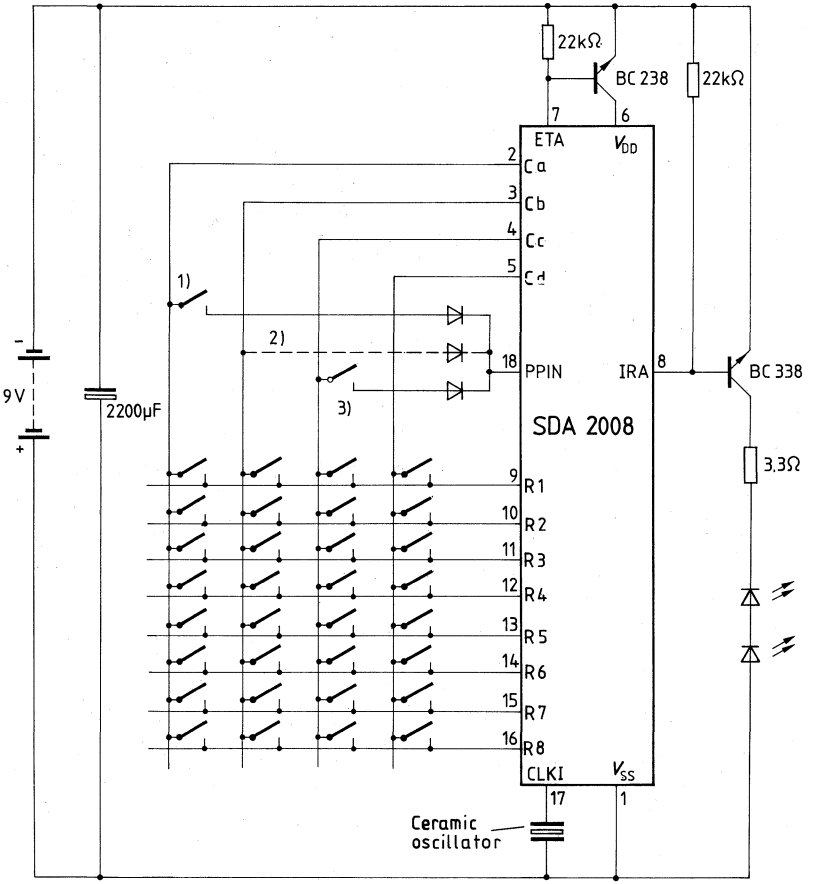
Extension for 60 instructions with additional diodes



$-V_S$ as fifth matrix column



Application circuit



If only one of these three possibilities is used, no diode is required.

1) Shift key
2) Connection for shortened instruction interval
3) Start bit changeover

MOS circuit

Type	Ordering code	Package outline
SDA 2010	Q 67120-C 74	DIP 40

Features

- 8 bit CPU, ROM, RAM, IN/OUT in a DIP 40 package
- 4 analog outputs with 6 bit resolution
- 30 digital IN/OUT lines
  Two serial interfaces
  Two 8 bit interfaces
  Two 4 bit interfaces
  Two test inputs
- 2 Kbyte ROM
- 64 byte RAM
- 10 µs cycle time – 1 or 2 cycles per instruction
- Zero passage detector
- Interface for mudulated digital signal
- Interval timer/counter
- 5 V supply voltage
- Instructions – subset of SAB 8048

Brief description[1)]

The SDA 2010 stresses application-specific control functions surpassing the former purely numeric computation performance. As a result, the use of additional hardware could be reduced and software operations have been simplified, optimizing cost savings during the developmental and production stages. Although the SDA 2010 was designed for electronic entertainment devices, it is equally suitable for mass-produced applications requiring highly economic components.

The SDA 2010 includes a 2 Kbyte program memory (ROM), a 64 byte data memory (RAM) and four 6 bit D/A converters. The 30 digital IN/OUT lines are comprised of two 4 and 8 bit ports each, two test inputs and 2 serial interfaces consisting of one data and one clock line each. Test input T0 processes signals modulated with approx. 30 kHz and is equipped with a digital demodulator, which derives the envelope curve from the modulated digital signal. Since the digital demodulator forwards an unmodulated signal without changing it, test input T0 can also function as a normal digital input during operations with standard H/L levels. Test input T1 includes a zero passage detector and can also serve as a normal digital input. The SDA 2010 is equipped with its own oscillator and timer/counter.

1) Detailed description is available upon request

The instruction set includes 65 instructions (1-2 bytes), which can be processed in max. 2 cycles. Numerical problems can be processed in either binary or BCD arithmetic modes. The large number of available bit-handling instructions increases the efficiency of the controller functions.

The program development and system testing for the SDA 2010 are carried out on the SME development system in conjunction with the SDA 2010 emulator board EMB U2. The EMB U2 emulator consists of one 2 K EPROM (SAB 2716) as well as a 40 pin plug which is used to insert an SAB 8035 type microprocessor or an ICE 48 plug. In addition, the EBM U2 contains all the necessary hardware to simulate the four analog outputs and the serial and parallel interfaces of the SDA 2010. A 40 wire cable is used to connect the U2 emulator with the user system.

A version without the ROM (SDA 3010) is available for in-house software development on an SME system.

Technical data of the SDA 2010

Maximum ratings

Maximum ratings must carefully be observed to prevent the IC from being permanently damaged.

Supply voltage range	V_{SS}	−0.5 to 7	V
Voltage between any pin and ground	V	−0.5 to 7	V
Total power dissipation	P_{tot}	1	W
Storage temperature range	T_{stg}	−55 to 125	°C
Operational ambient temperature range	T_{amb}	0 to 70	°C

DC characteristics

$T_{amb} = 0\,°C$ to 70°C, $V_{CC} = V_{SB} = 5.5\ V \pm 1\ V$, $V_{SS} = 0\ V$

			min	max	
L input voltage	(Ports, SS0, SS1, RESET)	V_{iL}	−0.5	0.8	V
H input voltage	(Ports, SS0, SS1) ($V_{CC} = 5{,}0\ V \pm 10\%$)	V_{iH}	2.0	V_{CC}	V
H input voltage	(Ports, SS0, SS1) ($V_{CC} = 6.0\ V \pm 0{,}5\ V$)	V_{iH1}	2.4	V_{CC}	V
H input voltage	(RESET, XTAL 1)	V_{iH2}	3.0	V_{CC}	V
L output voltage	(Ports, ALE) ($I_{qL} = 1{,}6\ mA$)	V_{qL}		0.45	V
L output voltage	(SS0, SS1, SCP0, SCP1) ($I_{qL} = 4\ mA$)	V_{qL1}		0.45	V
L output voltage	(A00–A0–3) ($I_{qL} = 4\ mA$)	V_{qL2}		0.45	V
H output voltage	(Ports, ALE) ($I_{qH} = 50\ \mu A$)	V_{qH}	2.4		V
H output voltage	(SS0, SS1, SCP0, SCP1) ($I_{qH} = 150\ \mu A$)	V_{qH1}	2.4		V
H output voltage	(A00–A0–3) ($I_{qH} = 4\ mA$)	V_{qH2}	V_{CC}–0.45		V
H input current	(T0, T1) ($V_{iH} = V_{CC}$)	I_{iH}		10	µA
L input current	(Ports, SS0, SS1) ($V_{iL} = 0.45\ V$)	$-I_{iL}$	30	340	µA
Input voltage at T1	($C_{in} = 1\ \mu F$) (peak-to-peak)	V_{T1}	1	3	V
Zero passage detector current consumption		I_{CC}		80	mA

AC characteristics

$T_{amb} = 0\,°C$ to 70 °C, $V_{CC} = V_{SB} = 5.5\ V \pm 1\ V$, $V_{SS} = 0V$

		min	max	
Cycle time (3 MHz crystal; = 10 µs)	t_C	10	50	µs
ALE pulse width ($t_C = 10\ \mu s$)	t_{ALE}	1.3		µs
Variation of oscillator frequency ($f = 2.5$ MHz, $R = 15\ k\Omega$)	Δf_{OSC}	−20	+20	%
Length of an unmodulated signal at T0 test input (3 MHz crystal)	t_{MT0}	60	–	µs
Frequency of a modulated signal at T0 test input (3 MHz crystal)	f_{TR}	30	35	kHz
Frequency range of the zero passage detector (input T1)	f_{T1}	0.03	1	kHz

Pin configuration

Pin No.	Symbol	Function
40	V_{CC}	+ 5 V
20	V_{SS}	GND 0 V
21, 22	XTAL1, XTAL2	Connection for crystal or similar
10–17	P0 0–7	Quasi-bidirectional 8 bit port
24–31	P1 0–7	Quasi-bidirectional 8 bit port
32–35	P2 0–3	Quasi-bidirectional 4 bit port
7–4	P3 0–3	Quasi-bidirectional 4 bit port
38, 39, 1, 2	A00–A0–A3	4 analog outputs. The analog values are output as rectangular signals with a frequency of approx. 2 kHz, during which the duty cycle corresponds to the analog value.
37, 8	SS0, SS1	Serial interface IN/OUT pin
36, 9	SCP0, SCP1	Serial interface clock pulse
23	RESET	Reset input for the initialization of the computer. Resets program counter, erases the status FFs. Sets all digital outputs to the H state (active H).
3	T0	Input that can be tested with the conditional jump instructions JT0 and JNT0. The input contains a digital demodulator and can be used for the separation of the envelope curve from a modulated signal.
19	T1	Input that can be tested with the conditional jump instructions JT1 and JNT1. Serves simultaneously as an external counter input. (Selection of functions with instruction STRT CNT). The input can also be used for zero passage recognition of low frequency alternating voltages.
18	ALE	This output generates one clock pulse signal per cycle.

Instruction set of SDA 2010

	Mnemonic	Description	Bytes	Cycles	Hexadecimal opcode
Accumulator	ADD A, Rr	Add register to A	1	1	68–6F
	ADD A, @ R	Add data memory to A	1	1	60–61
	ADD A, #data	Add immediate to A	2	2	03
	ADDC A, Rr	Add register with carry	1	1	78–7F
	ADDC A, @ R	Add data memory with carry	1	1	70–71
	ADDC A, #data	Add immediate with carry	2	2	13
	ANL A, Rr	And register to A	1	1	58–5F
	ANL A, @ R	And data memory to A	1	1	50–51
	ANL A, #data	And immediate to A	2	2	53
	ORL A, Rr	Or register to A	1	1	48–4F
	ORL A, @ R	Or data memory to A	1	1	40–41
	ORL A, #data	Or immdediate to A	2	2	43
	XRL A, Rr	Exclusive Or register to A	1	1	D8–DF
	XRL A, @ R	Exclusive Or data memory to A	1	1	D0–D1
	XRL A, #data	Exclusive Or immediate to A	2	2	D3
	INC A	Increment A	1	1	17
	DEC A	Decrement A	1	1	07
	CLR A	Clear A	1	1	27
	CPL A	Complement A	1	1	37
	DA A	Decimal adjust A	1	1	57
	SWAP A	Swap nibbles of A	1	1	47
	RL A	Rotate A left	1	1	E7
	RLC A	Rotate A left through carry	1	1	F7
	RR A	Rotate A right	1	1	77
	RRC A	Rotate A right through carry	1	1	67

Instruction set of SDA 2010

	Mnemonic	Description	Bytes	Cycles	Hexadecimal opcode
IN/OUT	IN A, Pp	Input port to A	1	2	08, 09, OC, OD
	OUT Pp, A	Output A to port	1	2	90, 39, 3C, 3D
	IN A, Sn	Input serial port to A0	1	2	OE–OF
	OUT Sn, A	Output A0 to serial port	1	2	3E–3F
Registers	INC Rr	Increment register	1	1	18–1F
	INC @ R	Increment data memory	1	1	10–11
Sub-routines	CALL	Jump to subroutine	1	2	14, 34, 54, 74, 94, B4, D4, F4,
	RET	Return	1	2	83
Branches	JMP adr	Jump unconditional	2	2	04, 24, 44, 64, 84, A4, C4, E4
	JMPP @ A	Jump indirect	1	2	B3
	DJNZ Rr, adr	Decrement register and jump on R not zero	2	2	E8–EF
	JC adr	Jump on carry = 1	2	2	F6
	JNC adr	Jump on carry = 0	2	2	E6
	JZ adr	Jump on A zero	2	2	C6
	JNZ adr	Jump on A not zero	2	2	96
	JT0 adr	Jump on T0 = 1	2	2	36
	JNT0 adr	Jump on T0 = 0	2	2	26
	JT1 adr	Jump on T1 = 1	2	2	56
	JNT1 adr	Jump on T1 = 0	2	2	46
	JTF adr	Jump on timer flag	2	2	16
Flags	CLR C	Clear carry	1	1	97
	CPL C	Complement carry	1	1	A7

Instruction set of SDA 2010

	Mnemonic	Description	Bytes	Cycles	Hexadecimal opcode
Transfer instructions	MOV A, Rr	Move register to A	1	1	F8–FF
	MOV A, @ R	Move data memory to A	1	1	F0–F1
	MOV A, #data	Move immediate to A	2	2	23
	MOV Rr, A	Move A to register	1	1	A8–AF
	MOV@ R, A	Move A to data memory	1	1	A0–A1
	MOV Rr # data	Move immediate to register	2	2	B8–BF
	MOV @ R, # data	Move immediate to data memory	2	2	B0–B1
	XCH A, Rr	Exchange A and register	1	1	28–2F
	XCH A, @R	Exchange A and data memory	1	1	20–21
	XCHD A,@ R	Exchange nibble of A and register	1	1	30–31
	MOVP A, @ A	Move to A from current page	1	2	A3
Timer/Counter	MOV A, T	Read timer/counter	1	1	42
	MOV T, A	Load timer/counter	1	1	62
	STRT T	Start timer	1	1	55
	STRT CNT	Start counter	1	1	45
	STOP TCNT	Stop timer/counter	1	1	65
	MOV DA, A	Move A to DA – converter	1	2	91
	NOP	No operation	1	1	00

Symbols and abbreviations

A	Accumulator
adr	11 bit program memory address
CNT	Event counter
DA	D/A converter
data	8 bit binary number
P	Mnemonic for "in page" operation
Pp	Port. label (p = 0–3)
Rr	Register label (r = 0–7)
Sn	S interface label (n = 0; 1)
T	Timer
T0, T1	Test 0, Test 1
#	Refers to immediate data
@	Refers to indirect addressing

Bipolar circuit

Type	Ordering code	Package outline
SDA 2014	Q 67000-Y 538	DIP 18

The SDA 2014 LED display driver enables cascade connection, decodes a serial BCD code and drives in multiplex operation 2 or 4 digits, as required. An output with serial data output permits cascade connections of the display drivers for more than 4 digits (6, 8, 10, etc.).

Features

- Serially read-in BCD code
- Enable input
- Any number of ICs permitted for cascade connection optional 2- or 4-digit operation

Maximum ratings

Supply voltage	V_S	8.5	V
Supply current	I_S	400	mA
Input voltage (pins 7, 8, 9)	V_i	5.5	V
Output voltage (pin 10)	$V_{q\,H}$	8.5	V
H output current (pins 11, 12, 13, 15, 16, 17, 18)	$I_{q\,H}$	−60	mA
L output current (pins 2, 3, 4, 5)	$I_{q\,L}$	380	mA
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−65 to 150	°C
Thermal resistance (system-air)	$R_{th\,SA}$	80	K/W

Operating range

Supply voltage range	V_S	4.5 to 8	V
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics ($V_S = 5.0$ V, $T_{amb} = 25\,°C$, unless otherwise specified)

		min	typ	max	
Internal current consumption (without load) ($V_S = 8$ V)	I_S		20	31	mA
Current consumption ($V_S = 8$ V)	I_S			380	mA
Upper threshold voltage (pins 7, 8, 9)	V_{thu}		1.3		V
Lower threshold voltage (pins 7, 8, 9)	V_{thl}		0.7		V
Hysteresis (pins 7, 8, 9)			0.6		V
H output voltage (pins 11, 12, 13, 15, 16, 17, 18) ($V_S = 8$ V, $I_{qH} = -40$ mA)	V_{qH}			7.35	V
H output voltage (pins 11, 12, 13, 15, 16, 17, 18) ($V_S = 4.5$ V, $I_{qH} = -40$ mA)	V_{qH}	3.2			V
L output voltage (pins 2, 3, 4, 5) ($V_S = 4.5$ V, $I_{qL} = 280$ mA)	V_{qL}		0.6	0.8	V
H input current (pins 7, 8, 9) ($V_i = 5$ V)	I_{iH}			8	µA
L input current (pins 6, 7, 8, 9) ($V_S = 8$ V, $V_{iL} = 0.4$ V)	I_{iL}			−50	µA
H output current (pins 11, 12, 13, 15, 16, 17, 18) ($V_S = 8$ V)	I_{qH}			−48*	mA
H output current (pins 2, 3, 4, 5) ($V_S = 8$ V)	I_{qH}			50	µA
L output current (pins 2, 3, 4, 5) ($V_S = 8$ V)	I_{qL}			336	mA
H output voltage (pin 10) ($-I_{qH} = 200$ µA)	V_{qH}	V_S−2	V_S−1.5	V_S−1	V
L output voltage (pin 10) ($I_{qL} = 3$ mA, $V_S = 4.5$ V)	V_{qL}			0.4	V
Short-circuit output current (pin 10) ($V_S = 8$ V, max. duration: 1 sec)	I_q	−20		−50	mA

* 48 mA ≙ 12 mA integral value at 4 digit operation or 24 mA at 2 digit operation, respectively

Switching times

		min	typ	max	
H pulse width (level = 2 V)	t_{WH8}	0.5	0.1		µs
L pulse width (level = 0.6 V)	t_{WL8}	3	1.5		µs
Hold time	t_{H8}	0.3	0		µs
Set-up time	t_{S9}	0	−0.4		µs
Hold time	t_{H9}	3	1.5		µs
Set-up time	t_{S7}	0	−0.3		µs
Hold time	t_{H7}	3			µs
L pulse width (level = 0.6 V)	t_{WL7}	3	1.6		µs
H pulse width (level = 2 V)	t_{WH7}	70	50		µs
H pulse width (pins 2, 3, 4, 5)	t_{WH}		4.5		ms
4-digit operation					
L pulse width (pins 2, 3, 4, 5)	t_{WL}		1.5		ms
4-digit operation					
Set-up time (pins 2, 3, 4, 5)	t_S	0		2	µs
H pulse width	$t_{WH2.3}$		3		ms
2-digit operation					
L pulse width	$t_{WL2.3}$		3		ms
2-digit operation					
Set-up time	$t_{S2.3}$	0		2	µs

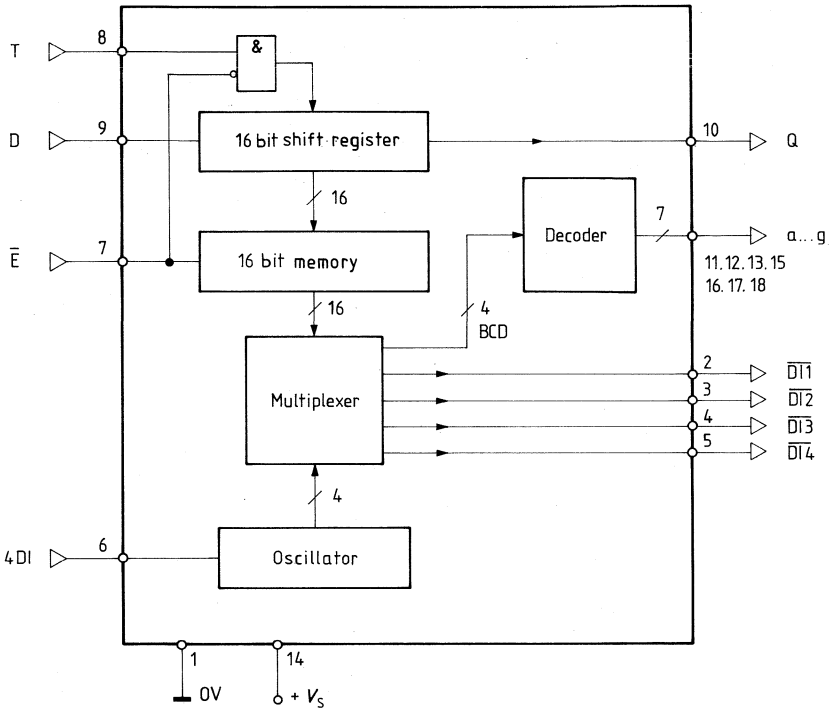
Truth table

Data D LSB...MSB[1]				Display	Segment driver (active H) a	b	c	d	e	f	g
L	L	L	L	0	H	H	H	H	H	H	L
H	L	L	L	1	L	H	H	L	L	L	L
L	H	L	L	2	H	H	L	H	H	L	H
H	H	L	L	3	H	H	H	H	L	L	H
L	L	H	L	4	L	H	H	L	L	H	H
H	L	H	L	5	H	L	H	H	L	H	H
L	H	H	L	6	H	L	H	H	H	H	H
H	H	H	L	7	H	H	H	L	L	L	L
L	L	L	H	8	H	H	H	H	H	H	H
H	L	L	H	9	H	H	H	H	L	H	H
L	H	L	H	dark	L	L	L	L	L	L	L
H	H	L	H	dark	L	L	L	L	L	L	L
L	L	H	H	dark	L	L	L	L	L	L	L
H	L	H	H	dark	L	L	L	L	L	L	L
L	H	H	H	dark	L	L	L	L	L	L	L
H	H	H	H	dark	L	L	L	L	L	L	L

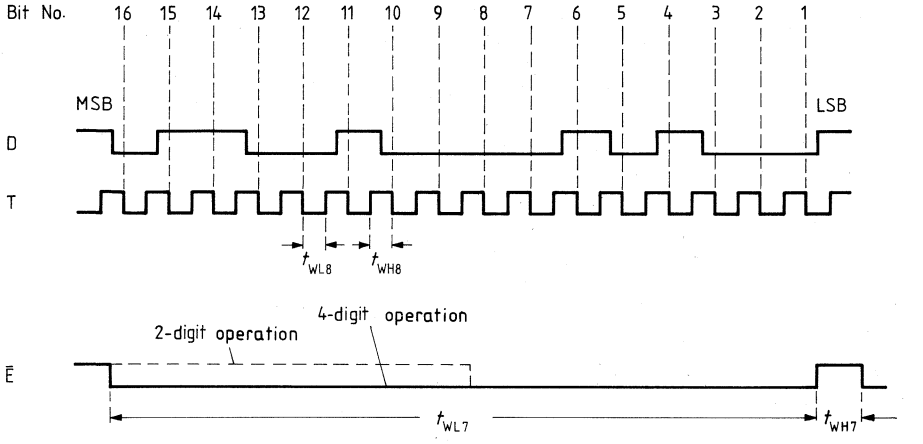
Segment designation

1) LSB = least significant bit
MSB = most significant bit

Block diagram



Pulse diagram



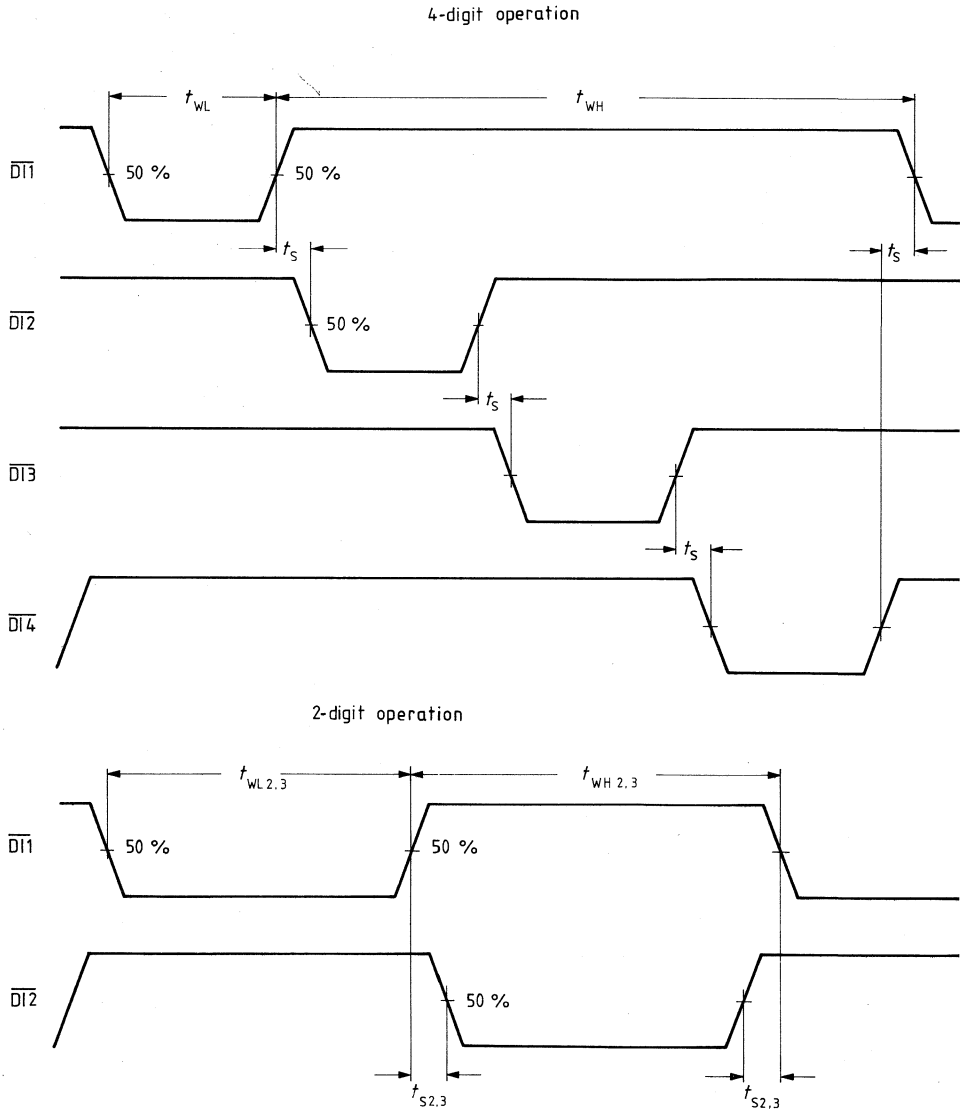
Memory contents after the rising edge of E: (4-digit operation)

	L	H	H	L	L	H	L	L	L	L	H	L	H	L	L	L
Display	6				4				2				8			
	Digit 4				Digit 3				Digit 2				Digit 1			

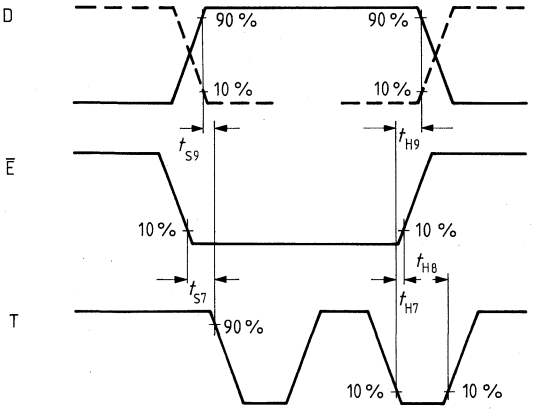
Memory contents and display at 2-digit operation

Remark: The information first shifted to D is displayed at digit 4; with digit 3, digit 2, and digit 1 following.
At every digit, MSB has to be shifted first.

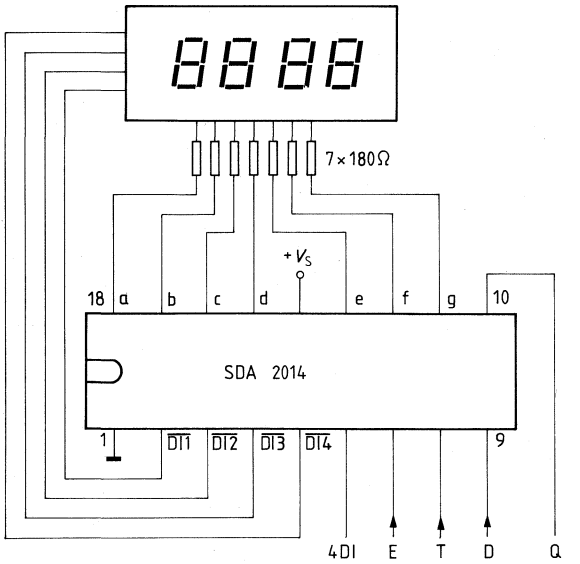
Timing diagram



Set-up and hold times



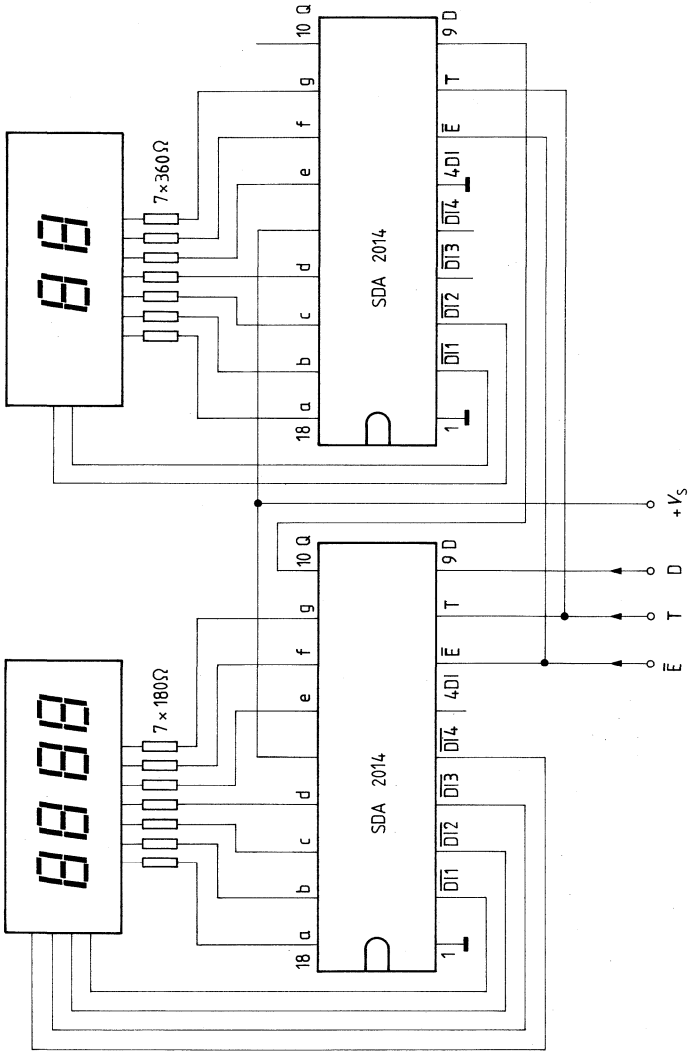
Application circuit 4-digit operation



At 2-digit operation ($\overline{DI1}$ and $\overline{DI12}$),4 DI is grounded

Application circuit

Example: Cascade connection to 6 digits



MOS circuit

Type	Ordering code	Package outline
SDA 2020	Q 67120-C 131	DIP 28

Features

- 8 bit CPU, ROM, RAM, IN/OUT in DIP 28 package
- 4 analog outputs with 6 bit resolution
- 18 digital IN/OUT lines
  serial interface
  8 bit interface
  4 bit interface
  2 bit interface
  two test inputs
- 1 Kbyte ROM
- 64 byte RAM
- 10 µs cycle time – 1 or 2 cycles per instruction
- Zero passage detector
- Interface for modulated digital signal
- Interval timer/counter
- 5 V supply voltage
- Instructions – subset of SAB 8048

Brief description[1])

Following the design concept implemented with the SDA 2010, the SDA 2020 stresses application-specific control functions surpassing the former purely numeric computation performance. As a result, the use of additional hardware could be reduced and software operations have been simplified, optimizing cost savings during the developmental and production stages.

Although the SDA 2020 was designed for electronic entertainment devices, it is equally suitable for mass-produced applications requiring highly economic components.

The SDA 2020 includes a 1 Kbyte program memory (ROM), a 64 byte data memory (RAM), and four 6 bit D/A converters. The 18 digital IN/OUT lines are comprised of one 2, 4, and 8 bit port each, two test inputs and a serial interface consisting of one data and one clock line. Test input T0 processes signals modulated with approx. 30 kHz and is equipped with a digital demodulator, which derives the envelope curve from the modulated digital signal. Since the digital demodulator forwards an unmodulated signal without changing it, test input T0 can also function as a normal digital input during operations with standard H/L levels. Test input T1 includes a zero passage detector and can also serve as a normal digital input. The SDA 2020 is equipped with its own oscillator and timer/counter.

1) Detailed description is available upon request.

The instruction set includes 63 instructions (1-2 bytes), which can be processed in max. 2 cycles. Numerical problems can be processed in either binary or BCD arithmetic modes. The large number of available bit-handling instructions increases the efficiency of the controller functions.

The program development and system testing for the SDA 2020 are carried out on the SME development system in conjunction with the SDA 2020 emulator board EMB U22. The EMB U22 emulator consists of one 2 K EPROM (SAB 2716) as well as a 40 pin plug which is used to insert an SAB 8035 type microprocessor or an ICE 48 plug. In addition, the EMB U22 contains all the necessary hardware to simulate the four analog outputs and the serial and parallel interfaces of the SDA 2020. A 28 wire cable is used to connect the U22 emulator with the user system.

Maximum ratings

Maximum ratings must carefully be observed to prevent the IC from being permanently damaged.

Supply voltage range	V_{SS}	−0.5 to 7	V
Voltage between any pin and ground	V	−0.5 to 7	V
Total power dissipation	P_{tot}	1	W
Storage temperature range	T_{stg}	−55 to 125	°C
Ambient temperature in operation	T_{amb}	0 to 70	°C

DC voltage characteristics

($T_{amb} = 0\,°C$ to $70\,°C$; $V_{CC} = 5.5\ V \pm 1\ V$; $V_{SS} = 0\ V$)

			Test condition	min	max	
L input voltage	(ports, SS1, RESET)	V_{iL}		−0.5	0.8	V
H input voltage	(ports, SS1)	V_{iH}	$V_{CC} = 5.0\ V \pm 10\%$	2.0	V_{CC}	V
H input voltage	(ports, SS1)	V_{iH1}	$V_{CC} = 6.0\ V \pm 0.5\ V$	2.4	V_{CC}	V
H input voltage	(RESET, X1)	V_{iH2}		3.0	V_{CC}	V
L output voltage	(ports, ALE)	V_{qL}	$I_{qL} = 1.6\ mA$		0.45	V
L output voltage	(SS1, SCP1)	V_{qL1}	$I_{qL} = 4\ mA$		0.45	V
L output voltage	(A0–A3)	V_{qL2}	$I_{qL} = 4\ mA$		0.45	V
H output voltage	(ports, ALE)	V_{qH}	$I_{qH} = 50\ \mu A$	2.4		V
H output voltage	(SS1, SCP1)	V_{qH1}	$I_{qH} = 150\ \mu A$	2.4		V
H output voltage	(A0–A3)	V_{qH2}	$I_{qH} = 4\ mA$	V_{CC}−0.45		V
H input current	T0, T1)	I_{iH}	$V_{iH} = V_{CC}$		10	µA
L input current	(ports, SS1)	$-I_{iL}$	$V_{iL} = 0.45\ V$	30	340	µA
Input voltage at T1	(peak-to-peak)	V_{T1}	$C_i = 1\ \mu F$	1	3	V
Zero passage detector current consumption		I_{CC}			80	mA

AC voltage characteristics

($T_{amb} = 0\,°C$ to $70\,°C$; $V_{CC} = 5.5\ V \pm 1\ V$; $V_{SS} = 0\ V$)

Cycle time	t_C	3 MHz crystal ≡ 10 µs)	10	50	µs
ALE pulse width	t_{ALE}	$t_C = 10\ \mu s$	1.3		µs
Variation of oscillator frequency	Δf_{OSC}	$f = 2.5\ MHz$, $R = 15\ k\Omega$	−20	+20	%
Period of an unmodulated signal at test input T0	t_{MT0}	3 MHz crystal	60		µs
Frequency of a modulated signal at test input T0	f_{TR}	3 MHz crystal	25	40	kHz
Frequency range of the zero passage detector (input T1)	f_{T1}		0.03	1	kHz
Width of an externally applied clock signal	t_{HOSC}	$f = 3\ MHz$ at X1	100	200	ns

Pin configuration

Pin No.	Symbol	Function
28	V_{DD}	+ 5 V
14	V_{SS}	GND 0 V
15, 16	X1, X2	Connection for crystal or similar
4–11	P0 0–7	Quasi bidirectional 8 bit port
18, 19	P1 0–1	Quasi bidirectional 2 bit port
20–23	P2 0–3	Quasi bidirectional 4 bit port
24, 25, 26, 27	A0–A3	4 analog outputs. The analog values are output as rectangular signals with a frequency of approx. 2 kHz, during which the pulse width is proportional to the analog value.
1	SS1	Serial interface IN/OUT pin
2	SCP1	Serial interface clock pulse
17	RESET	Reset input for computer initialization. Resets program counter, erases the status FFs, sets all digital outputs to H state (active H). Exception P2 0–3 = L! Resets all analog outputs.
3	T0	Input that can be tested with the conditional jump instructions JT0 and JNT0. The input contains a digital demodulator and can be used for the separation of the envelope curve from a modulated signal.
13	T1	Input that can be tested with the conditional jump instructions JT1 and JNT1. Serves simultaneously as an external counter input. (Selection of functions with instruction STRT CNT). The input can also be used for zero passage recognition of low frequency alternating voltages.
12	ALE	This output generates one clock pulse signal per cycle.

Instruction set of SDA 2020

	Mnemonic	Description	Bytes	Cycles	Hexadecimal opcode
Accumulator	ADD A, Rr	Add register to A	1	1	68–6F
	ADD A,@ R	Add data memory to A	1	1	60–61
	ADD A, #data	Add immediate to A	2	2	03
	ADDC A, Rr	Add register with carry	1	1	78–7F
	ADDC A,@ R	Add data memory with carry	1	1	70–71
	ADDC A, # data	Add immediate with carry	2	2	13
	ANL A, Rr	And register to A	1	1	58–5F
	ANL A,@ R	And data memory to A	1	1	50–51
	ANL A, # data	And immediate to A	2	2	53
	ORL A, Rr	Or register to A	1	1	48–4F
	ORL A,@ R	Or data memory to A	1	1	40–41
	ORL A, # data	Or immediate to A	2	2	43
	XRL A, Rr	Exclusive Or register to A	1	1	D8–DF
	XRL A,@ R	Exclusive Or data memory to A	1	1	D0–D1
	XRL A, # data	Exclusive Or immediate to A	2	2	D3
	INC A	Increment A	1	1	17
	DEC A	Decrement A	1	1	07
	CLR A	Clear A	1	1	27
	CPL A	Complement A	1	1	37
	DA A	Decimal adjust A	1	1	57
	SWAP A	Swap nibbles of A	1	1	47
	RL A	Rotate A left	1	1	E7
	RLC A	Rotate A left through carry	1	1	F7
	RR A	Rotate A right	1	1	77
	RRC A	Rotate A right through carry	1	1	67

Instruction set of SDA 2020

	Mnemonic	Description	Bytes	Cycles	Hexadecimal opcode
IN/OUT	IN A, Pp	Input port to A	1	2	08, 09, OC
	OUT Pp, A	Output A to port	1	2	90, 39, 3C
	INA A, S1	Input serial port to A0	1	2	OF
	OUT S1, A	Output A0 to serial port 1	1	2	3F
Register	INC Rr	Increment register	1	1	18–1F
	INC @ R	Increment data memory	1	1	10–11
Sub-routines	CALL	Jump to subroutine	1	2	14, 34, 54, 74, 94, B4, D4, F4,
	RET	Return	1	2	83
Branches	JMP adr	Jump unconditional	2	2	04, 24, 44, 64, 84, A4, C4, E4
	JMPP @ A	Jump indirect	1	2	B3
	DJNZ Rr adr	Decrement register and jump on R not zero	2	2	E8–EF
	JC adr	Jump on carry = 1	2	2	F6
	JNC adr	Jump on carry = 0	2	2	E6
	JZ adr	Jump on A zero	2	2	C6
	JNZ adr	Jump on A not zero	2	2	96
	JT0 adr	Jump on T0 = 1	2	2	36
	JNT0 adr	Jump on T0 = 0	2	2	26
	JT1 adr	Jump on T1 = 1	2	2	56
	JNT1 adr	Jump on T1 = 0	2	2	46
	JTF adr	Jump on timer flag	2	2	16
Flags	CLR C	Clear carry	1	1	97
	CPL C	Complement carry	1	1	A7

Instruction set of SDA 2020

	Mnemonic	Description	Bytes	Cycles	Hexadecimal Opcode
Transfer instructions	MOV A, Rr,	Move register to A	1	1	F8–FF
	MOV A, @R	Move data memory to A	1	1	F0-F1
	MOV A, # data	Move immediate to A	2	2	23
	MOV Rr, A	Move A to register	1	1	A8-AF
	MOV @R, A	Move A to data memory	1	1	A0-A1
	MOV R r #data	Move immediate to register	2	2	B8-BF
	MOV@R,#data	Move immediate to data memory	2	2	B0–B1
	XCH A, Rr	Exchange A and register	1	1	28–2F
	XCH A,@ R	Exchange A and data memory	1	1	20–21
	XCHD A,@R	Exchange nibble of A and register	1	1	30–31
	MOVP A, @ A	Move to A from current page	1	2	A3
Timer/Counter	MOV A, T	Read timer/counter	1	1	42
	MOV T, A	Load timer/counter	1	1	62
	STRT T	Start timer	1	1	55
	STRT CNT	Start counter	1	1	45
	STOP TCNT	Stop timer/counter	1	1	65
	MOV DA, A	Move A to DA – converter	1	2	91
	NOP	No operation	1	1	00

Symbols and abbreviations

A	Accumulator
adr	10 bit program memory address
CNT	Event counter
DA	D/A converter
data	8 bit binary number
P	Mnemonic for "in-page" operation
Pp	Port label (p = 0–2)
Rr	Register label (r = 0–7)
S1	S interface label (n = 0; 1)
T	Timer
T0, T1	Test 0, test 1
#	Refers to immediate data
@	Refers to indirect addressing

MOS circuit

Type	Ordering code	Package outline
SDA 2030	Q 67120-C 132	DIP 28

Features

- 8 bit CPU, ROM, RAM, IN/OUT in the DIP 28 package
- 4 analog outputs with 6 bit resolution
- 18 digital IN/OUT lines
  serial interface
  8 bit interface
  4 bit interface
  2 bit interface
  two test inputs
- 2 Kbyte ROM
- 64 byte RAM
- 10 µs cycle time – 1 or 2 cycles per instruction
- Zero passage detector
- Interface for modulated digital signal
- Interval timer/counter
- 5 V supply voltage
- Instructions – subset of SAB 8048

Brief description[1])

Following the design concept implemented with the SDA 2010, the SDA 2030 stresses application-specific control functions surpassing the former purely numeric computation performance. As a result, the use of additional hardware could be reduced and software operations have been simplified, optimizing cost savings during the developmental and production stages.

Although the SDA 2030 was designed for electronic entertainment devices, it is equally suitable for mass-produced applications requiring highly economic components.

The SDA 2030 includes a 2 Kbyte program memory (ROM), a 64 byte data memory (RAM) and four 6 bit D/A converters. The 18 digital IN/OUT lines are comprised of one 2, 4, and 8 bit port each, two test inputs and a serial interface consisting of one data and one clock line. Test input T0 processes signals modulated with approx. 30 kHz and is equipped with a digital demodulator, which derives the envelope curve from the modulated digital signal. Since the digital demodulator forwards an unmodulated signal without changing it, test input T0 can also function as a normal digital input during operations with standard H/L levels. Test input T1 includes a zero passage detector and can also serve as a normal digital input. The SDA 2030 is equipped with its own oscillator and timer/counter.

1) Detailed description is available upon request.

The instruction set includes 63 instructions (1-2 bytes), which can be processed in max. 2 cycles. Numerical problems can be processed in either binary or BCD arithmetic modes. The large number of available bit-handling instructions increases the efficiency of the controller functions.

The program development and system testing for the SDA 2030 are carried out on the SME development system in conjunction with the SDA 2030 emulator board EMB U23. The EMB U23 emulator consists of one 2 K EPROM (SAB 2716) as well as a 40 pin plug which is used to insert an SAB 8035 type microprocessor or an ICE 48 plug. In addition, the EMB U23 contains all the necessary hardware to simulate the four analog outputs and the serial and parallel interfaces of the SDA 2030. A 28 wire cable is used to connect the U23 emulator with the user system.

Maximum ratings

Maximum ratings must carefully be observed to prevent the IC from being permanently damaged.

Supply voltage range	V_{SS}	−0.5 to 7	V
Voltage between any pin and ground	V	−0.5 to 7	V
Total power dissipation	P_{tot}	1	W
Storage temperature range	T_{stg}	−55 to 125	°C
Ambient temperature in operation	T_{amb}	0 to 70	°C

DC voltage characteristics

(T_{amb} = 0 °C to 70 °C; V_{CC} = 5.5 V ± 1 V; V_{SS} = 0 V)

			Test condition	min	max	
L input voltage	(ports, SS1, RESET)	V_{iL}		−0.5	0.8	V
H input voltage	(ports, SS1)	V_{iH}	V_{CC} = 5.0 V ±10%	2.0	V_{CC}	V
H input voltage	(ports, SS1)	V_{iH1}	V_{CC} = 6.0 V ±0.5 V	2.4	V_{CC}	V
H input voltage	(RESET, X1)	V_{iH2}		3.0	V_{CC}	V
L output voltage	(ports, ALE)	V_{qL}	I_{qL} = 1.6 mA		0.45	V
L output voltage	(SS1, SCP1)	V_{qL1}	I_{qL} = 4 mA		0.45	V
L output voltage	(A0–A3)	V_{qL2}	I_{qL} = 4 mA		0.45	V
H output voltage	(ports, ALE)	V_{qH}	I_{qH} = 50 µA	2.4		V
H output voltage	(SS1, SCP1)	V_{qH1}	I_{qH} = 150 µA	2.4		V
H output voltage	(A0–A3)	V_{qH2}	I_{qH} = 4 mA	V_{CC}−0.45		V
H input current	(T0, T1)	I_{iH}	V_{iH} = V_{CC}		10	µA
L input current	(ports, SS1)	$-I_{iL}$	V_{iL} = 0.45 V	30	340	µA
Input voltage at T1	(peak-to-peak)	V_{T1}	C_i = 1 µF	1	3	V
Zero passage detector current consumption		I_{CC}			80	mA

AC voltage characteristics

(T_{amb} = 0 °C to 70 °C; V_{CC} = 5.5 V ± 1 V; V_{SS} = 0 V)

			min	max	
Cycle time	t_C	3 MHz crystal (≡10 µs)	10	50	µs
ALE pulse width	t_{ALE}	t_C = 10 µs	1.3		µs
Variation of oscillator frequency	Δf_{OSC}	f = 2.5 MHz, R = 15 kΩ	−20	+20	%
Period of an unmodulated signal at test input T0	t_{MT0}	3 MHz crystal	60		µs
Frequency of a modulated signal at test input T0	f_{TR}	3 MHz crystal	25	40	kHz
Frequency range of the zero passage detector (input T1)	f_{T1}		0.03	1	kHz
Width of an externally applied clock signal	t_{HOSC}	f = 3 MHz at X1	100	200	ns

Pin configuration

Pin No.	Symbol	Function
28	V_{DD}	+ 5 V
14	V_{SS}	GND 0 V
15, 16	X1, X2	Connection for crystal or similar
4–11	P0 0–7	Quasi bidirectional 8 bit port
18, 19	P1 0–1	Quasi bidirectional 2 bit port
20–23	P2 0–3	Quasi bidirectional 4 bit port
24, 25, 26, 27	A0–A3	4 analog outputs. The analog values are output as rectangular signals with a frequency of approx. 2 kHz, during which the pulse width is proportional to the analog value.
1	SS1	Serial interface IN/OUT pin
2	SCP1	Serial interface clock pulse
17	RESET	Reset input for computer initialization. Resets program counter, erases the status FFs, sets all digital outputs to H state (active H). Exception P2 0–3 = L! Resets all analog outputs.
3	T0	Input that can be tested with the conditional jump instructions JT0 and JNT0. The input contains a digital demodulator and can be used for the separation of the envelope curve from a modulated signal.
13	T1	Input that can be tested with the conditional jump instructions JT1 and JNT1. Serves simultaneously as an external counter input. (Selection of functions with instruction STRT CNT). The input can also be used for zero passage recognition of low frequency alternating voltages.
12	ALE	This output generates one clock pulse signal per cycle.

Instruction set of SDA 2030

	Mnemonic	Description	Bytes	Cycles	Hexadecimal opcode
Accumulator	ADD A, Rr	Add register to A	1	1	68–6F
	ADD A, @ R	Add data memory to A	1	1	60–61
	ADD A, # data	Add immediate to A	2	2	03
	ADDC A, Rr	Add register with carry	1	1	78–7F
	ADDC A, @ R	Add data memory with carry	1	1	70–71
	ADDC A, # data	Add immediate with carry	2	2	13
	ANL A, Rr	And register to A	1	1	58–5F
	ANL A, @ R	And data memory to A	1	1	50–51
	ANL A, # data	And immediate to A	2	2	53
	ORL A, Rr	Or register to A	1	1	48–4F
	ORL A, @ R	Or data memory to A	1	1	40–41
	ORL A, # data	Or immediate to A	2	2	43
	XRL A, Rr	Exclusive Or register to A	1	1	D8–DF
	XRL A, @ R	Exclusive Or data memory to A	1	1	D0–D1
	XRL A, # data	Exclusive Or immediate to A	2	2	D3
	INC A	Increment A	1	1	17
	DEC A	Decrement A	1	1	07
	CLR A	Clear A	1	1	27
	CPL A	Complement A	1	1	37
	DA A	Decimal adjust A	1	1	57
	SWAP A	Swap nibbles of A	1	1	47
	RL A	Rotate A left	1	1	E7
	RLC A	Rotate A left through carry	1	1	F7
	RR A	Rotate A right	1	1	77
	RRC A	Rotate A right through carry	1	1	67

Instruction set of SDA 2030

	Mnemonic	Description	Bytes	Cycles	Hexadecimal opcode
IN/OUT	IN A, Pp	Input port to A	1	2	08, 09, OC
	OUT Pp, A	Output A to port	1	2	90, 39, 3C
	IN A, S1	Input serial port to A0	1	2	OF
	OUT S1, A	Output A0 to serial port	1	2	3F
Register	INC Rr	Increment register	1	1	18–1F
	INC @ R	Increment data memory	1	1	10–11
Sub-routines	CALL	Jump to subroutine	1	2	14, 34, 54, 74 94, B4, D4, F4,
	RET	Return	1	2	83
Branches	JMP adr	Jump unconditional	2	2	04, 24, 44, 64, 84, A4, C4, E4
	JMPP @ A	Jump indirect	1	2	B3
	DJNZ Rr, adr	Decrement register and jump on R not zero	2	2	E8–EF
	JC adr	Jump on carry = 1	2	2	F6
	JNC adr	Jump on carry = 0	2	2	E6
	JZ adr	Jump on A zero	2	2	C6
	JNZ adr	Jump on A not zero	2	2	96
	JT0 adr	Jump on T0 = 1	2	2	36
	JNT0 adr	Jump on T0 = 0	2	2	26
	JT1 adr	Jump on T1 = 1	2	2	56
	JNT1 adr	Jump on T1 = 0	2	2	46
	JTR adr	Jump on timer flag	2	2	16
Flags	CLR C	Clear carry	1	1	97
	CPL C	Complement carry	1	1	A7

Instruction set of SDA 2030

	Mnemonic	Description	Bytes	Cycles	Hexadecimal opcode
Transfer instructions	MOV A, Rr	Move register to A	1	1	F8-FF
	MOV A, @ R	Move data memory to A	1	1	F0-F1
	MOV A, @ data	Move immediate to A	2	2	23
	MOV Rr, A	Move A to register	1	1	A8-AF
	MOV @ R, A	Move A to data memory	1	1	A0-A1
	MOV Rr, # data	Move immediate to register	2	2	B8-BF
	MOV@R,# data	Move immediate to data memory	2	2	B0-B1
	XCH A, Rr	Exchange A and register	1	1	28-2F
	XCH A, @ R	Exchange A and data memory	1	1	20-21
	XCHD A,@ R	Exchange nibble of A and register	1	1	30-31
	MOVP A,@ A	Move to A from current page	1	2	A3
Timer/Counter	MOV A, T	Read timer/counter	1	1	42
	MOV T, A	Load timer/counter	1	1	62
	STRT T	Start timer	1	1	55
	STRT CNT	Start counter	1	1	45
	STOP TCNT	Stop timer/counter	1	1	65
	MOV DA, A	Move A to DA – converter	1	2	91
	NOP	No operation	1	1	00

Symbols and abbreviations

A	Accumulator
adr	11 bit program memory address
CNT	Event counter
DA	D/A converter
data	8 bit binary number
P	Mnemonic for "in-page" operation
Pp	Port label (p = 0–2)
Rr	Register label (r = 0–7)
S1	S interface label
T	Timer
T0, T1	Test 0, Test 1
#	Refers to immediate data
@	Refers to indirect addressing

Bipolar circuit
MOS handling

Type	Ordering code	Package outline
SDA 2101	Q 67000-A1753	DIP 8

The component is intended for installation in TV receivers with frequency adjustment according to the frequency synthesis concept. It contains a preamplifier and an ECL divider with a scaling ratio of 1:64.

The frequency range extends up to 1 GHz.

- Few external components

Maximum ratings

Supply voltage	V_8	6	V
Input voltage (UHF/VHF & reference) (peak-to-peak)	V_i	2.5	V
Divider outputs	$V_{q\,6}$, $V_{q\,7}$	0 to V_S	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−55 to 150	°C
Thermal resistances (system-air)	$R_{th\,SA}$	115	K/W
(system case)	$R_{th\,SC}$	60	K/W

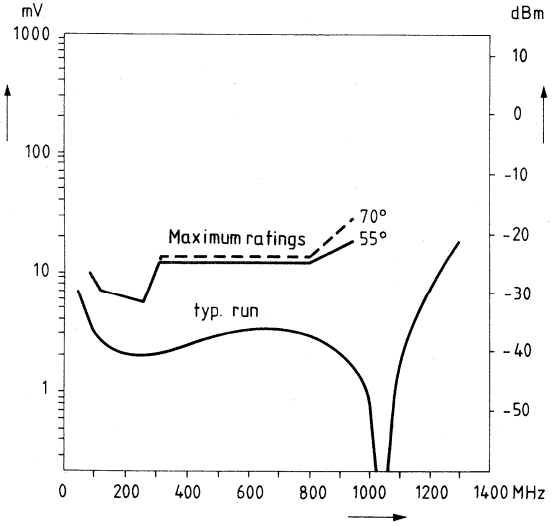
Operating range

Supply voltage	V_8	4.7 to 5.5	V
Input frequency ($T_{amb} = 0 \ldots 70\,°C$)	$f_{i\,1}$	80 to 1000	MHz
Ambient temperature range (80 MHz...950 MHz)	T_{amb}	0 to 85	°C

Characteristics ($V_S = 5$ V; $T_{amb} = 25$ °C)

		min	typ	max	
Input level ("input sensitivity")	V_2				
$V_S = 4.7$ to 5.5 V; $T_{amb} = 0$ to 70 °C					
80 MHz		−27		3	dBm
120 MHz		−30		3	dBm
250 MHz		−32		3	dBm
300 MHz		−24		3	dBm
800 MHz		−24		3	dBm
950 MHz		−15		3	dBm
$V_S = 4.7$ to 5.5 V; $T_{amb} = 0$ to 55 °C					
800 MHz		−25			dBm
950 MHz		−21			dBm
$V_S = 4.7$ to 5.5 V; $T_{amb} = 0$ to 25 °C					
800 MHz		−27			dBm
950 MHz		−27			dBm
Current consumption	I_8		50	70	mA
Output voltage shift (peak-to-peak)	V_6, V_7	0.5	1.0	1.2	V
Output voltage "high"	V_6, V_7		V_S		V

Typical input sensitivity of the divider



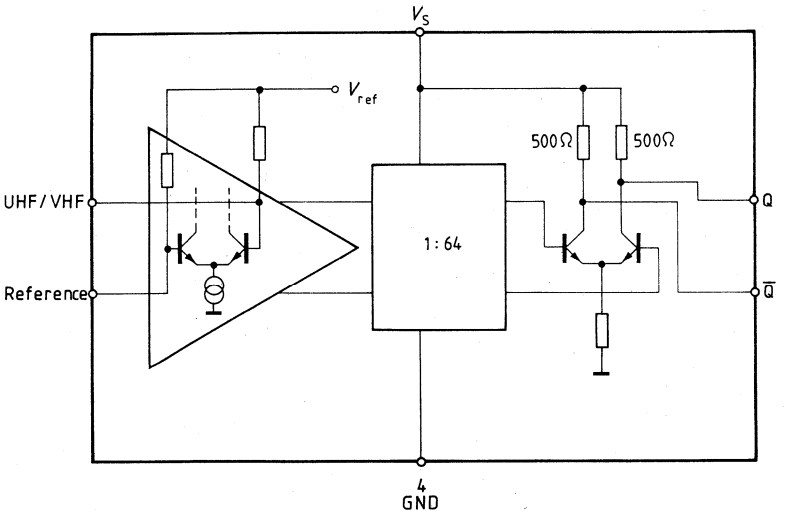
Circuit discription

The amplifier of the IC features a VHF/UHF input and a reference input. The reference input should be grounded by a capacitor with low series inductance. The divider of the component consists of several, controlled master slave flipflops with a dividing ratio of 1 : 64.

Pin configuration

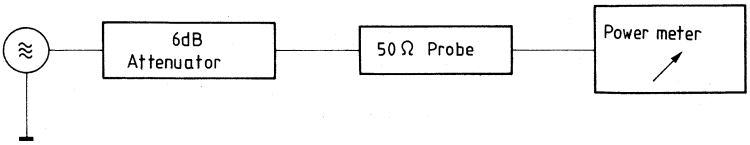
Pin No.	Function
1	N.C.
2	UHF/VHF signal input
3	Reference input
4	GND
5	N.C.
6	Divider output
7	Divider output
8	Supply voltage $+V_S$

Block diagram



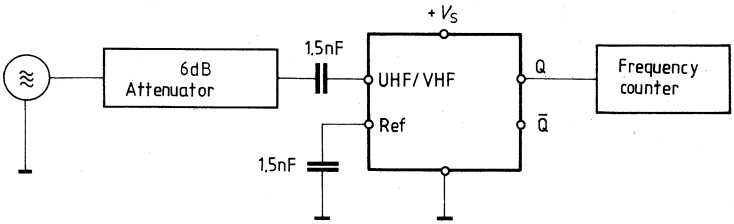
Test and measurement circuit

Signal generator
$Z_0 = 50\ \Omega$



Test circuit 1: Calibration of the signal generator

Signal generator
$Z_0 = 50\ \Omega$



Test circuit 2: Measurement of the input sensitivity

Application-Oriented Single Chip Microcomputer for Special Cost-Critical Applications

SDA 2110

MOS circuit

Type	Ordering code	Package outline
SDA 2110	Q 67120-C 73	DIP 28

Features

- 8 bit CPU, ROM, RAM, IN/OUT in a DIP 28 package
- 21 digital IN/OUT lines
  One serial interface
  One 8 bit interface
  Two 4 bit interfaces
  One 1 bit interface
  Two test inputs
- 1 Kbyte ROM
- 40 byte RAM
- 10 µs cycle time – 1 or 2 cycles per instruction
- Zero passage detector
- Interface for modulated digital signal
- Interval timer/counter
- 5 V supply voltage
- RAM standby operation
- Instructions – subset of the SAB 8048

Brief description[1)]

The SDA 2110 introduces a new generation of highly economic single chip computers with application-specific control functions. Considerable cost savings could be realized during the development and production stages, because the emphasis on specific applications reduces at the same time the number of additionally required hardware and simplifies the software tasks. Although the SD 2110 was designed for electronic entertainment devices, it is equally suitable for mass-produced applications requiring highly economic components.

For further cost optimizing with low performance requirements, the simplified version SDA 2111 can be substituted for the SDA 2110.

The SDA 2110 is eqipped with a 1 Kbyte program memory (ROM) and 40 byte data memory (RAM), which can be used in "standby" operation during heavily reduced output losses. The 21 digital IN/OUT lines include one 8-bit port, two 4-bit ports, two test inputs, one serial interface and one single bit interface. Test input T0 processes signals modulated with approx. 30 kHz and is equipped with a digital demodulator, which derives the envelope curve from the modulated digital signal. Since the digital demodulator forwards an unmodulated signal without changing it, test input T0 can also function as a normal digital input during operation with standard H/L levels. Test input T1 includes a zero passage (crossing) detector and can also serve as a normal digital input. A data and pulse line comprise the serial interface. The component is equipped with its own oscillator and timer/counter.

1) Detailed description is available upon request

The instruction set includes 66 instructions (1-2 bytes) which can be processed in max. 2 cycles. Numerical problems can be processed in either binary or BCD arithmetic mode. The large number of bit-handling instructions increases the efficiency of the controller functions.

The program development and system testing for the SDA 2110 is carried out on the SME development system with the SDA 2110 emulator board EMB U21. The EMB U21 emulator consists of one 2K EPROM (SAB 2716) as well as a 40 pin socket which is used to insert an SAB 8035L type microprocessor or the ICE 48 plug. In addition, the EMB U21 contains all the necessary hardware to simulate the serial and parallel interfaces of the SDA 2110. A 28 wire cable is used to connect the U21 emulator with the user system.

A version without ROM (SDA 3010) is available which enables in-house software developments on an SME device.

Maxmimum ratings

Maximum ratings must carefully be observed to prevent the IC from being permanently damaged.

Supply voltage range	V_{SS}	−0.5 to 7	V
Voltage between any pin and ground	V	−0.5 to 7	V
Total power dissipation	P_{tot}	1	W
Storage temperature range	T_{stg}	−55 to 125	°C
Operational ambient temperature range	T_{amb}	0 to 70	°C

DC voltage characteristics

$T_{amb} = 0\,°C$ to $70\,°C$, $V_{CC} = V_{SB} = 5.5\,V \pm 1\,V$, $V_{SS} = 0\,V$

			min	max	
L input voltage	(Ports, SS0, SS1, RESET)	V_{iL}	−0.5	0.8	V
H input voltage	(Ports, SS0, SS1) ($V_{CC} = 5.0\,V \pm 10\%$)	V_{iH}	2.0	V_{CC}	V
H input voltage	(Ports, SS0, SS1) ($V_{CC} = 6.0\,V \pm 0.5\,V$)	V_{iH1}	2.4	V_{CC}	V
H input voltage	(RESET, XTAL 1)	V_{iH2}	3.0	V_{CC}	V
L output voltage	(Ports, ALE) ($I_{qL} = 1.6\,mA$)	V_{qL}		0.45	V
L output voltage	(SS0, SS1, SCP0, SCP1) ($I_{qL} = 4\,mA$)	V_{qL1}		0.45	V
H output voltage	(Ports, ALE) ($I_{qH} = 50\,\mu A$)	V_{qH}	2.4		V
H output voltage	(SS0, SS1, SCP1) ($I_{qH} = 150\,\mu A$)	V_{qH1}	2.4		V
H input current	(T0, T1) ($V_{iH} = V_{CC}$)	I_{iH}		10	µA
L input current	(Ports, SS0, SS1) ($V_{iL} = 0.45\,V$)	$-I_{iL}$	30	340	µA
Input voltage at T1	($C_{in} = 1\,\mu F$) (peak-to-peak)	V_{T1}	1	3	V
Zero passage detector current consumption		I_{CC}		60	mA

AC voltage characteristics

$T_{amb} = 0\,°C$ to $70\,°C$, $V_{cc} = V_{SB} = 5.5\,V \pm 1\,V$, $V_{SS} = 0\,V$

		min	max	
Cycle time (3 MHz crystal; ≙ 10 µs)	t_C	10	50	µs
ALE pulse width ($t_C = 10\,\mu s$)	t_{ALE}	1.3		µs
Variation in oscillator frequency ($f = 2.5\,MHz$, $R = 15\,k\Omega$)	Δf_{OSC}	−20	+20	%
Length of an unmodulated signal at the T0 test input (3 MHz crystal)	t_{MT0}	60	–	µs
Frequency of a modulated signal at the T0 test input (3 MHz crystal)	f_{TR}	30	35	kHz
Frequency range of the zero passage detector (input T1)	f_{T1}	0.03	1	kHz

Pin configuration

Pin No.	Symbol	Function
28	V_{CC}	+ 5 V
1	V_{SB}	+ 5 V standby supply
14	V_{SS}	GND 0 V
15, 16	XTAL1, XTAL2	Connection for crystal or similar
4–11	P0 0–7	Quasi-bidirectional 8 bit port
18–21	P2 0–3	Quasi-bidirectional 4 bit port
22–25	P3 0–3	Quasi-bidirectional 4 bit port
26	SS0	1 bit interface IN/OUT pin
27	SS1	Serial interface S1 IN/OUT pin
2	SCP1	Serial interface S1 clock pulse
17	RESET	Reset input for computer initialization (active H). Resets program counter, erases the status FFs, sets all digital outputs to H state.
3	T0	Input that can be tested with the conditional jump instruction JT0 and JNT0. The input contains a digital demodulator and can be used for the separation of the envelope curve from a modulated signal.
13	T1	Input that can be tested with the conditional jump instruction JT1 and JNT1. Serves simultaneously as an external counter input. (Selection of functions with instruction STRT CNT). The input can also be used for zero passage recognition of low frequency alternating voltages.
12	ALE	This output generates one clock pulse signal per cycle.

SDA 2110 instruction set

	Mnemonic	Description	Bytes	Cycles	Hexadecimal opcode
Accumulator	ADD A, Rr	Add register to A	1	1	68–6F
	ADD A, @ R	Add data memory to A	1	1	60–61
	ADD A, # data	Add immediate to A	2	2	03
	ADDC A, Rr	Add register with carry	1	1	78–7F
	ADDC A,@ R	Add data memory with carry	1	1	70–71
	ADDC A, # data	Add immediate with carry	2	2	13
	ANL A, Rr	And register to A	1	1	58–5F
	ANL A, @ R	And data memory to A	1	1	50–51
	ANL A, # data	And immediate to A	2	2	53
	ORL A, Rr	Or register to A	1	1	48–4F
	ORL A, @ R	Or data memory to A	1	1	40–41
	ORL A, # data	Or immediate to A	2	2	43
	XRL A, Rr	Exclusive Or register to A	1	1	D8–DF
	XRL A, @ R	Exclusive Or data memory to A	1	1	D0–D1
	XRL A, # data	Exclusive Or immediate to A	2	2	D3
	INC A	Increment A	1	1	17
	DEC A	Decrement A	1	1	07
	CLR A	Clear A	1	1	27
	CPL A	Complement A	1	1	37
	DA A	Decimal adjust A	1	1	57
	SWAP A	Swap nibbles of A	1	1	47
	RL A	Rotate A left	1	1	E7
	RLC A	Rotate A left through carry	1	1	F7
	RR A	Rotate A right	1	1	77
	RRC A	Rotate A right through carry	1	1	67

SDA 2110 instruction set

	Mnemonic	Description	Bytes	Cycles	Hexadecimal opcode
IN/OUT	IN A, Pp	Input port to A	1	2	08, OC, OD
	OUT Pp, A	Output A to port	1	2	90, 3C, 3D
	IN A, S1	Input serial port to A0	1	2	OF
	IN A, S0	Input 1 bit port to A0	1	2	OE
	OUT S1, A	Output A0 to serial port	1	2	3F
	OUT S0, A	Output A0 to 1 bit port	1	2	3E
Sub-routines	CALL	Jump to subroutine	1	2	14, 34, 54, 74, 94, B4, D4, F4,
	RET	Return	1	2	83
Branches	JMP adr	Jump unconditional	2	2	04, 24, 44, 64, 84, A4, C4, E4
	JMPP @A	Jump indirect	1	2	B3
	DJNZ Rr, adr	Decrement register and jump on R not zero	2	2	E8–EF
	JC adr	Jump on carry = 1	2	2	F6
	JNC adr	Jump on carry = 0	2	2	E6
	JZ adr	Jump on A zero	2	2	C6
	JNZ adr	Jump on A not zero	2	2	96
	JT0 adr	Jump on T0 = 1	2	2	36
	JNT0 adr	Jump on T0 = 0	2	2	26
	JT1 adr	Jump on T1 = 1	2	2	56
	JNT1 adr	Jump on T1 = 0	2	2	46
	JTF adr	Jump on timer flag	2	2	16
Flags	CLR C	Clear carry	1	1	97
	CPL C	Complement carry	1	1	A7

SDA 2110 instruction set

	Mnemonic	Description	Bytes	Cycles	Hexadecimal opcode
Transfer instructions	MOV A, Rr	Move register to A	1	1	F8–FF
	MOV A,@ R	Move data memory to A	1	1	F0–F1
	MOV A, #data	Move immediate to A	2	2	23
	MOV Rr, A	Move A to register	1	1	A8–AF
	MOV@ R, A	Move A to data memory	1	1	A0–A1
	MOV Rr, # data	Move immediate to register	2	2	B8–BF
	MOV@R, # data	Move immediate to data memory	2	2	B0–B1
	XCH A, Rr	Exchange A and register	1	1	28–2F
	XCH A, @ R	Exchange A and data memory	1	1	20–21
	XCHD A, @ R	Exchange nibble of A and register	1	1	30–31
	MOVP A,@ A	Move to A from current page	1	2	A3
Timers/ Counters	MOV A, T	Read timer/counter	1	1	42
	MOV T, A	Load timer/counter	1	1	62
	STRT T	Start timer	1	1	55
	STRT CNT	Start counter	1	1	45
	STOP TCNT	Stop timer/counter	1	1	65
Re- gisters	INC Rr	Increment register	1	1	18–1F
	INC @ R	Increment data memory	1	1	10–11
	NOP	No operation	1	1	00

Symbols and abbreviations

A	Accumulator	Rr	Register label (r = 0–7)
adr	10 bit program memory address	Sn	S-Interface label (n = 0; 1)
CNT	Event counter	T	Timer
data	8 bit binary number	T0, T1	Test 0, Test 1
P	Mnemonic for "in page" operation	#	Refers to immediate data
Pp	Port label (p = 0, 2, 3)	@	Refers to indirect addressing

Bipolar circuit

Type	Ordering code	Package outline
SDA 2112-2	Q67000-A1778-E12	DIP 18

The SDA 2112-2 is fabricated in ASBC technology. In connection with a VCO (tuner) and a high-speed 1:64 divider, it forms a digitally programmable phase-locked loop for producing TV sets with PLL frequency-synthesis tuning. The PLL enables crystal-controlled setting of the tuner oscillator frequency for a 125 kHz rsolution in the frequency bands I/III, IV, and V.

A serial interface provides for simple connection to a microprocessor. The latter loads the programmable divider and the band-selection outputs with the appropriate information.

Features

- No external integrator necessary
- Internal buffer
- Microprocessor compatible

Maximum ratings

Supply voltage pin 18	V_{S1}	−0.3 to 7.5	V
Inputs			
Q 1, Q 2, F, $\overline{F}$ pin 1, 2, 15, 16	V_I	−0.3 to V_{S1} +0.2	V
CPL, IFO, PLE pin 7, 8, 10	V_I	−0.3 to 5.5	V
Outputs			
UHF, VHF, Bd I/III pin 3, 4, 5	V_Q	−0.3 to 16	V
CL (pin 6)	V_6	−0.3 to 16	V
	I_6	3	mA
$\overline{LDM}$ (pin 17)	V_{17}	−0.3 to 7.5	V
	I_{17}	3	mA
LOCK IND (pin 12)	V_{12}	−0.3 to V_{S1} +0.2	V
PD (pin 14)	I_{14}	1	mA
UD (pin 11)	V_{11}	−0.3 to 33	V
OSC (pin 13)	V_{13}	−0.3 to V_{S1} +0.2	V
	I_{13}	8	mA
Junction temperature	T_j	140	°C
Storage temperature range	T_{stg}	−55 to 150	°C
Thermal resistance (system-air)	$R_{th\,SA}$	80	K/W

Operating range

Supply voltage	V_{S1}	4.5 to 7.15	V
Input frequency	$f_{F,F}$	16	MHz
Divider factor	N	256 to 8191	
Crystal frequency	f_Q	3	MHz
Tuning voltage	V_{tun}	0.3 to 33	V
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics ($V_{S1} = 5$ V; $T_{amb} = 25$ °C)

		No. of test circuit	min	typ	max	
Supply current, pin 18	I_{S1}			20	35	mA
Oscillator output, pin 13	V_{13H}	4	4.5			V
$R_{L2} = 3{,}4$ kΩ						
OSC	V_{13L}	4			0.7	V
$R_{L2} = 3.5$ kΩ						
Signal inputs, pin 15, 16						
Input voltage	V_{15H}	1	4.1		V_{S1}+0.2	V
	V_{15L}	1	3.8		V_{S1}−0.1	V
Input current	I_{15}	1			50	µA
$V_{15} = 5$ V						
Input sensitivity (peak to peak)	$V_{15,16}$	1	300		1200	mV
Sine push-pull $f = 16$ MHz						
Bus inputs CPL, IFO, PLE, pin 7, 8, 10						
Upper threshold voltage	V_{7u}	2	1.0	1.3	1.6	V
Lower threshold voltage	V_{7l}	2	0.5	0.7	1.0	V
Hysteresis	ΔV_7	2		0.6		V
H input current	I_{7H}	2			8	µA
$V_{7H} = 5$ V						
L input current	I_{7L}	2	−50			µA
$V_{7L} = 0.4$ V						
Band selection outputs UHF, VHF, Bd I/III pins 3, 4, 5						
Reverse current	I_{3H}	3			10	µA
$V_{3H} = 15$ V						
Forward current (current drain)	I_{3L}	3	0.8		1.7	mA
$2\text{ V} \leqq V_3 \leqq 15$ V						
Clock output CL, pin 6						
H output voltage	V_{6H}	4	14			V
$V_{S3} = 15$ V						
L output voltage	V_{6L}	4			1.5	V
$R_{L1} = 6.8$ kΩ						
Tuning section V_{tun}, PD, pins 11, 14						
Tuning voltage	V_{11}	5	0.3		32.5	V
$V_{S2} = 33$ V						
Charge-pump current	I_{14}	5	−150	±100	+150	µA
PLL locked						
PLL unlocked	I_{14}	5	−450	±300	+450	µA

Characteristics ($V_{S1} = 15$ V; $T_{amb} = 25$ °C) (cont'd)

		No. of test circuit	min	typ	max	
Lock indication, pin 12						
H output voltage	V_{12H}	5	2.8			V
L output voltage	V_{12L}	5			0.4	V
Carry synchronous divider $\overline{\text{LDM}}$ pin 17 (open collector)						
Reverse current $V_{17H} = 5$ V	I_{17}	1			10	µA
L output voltage $R_L = 5$ kΩ	V_{17L}				0.4	V
Switching times						
IFO, PLE						
Set-up time	t_S	2	2	1.5		µs
Hold time	t_H	2	2	1.5		µs
CLK						
H pulse width	t_{TH}	4		8.0		µs
L pulse width	t_{TL}	4		8.0		µs
HL transition time $R_{L1} = 6.8$ kΩ	t_{THL}	4	0		0.5	µs
LH transition time $C_{L1} = 50{,}0$ pF	t_{TLH}		0		1.5	µs
CPL						
H pulse width	t_{CH}	2	2	1.5		µs
L pulse width	t_{CL}	2	2	1.5		µs
OSC						
H pulse width	t_{OH}	4	133			ns
L pulse width	t_{OL}	4			200	ns
HL transition time $R_{L2} = 3.5$ kΩ	t_{OHL}	4			20	ns
LH transition time $C_{L2} = 8$ pF	t_{OLH}	4			50	ns

Circuit description (refer to block diagram)

F, $\overline{F}$ A switchable 16/17 counter is triggered by the ECL signal inputs F/$\overline{F}$. The counter, in connection with a 4-bit and a 9-bit programmable, synchronous counter, forms a programmable, 13-bit synchronous divider using the dual-modulus technique, the 4-bit counter controlling the switchover from 16 to 17. Divider ratios of $N = 256$ to 8191 are possible. For test purposes the carry of the synchronous $\overline{LDM}$ divider is available at the $\overline{LDM}$ output (open collector). The 16-bit shift register CPL and latch is subdivided into 13 bits for storing the divider ratio N and 3 bits IFO for controlling the three band-selection outputs. The telegram is shifted in via PLE the serial data input IFO with the HL edge of the shift clock CPL when the enable input PLE is also on high level. First the complement of the divider ratio N, beginning with the LSB, is inserted in binary code, followed by the three control bits for the band-selection switching (see truth table). The 16-bit latch takes the data from the shift register when the enable input PLE is on low level.

Q1, Q2 The IC includes a crystal-controlled, 3-MHz clock oscillator. The output signal is divided down to 1.953125 kHz (reference signal) by a 1/1536 reference divider.
OSC The oscillator frequency appears at the TTL output OSC.

CL The clock of 62.5 kHz is available at the open-collector output CL.

PD The divided input signal is compared with the reference signal in a digital phase detector. If the falling edge of the input signal appears prior to the falling edge of the reference signal, the DOWN output of the phase detector turns to high level for the duration of this phase difference. In the reverse case the UP output turns to high level. If the two signals are in phase, both outputs remain at low level. The UP/DOWN outputs control the two current sources I^+ und I (charge pump). If the two outputs are low (PLL locked), the charge-pump output PD will turn to the high-impedance state (TRISTATE).

LOCK IND An L signal appears at the LOCK IND output if frequency and phase are synchronous. The current sources I^+ and I^- are then reduced from 300 to 100 µA.

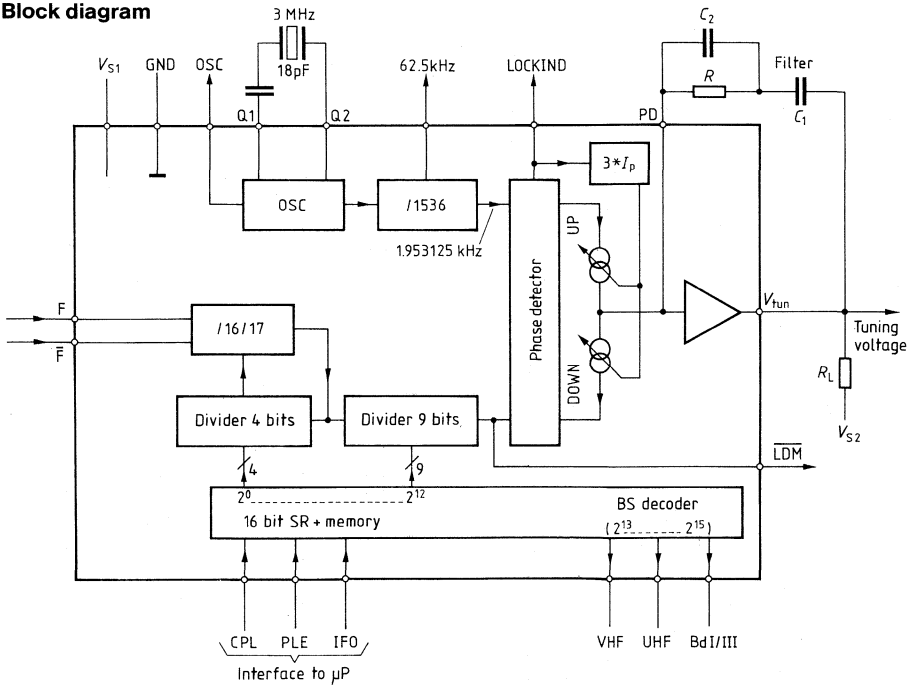
V_{tun} The current pulses generated by the charge pump are integrated to form the tuning voltage by means of an active lowpass filter (external pull-up resistor to supply V_{S2} and external RC circuitry). The dc output signal appears at V_{tun} and serves as a tuning voltage for the VCO.

UHF The band-selection outputs (UHF, VHF, Bd I/III) contain current drains with open
VHF collectors. In this way PNP transistors working as band-selection switches can be
Bd I/III connected directly without current-limiting resistors (see application circuit).

Pin configuration

Pin No.	Symbol	Function
1	Q 2	Crystal
2	Q 1	Crystal
3	UHF	} Band selection outputs
4	VHF	
5	Bd I/III	
6	CLK	Clock output
7	CPL	Clock input
8	IFO	Data input
9	GND	Ground
10	PLE	Shift register enable input
11	V_{tun}	Tuning voltage
12	LOCK IND	Lock indication output
13	OSC	Oscillator output
14	V_{PD}	Phase detector voltage
15	$\overline{F}$	Inverted input
16	F	Input
17	$\overline{LDM}$	Carry
18	V_{S1}	Supply voltage

Block diagram



Application circuit

Loop-filter calculations

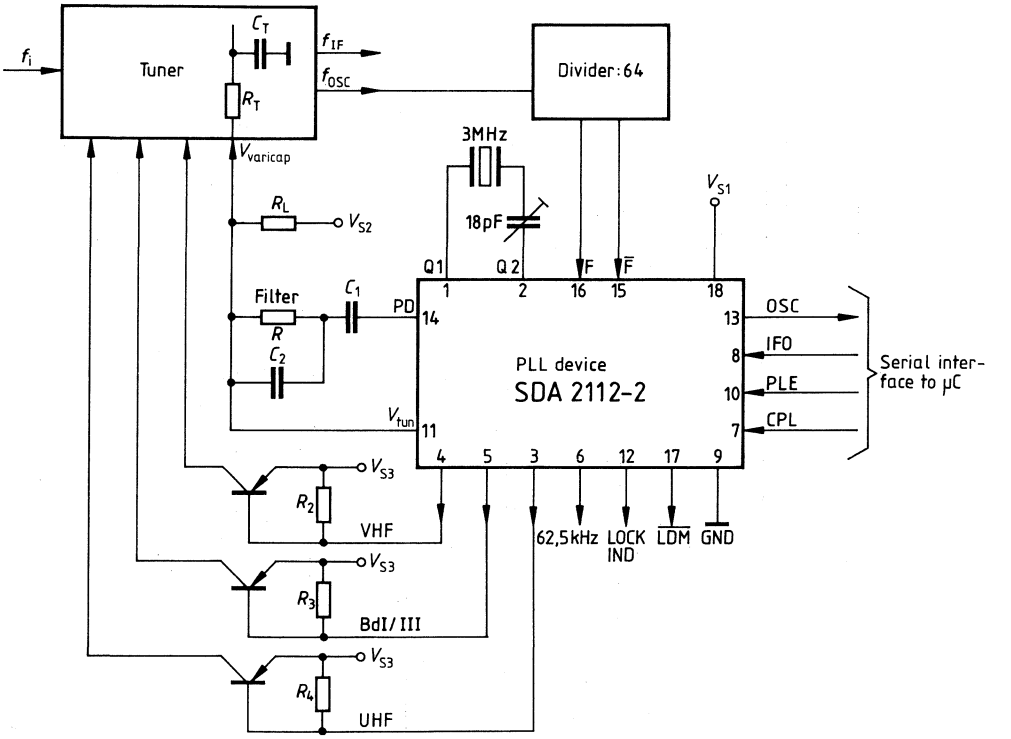
Loop bandwidth: $w_n = \sqrt{\frac{I_p \times K_{VCO}}{C_1 \times P \times N}}$

Attenuation: $a = 0.5 \times w_n \times R \times C_1$

P = prescaler
N = programmable prescaler
I_p = pump current
K_{VCO} = tuner characteristic
R, C_1 = loop filter

Example for channel 47:

P = 64 N = 5760 I_p = 100 µA K_{VCO} = 18.7 MHz/V R = 33 kΩ
C_1 = 330 nF w_n = 124 Hz f_n = 20 Hz a = 0.675
Post filter: R_t = 10 kΩ C_t = 47 nF
Standard dimensioning: $C_2 = C_1/5$
V_{S1} = 5 V V_{S2} = 33 V V_{S3} = 12 V R_2 to R_4 = 22 kΩ R_L = 22 kΩ

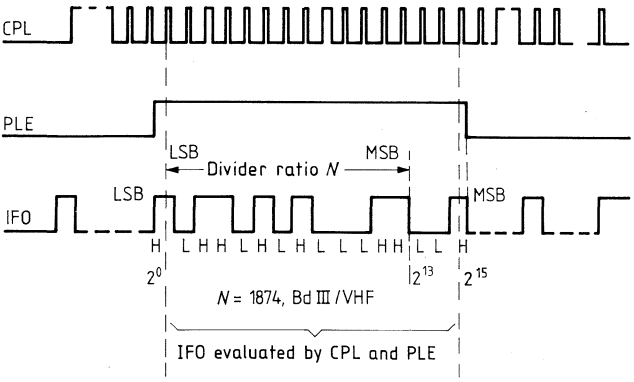


Truth table

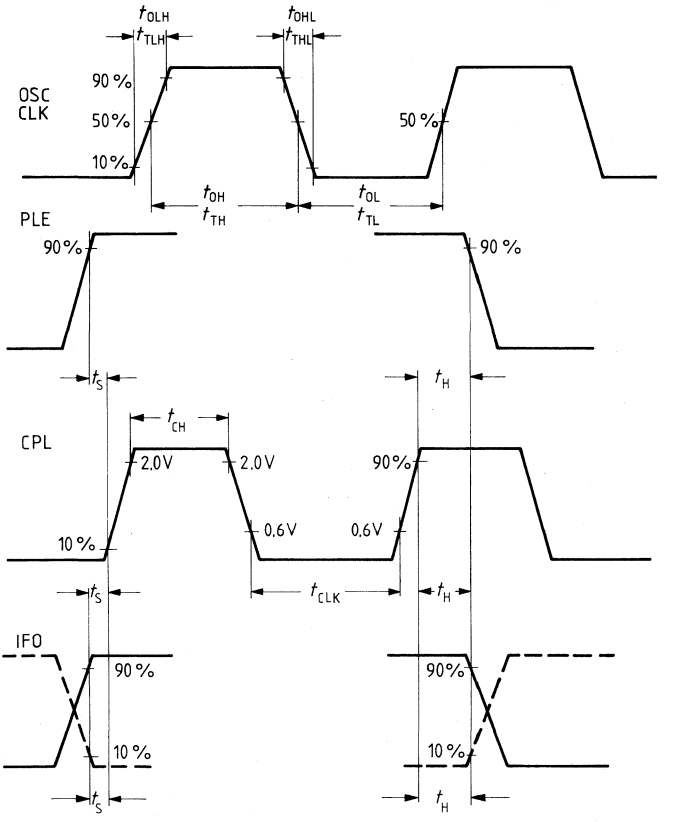
Input "IFO" bit			Outputs			Meaning
2^{13}	2^{14}	2^{15}	Bd I/III	VHF	UHF	
H	H	L	H	H	L	"UHF"
H	L	H	H	L	H	"Bd I/VHF"
L	L	H	L	L	H	"Bd III/VHF"
L	H	H	L	H	H	"Bd III/VHF"

At positive logic, the "IFO" bits $2^0 \ldots 2^{12}$ complement the dual code from divider ratio *N*.

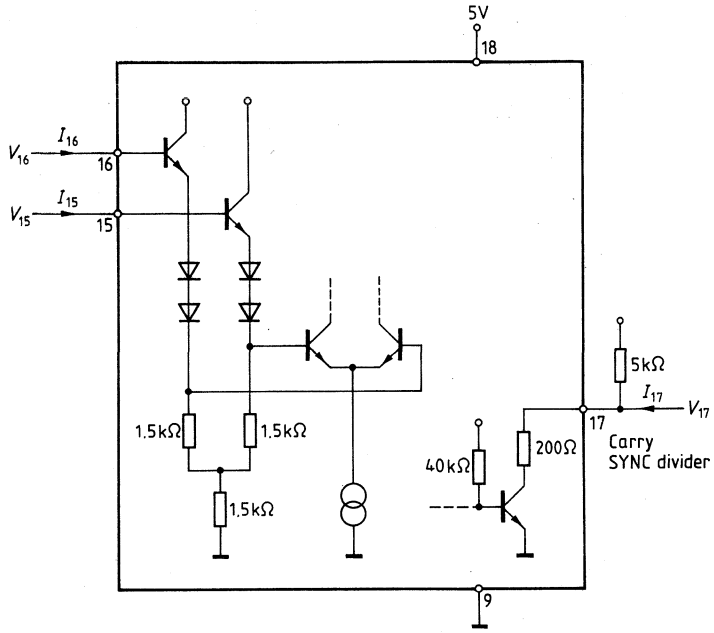
Pulse diagram

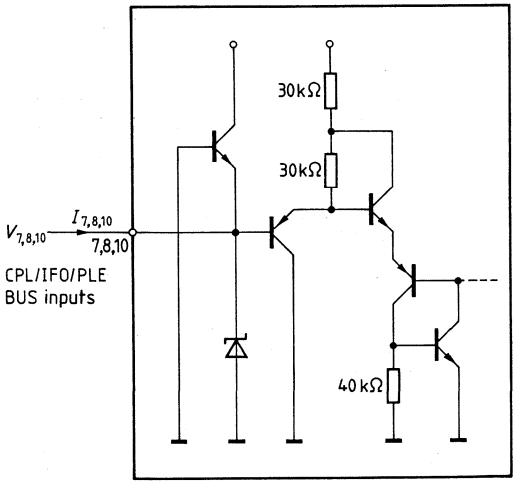


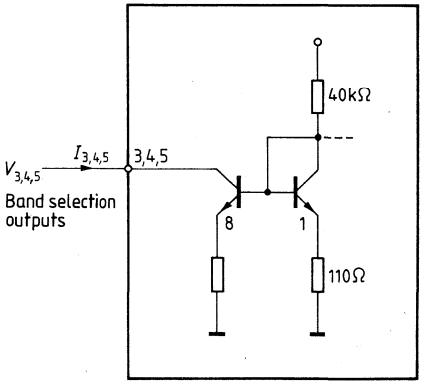
Pulse diagram



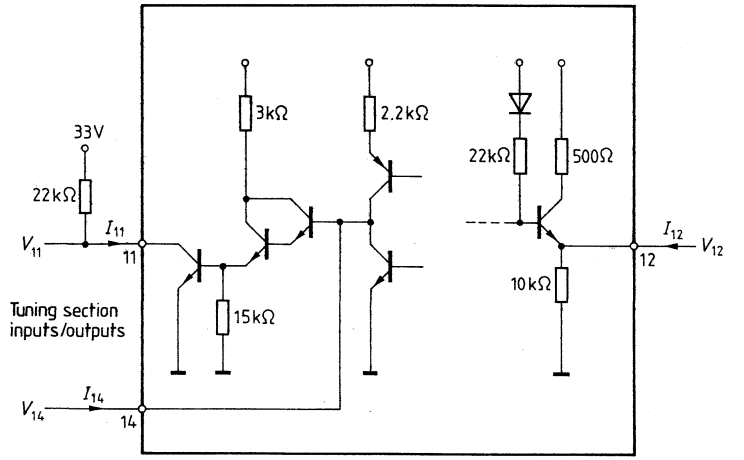
Test and measurement circuits

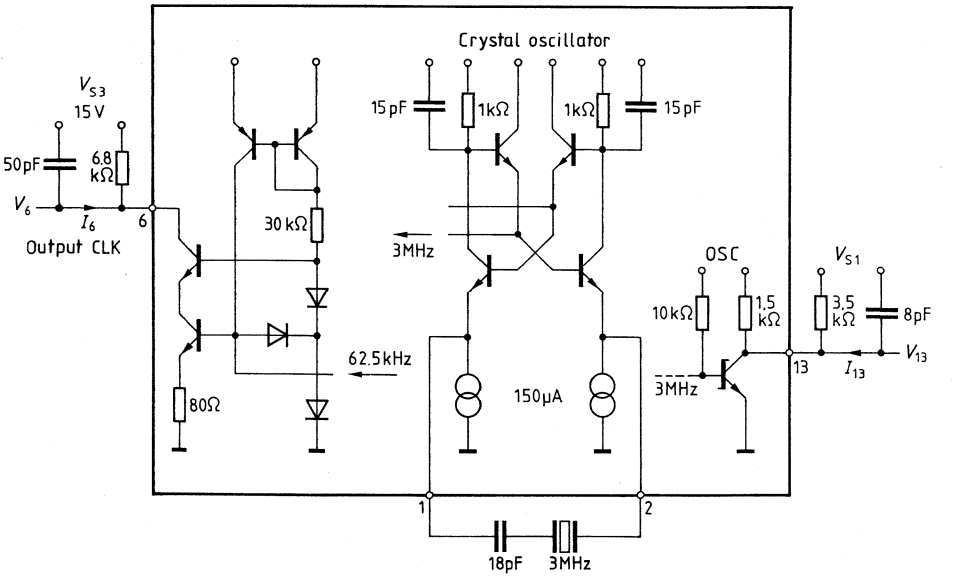






Test and measurement circuits





Infrared Diode Driver IC including Power-on Transistor for PMOS Control

SDA 2114 P

Bipolar circuit

Type	Ordering code	Package outline
SDA 2114 P	Q67000-A1859	DIP 6

The SDA 2114 P serves as a driver for IR diodes and can be controlled, e.g. by a PMOS transmitter. A switch-on transistor is available for single-channel transmitters.

Features

- Largely replaces the external circuitry of the IR transmitters
- Supplies the complete LED current, 0.5 A typical
- Minimal quiescent current consumption (1 µA)
- Simple mounting

Maximum ratings

Supply voltage	V_S	15	V
Output voltage	V_{QET}	0 to V_S	V
Output voltage	V_{QIR}	0 to V_S	V
Input voltage	V_{ETP}	0	
Input voltage	V_{IRP}	0 to V_S	V
Input current	I_{ETP}	10	mA
Output current	I_{QET}	50	mA
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	–20 to 135	°C
Thermal resistance (system-air)	$R_{th\,SA}$	120	K/W

Operating range

Supply voltage range	V_S	4 to 10	V
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics ($V_S = 6$ V; $T_{amb} = 25$ °C)

		min	typ	max	
Input current ($I_{QET} = 10$ mA)	I_{ETP}	0.1			mA
Input voltage ($I_{ETP} = 0.1 \ldots 2$ mA)	V_{ETP}			1	V
Output voltage ($I_{ETP} = 0.1$ mA) ($I_{QET} = 10$ mA)	V_{QET}			0.4	V
Input current ($I_{QIR} \geq 0.4$ A)	I_{IRP}	0.25			mA
Input current ($V_{IRP} = 5.3$ V)	I_{IRP}	0.4			mA
Input current ($V_{IRP} = 6$ V)	I_{IRP}			1.2	mA
Output current ($V_{QIR} = 1 \ldots 4$ V) ($I_{IRP} = 0{,}25 \ldots 2$ mA)	I_{QIR}		0.5		A
Saturation output voltage ($I_{QIR} = 0.3$ A)	$V_{QIR\,SAT}$			1	V
Supply current ($I_{QIR} = 0.5$ A)	I_S		10		mA
Quiescent current all inputs open	I_R		1	10	µA
Output current ($V_{QIR} = 1 \ldots 4$ V) ($I_{IRP} = 0.25 \ldots 2$ mA) ($V_S = 4$ V)	I_{QIR}	0.3	0.4		A
Output current ($V_{QIR} = 1 \ldots 6$ V) ($I_{IRP} = 0.25 \ldots 2$ mA) ($V_S = 9$ V)	I_{QIR}			0.9	A
Input current all inputs $\lvert I_{QET} \rvert < 10$ µA $I_{QIR} < 10$ µA	$\lvert I_I \rvert$			3	µA
Switch-on delay	t_1			3	µs
Switch-off delay	t_2	$t_1 + 0.1$		3	µs

Circuit description

The driver supplies a typical constant current of 0.5 A at the output QIR and is activated via the input IRP.

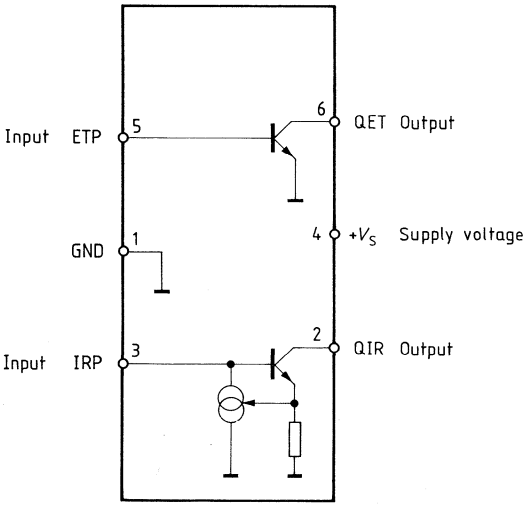
By controlling the input ETP, a current drain (rated current = 10 mA) is available at output QET.

If the current flow through the input of the driver and the switch-on transistor is inhibited, the current consumption of the IC lies at 1 µA.

Pin configuration

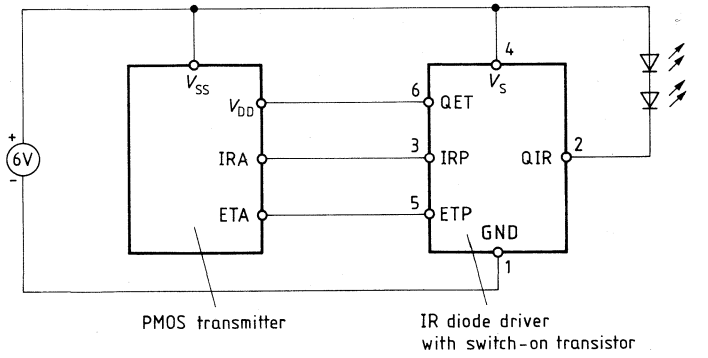
Pin No.	Symbol	Function
1	GND	Ground
2	QIR	Output of the IR driver
3	IRP	Input of the IR driver
4	V_S	Supply voltage
5	ETP	Input of the switch-on transistor
6	QET	Output of the switch-on transistor

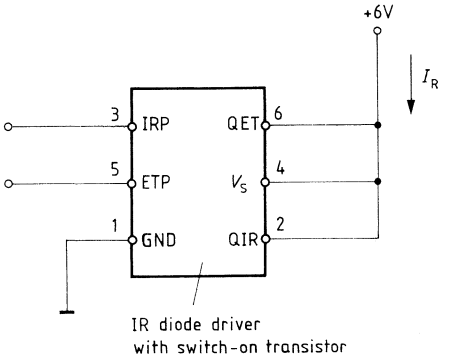
Block diagram



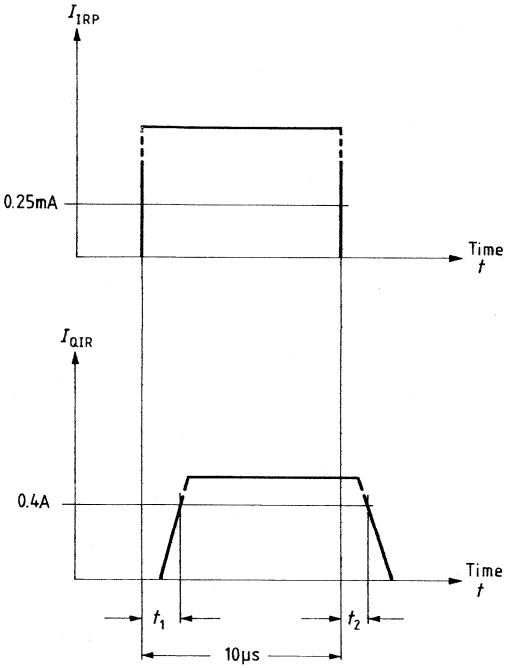
Application and measurement circuits

(IRA is an open drain output)





Pulse diagram



Preliminary data **MOS circuit**

Type	Ordering code	Package outline
SDA 2116	Q67100-A2128	DIP 8

Features

- Electrically word-organized programmable nonvolatile memory in n-channel floating-gate technology
- Organization 128 words by 8 bits each
- Supply voltage 5 V, programming voltage 24 V
- A total of 3 lines provides data transfer and chip control between processing unit and E^2PROM
- Data (8 bits), address (7 bits) and input of control information (1 bit) as well as serial data output
- Number of reprogramming cycles per address $>10^3$
- Data retention >10 years (within specified operating temperature range)
- Unlimited number of read-out procedures without refresh
- Erase and write cycle in 50 ms each

Maximum ratings

Supply voltage 1	V_{CC}	−0.3 to 6	V
Supply voltage 2	V_{pp}	−0.3 to 26	V
Input voltage	V_i	−0.3 to 6	V
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	100	K/W

Operating range

Supply voltage	V_{CC}	4.5 to 5.5	V
Ambient temperature range	T_{amb}	0 to 70	°C

Static characteristics

		min	typ	max	
Supply voltage 1	V_{CC}	4.5	5	5.5	V
Supply current 1	I_{CC}			5	mA
Supply voltage 2	V_{PP}	22.8[1]	24[1]	25.6[1]	V
Supply current 2	I_{PP}			2	mA
Inputs	V_L			0.5	V
(D, Φ, $\overline{CE}$)	V_H	3.0			V
(V_H = 5.5 V)	I_H			10	µA
Data output D (open drain)					
(V_L = 0.5 V)	I_L			0.5	mA
(V_H = 5.5 V)	I_H			10	µA
Clock pulse Φ					
High duration	Φ_H	2.5		60	µs
Low duration					
before/after Φ_H	Φ_L	5			µs
before/after $\overline{CE}$ alteration	Φ_L	5			µs
before/after D alteration	Φ_L	2.5			µs
Signal edge distance	Δt				
$\overline{CE}$ against D		2.5			µs
Erase time	t_{ET}	50			ms
Write time	t_{WR}	50			ms

1) Voltage peaks higher than the static value of V_{PP} must be avoided, e.g. by a Z diode between the inputs 6 and 1.

Data transfer and chip control

Total data transfer between processing unit and E^2PROM memory requires 3 lines, each of which controls several functions.

a) Data input D:
- bidirectional serial data transfer
- serial address input
- clocked input of control information
- control input directly

b) Clock input Φ:
- data, address, and control bit input
- data output
- start data output with data transfer from memory in shift register or start data change when reprogramming

c) Chip enable input $\overline{CE}$:
- chip reset and data input (active high)
- chip enabling (active low)

Prior to chip enabling the data address and control information will be clocked in via a bidirectional data bus. This data remains stored during reprogramming and during read until the 2nd clock pulse is generated. The following data formats have to be applied:

a) Memory read: one 8 bit control word, thereof
- 7 address bits A0 to A6 (A0 as LSB first)
- 1 control bit, SB = "0", after A6

b) Memory change (erase and/or write)
16-bit input information, thereof
- 8-bit D0 to D7 new memory information (D0 as LSB first)
- 7-bit A0 to A6 address information (A0 as LSB after D7 first)
- 1-bit control information, SB = "1", after A6

Read (figure 1)

After data input and with SB = "0" the read operation of the selected word address is started by the falling edge of $\overline{CE}$ from "1" to "0". The information on the data line is disregarded during chip activation.

With the aid of the first clock pulse after $\overline{CE}$ = "0" the data word is transferred out of the selected memory address into the shift register. After the first Φ-pulse has been terminated, the data output becomes low-ohmic and the first data bit D0 can be read. With each following clock pulse a further data bit will be passed to the output. The data line turns again high-ohmic at the rising edge of $\overline{CE}$ going from "0" to "1".

Reprogramming (figure 2)

A complete reprogramming operation normally consists of an erase cycle and a following write cycle. During erasing every bit of the selected word will be brought into the common "1" status, during writing the "0" states are generated depending on the information of the shift register.

A reprogramming cycle starts if, after the data input at chip enable, an information SB = "1" is set in the corresponding shift register location. Whether an erase or a write cycle is executed, depends again on the information of the data line D during chip activation.

Erasing into the "1" status requires a "1" at the data input during the falling edge $\overline{CE}$ to low. Should, however, a write cycle into "0" status be started, then a "0" must be on the data line during chip activation.

To start programming, a start pulse must be applied to clock input Φ, and the control information at D must remain stable until its rising edge. The active data change starts with the falling edge of this start pulse. The programming cycle will be terminated by a reset of the chip activation, i.e. by applying $\overline{CE}$ = "1".

The reprogramming of a word begins by starting and processing an erase cycle. $\overline{CE}$ = "1" ends the erase cycle. The control bit in the shift register SB = "1", which is also required for the write cycle, remains stable even after termination of the erase cycle. In order to write the selected word, the data line D has to be switched from "1" to "0" the chip must be activated again by $\overline{CE}$ = "0" and finally by means of the start pulse, the data change can be started.

The erase and write function can be performed separately. In order to obtain a stable "1" in all 8 bits of the selected memory address during erasing, a data word featuring 8 times "1" must be read in prior to the erasing process. In case a word is written into a previously not erased memory cell the "0" status of the previous and the new information will be added up.

RESET and supply voltages

A not addressed memory automatically remains in reset position through $\overline{CE}$ = "1". All flipflops in the process control section are reset. The information in the shift register, however, remains and will only be changed by shifting the data.

If the defined position of the signal levels (quiescent state $\overline{CE}$ = high, Φ = low) cannot be ensured at switching on or off the supply voltage, data losses upon unintended decoding of a programming instruction can be avoided by switching V_{PP} on after V_{CC} and off prior to V_{CC}.

Figure 1: Read cycle (1 Kbit E²PROM)

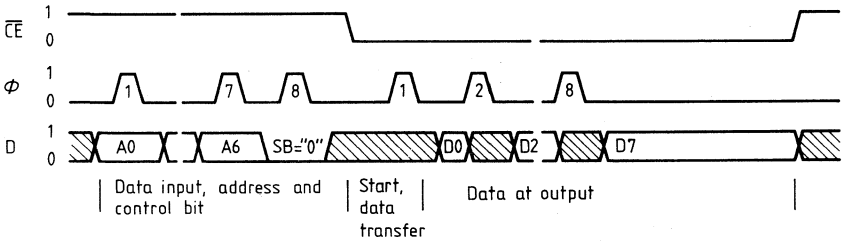
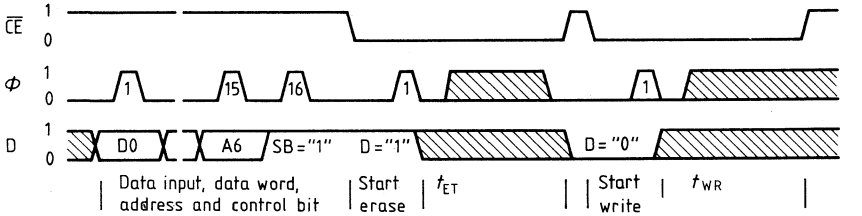


Figure 2: Reprogramming cycle (1 Kbit E²PROM)



Pin configuration

Pin No.	Symbol	Function
1	V_{SS}	Ground
2	$\overline{CE}$	Chip enable
3	V_{CC}	Supply voltage 5 V
4	D	Data input/output
5	Φ	Clock input
6	V_{PP}	Programming voltage 25 V
7	TP	Test input, at V_{SS}
8	TG	Test input, remains open

Bipolar circuit
MOS handling

Type	Ordering code	Package outline
SDA 2120	Q 67000-A 1953	DIP 22

The SDA 2120 contains the complete digital section (reference oscillator, 20-bit shift register with memory, programmable divider, band select outputs as well as a phase detector, two charge pumps, one current multiplier, and two amplifiers) for tuning an AM/FM receiver by PLL frequency synthesis.

A serial interface facilitates connection to a microprocessor. The microprocessor will load the divider, the band select outputs, and the current multiplier with the suitable information.

Features

- Integrated prescaler
- Switch-selectable from AM to FM
- High frequency resolution FM = 12.5 kHz, AM = 0.5 kHz

Maximum ratings

Supply voltage	V_S	7.5	V
Tuning supply voltage	V_{SAM}/V_{SFM}	32	V
IFO, PLE, CPL	V_{iH}	5.5	V
Band select: UKW, SW, MW, LW	V_{BS}	18	V
AM, FM	$V_{AM/FM}$	5.5	V
F	V_F	5.5	V
Input current amplifier	I_{iV}	500	µA
Output current amplifier	$I_{DAM/FM}$	7	mA
Junction temperature	T_j	140	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	65	K/W

Operating range

Supply voltage	V_S	4.5 to 5.5	V
Ambient temperature range	T_{amb}	−25 to 85	°C
Resistance for charge pump current[1])	R_I	> 100	kΩ
Input frequency input AM	f_{iAM}	10	MHz
Input frequency input FM	f_{iFM}	120	MHz
Prescaler factor LW/MW	$N_{LW/MW}$	2 / 16383	
Prescaler factor SW/UKW	$N_{SW/UKW}$	4097 / 16383	

1) Multiplication factor $M = 15$

Characteristics ($V_S = 5$ V; $T_{amb} = 25$ °C)

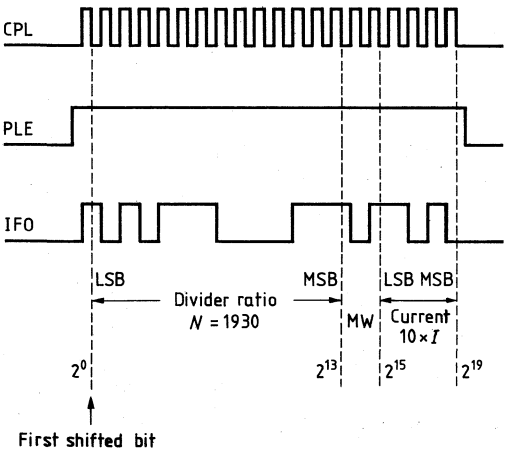
		min	typ	max	
Supply current	I_S		60		mA
L tuning voltage V_{tunAM}/V_{tunFM} ($I_{DL} = 2.5$ mA)	V_{DL}			0.5	V
H tuning voltage V_{tunAM} ($V_{S2} = 32$ V)	V_{tunHAM}	30			V
H tuning voltage V_{tunFM} ($V_{S2} = 32$ V)	V_{tunHFM}	30			V
Sensitivity input AM ($f = 10$ MHz)	$V_{iAM\,rms}$		10		mV
Sensitivity input FM ($f = 120$ MHz)	$V_{iFM\,rms}$		20		mV
Input resistance input AM ($f = 10$ MHz; $V_{iAMrms} = 100$ mV)	R_{iAM}		1		kΩ
Input resistance input FM ($f = 120$ MHz; $V_{iFMrms} = 100$ mV)	R_{iFM}		0.5		kΩ
Input capacitance, input AM/FM	C_i		4		pF
Inputs IFO, PLE, CPL					
Upper threshold voltage	V_{Su}	2.0[1]			V
Lower threshold voltage	V_{Sl}			0.8[1]	V
H input current	I_{iH}			8	μA
L input current	I_{iL}			−50	μA
BS outputs: UKW, SW, MW, LW					
($V_{pp} = 15$ V)	I_{qH}			10	μA
($0.5\ V \leqq V_{pp} = 15$ V)	I_{qL}	0.8	1.2	3.0	mA
Oscillator output F					
($I_{FH} = -100$ μA)	V_{qFH}	4.5			V
($I_{FL} = 100$ μA)	V_{qFL}			0.7	V
Residual ripple of the tuning voltage ($f = 0$–1 kHz, test bandwidth 10 Hz)	V_{tunAM}		5		μV
($f = 1$–50 kHz, test bandwidth 100 Hz)	V_{tunFM}		1		μV
Charge pump output current AM/FM ($R_i = 130$ kΩ, $M = 15$, I_{qAI} tested against 2.5 V) tristate	I_{qAI}		±500		μA
			±5		nA
Switching times					
IFO, PLE					
Set-up time for enable	t_{SE}	0.3			μs
Set-up time for data	t_{SD}	0.4			μs
Hold time for enable	t_{HE}	3			μs
Hold time for data	t_{HD}	3			μs
CPL					
H pulse width	t_{CH}	2			μs
L pulse width	t_{CL}	2			μs
F					
H pulse width	t_{FH}	200			ns
L pulse width	t_{FL}			300	ns
H/L transition time ($C_{L2} = 10$ pF)	t_{FHL}			20	ns
L/H transition time ($C_{L2} = 10$ pF)	t_{FLH}			50	ns

1) Values apply throughout the operational range.

Truth table

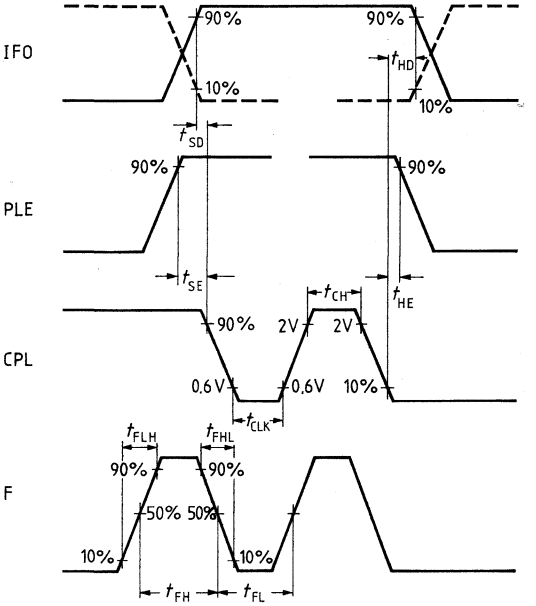
Function	"IFO" 2^{14}	bit 2^{15}	Band select outputs LW	MW	SW	UKW	f_{ref}/kHz	Active input	Active output
LW	L	L	H	H	H	H	0.5	AM	AI AM
MW	L	H	H	L	H	H	0.5	AM	AI AM
SW	H	L	H	H	L	H	0.5	AM	AI AM
UKW	H	H	H	H	H	L	12.5	FM	AI FM

Pulse diagram



Pulse diagram

Set-up and hold times



Circuit description

The component contains a 14 bit programmable synchronous divider (% P, % M, % S), which divides the frequency of a signal pending at input AM, or FM resp. by the factor N=2...16383 (LW/MW), or N = 4097...16383 (SW/VHF). The buffered inputs AM and FM can be directly connected to the VCO via capacitors due to their own prevoltage generation.

The input sensitivity of the inputs is 10 mV_{rms} (AM) or 20 V_{rms} (FM). The frequency divider input can be switched optionally to AM or FM per software switch. While the LW/MW signal is divided into a pure synchronous divider, the SW/VHF signal is divided into a modulo two divider followed by a synchronous divider. The shift register with latch, with a depth of 20 bits, is divided into 14 bits to store the divider ratio N of the synchronous divider; 2 bits to control the four band select outputs (VHF, SW, MW, LW); 4 bits for the current multiplier to select the optimum current for the charge pump.

The divider ratio N, the band selection, as well as the information for the current multiplier are loaded into the 20 bit shift register via the serial data input IFO. First, the complement of the divider ratio, beginning with the least significant bit, is loaded in a binary encoded form. This is followed by the band select control bits SB0 und SB1 (refer to table), finished by the information bits for the current multiplier. During FM operation, they are loaded in binary encoded form beginning with the LSB, during which the bit sequence 0000 is not permissible. During AM operation, the complement of the information bit is loaded in binary encoded form beginning with the LSB, during which the bit sequence 1111 is not permissible. The information is loaded with the HL slope of the shift pulse CPL. Acceptance of the data at the IFO input can only take place during the H state of the enable input PLE. The 20 bit latch accepts the data from the shift register during the L state of the enable input PLE. The component is equipped with its own crystal-controlled 4 MHz pulse oscillator.

A square-wave signal of 2 MHz derived from the pulse oscillator is available at output F, which can be used for the synchronization of peripheral devices (e.g. microprocessor). The output F is to be connected to ground in order to provide a high signal-to-noise ratio. The oscillator output signal (f_{OSC} = 4 MHz) is divided down to 0.5 kHz or 12.5 kHz respectively, by a switch-selectable reference divider (reference signal). The reference divider is switched by the same signal that also switches the inputs. The divided input signal is compared with the reference signal in a digital phase detector. If the falling edge of the divided input signal appears prior to the falling edge of the reference signal, the DOWN output of the phase detector goes into the H state for the duration of the phase difference. In the opposite case, the output UP goes into the L state. If both signals are in phase, the DOWN output remains in the L state and output UP in the H state.

The outputs UP/DOWN control the two current sources I^+ and I^- (charge pump). If output UP is in the L state, current source I^+ is activated; if output DOWN is in the H state, current source I^- is in effect. If DOWN is in the L state and UP is in the H state, the charge pump output changes into a high-ohmic state (TRI STATE). The current pulses generated by the charge pump are integrated with the aid of an active low pass (external FET op amp with *RC* circuitry). The DC output signal of the low pass is available at the FET op amp output and serves as tuning voltage for the VCO. If there are minor requirements to be met regarding the signal-to-noise ratio, an internal amplifier with a series-connected external darlington transistor can be used instead of the external FET op amp. The output stage of the internal amplifier comprises a transistor with open-collector output. The external collector resistor can then be connected to voltages up to 30 V. The output transistor is dimensioned such that a voltage drop of 0.5 V occurs at a 2.5 mA collector current.

The component contains two separate charge pumps and two separate amplifiers. Only one charge pump is active at a time. The switch-over is achieved by the same signal that also switches the AM/FM inputs. Thus, separate low passes can be set up for AM and FM. The output current of both charge pumps (source current = sink current) is $M \times I$. M is the multiplication factor that is given by the information bits for the current multiplier, M being an integer and $1 \leq M \leq 15$. I is the basic current of the charge pump that is set by means of an external resistor between pin I_{ref} and V_S. As the software monitors the current, a fast transient response of the PLL during band limit peaks and range changes (recharging the low pass) can be achieved, as well as a high signal-to-noise ratio in the steady state. The delay time between phase detector input and charge pump output is typically 20 ns. The phase detector with charge pump gain depends on the selected charge pump output current and is calculated as follows:

$$K_D = \frac{2\,I}{4\,\pi}\left[\frac{\mu A}{rad}\right].$$

The wiring of the charge pump output AI has to ensure that the DC voltage value at the output varies only between 1.2 V and 3.8 V (e.g. by applying a reference voltage of approx. 2.5 V when using the external operational amplifier. The band select outputs contain current drains (I_{qL} = 0.8 to 3.0 mA) with open collectors, in order to be able to switch voltages greater than the supply voltage of the component (5 V). Thus the transistors, operating as band select switches, can be directly driven without current limiting resistors (refer to application circuit).

During operation, pin 2 (N.C.) must be connected to ground.

Supplements to the circuit description

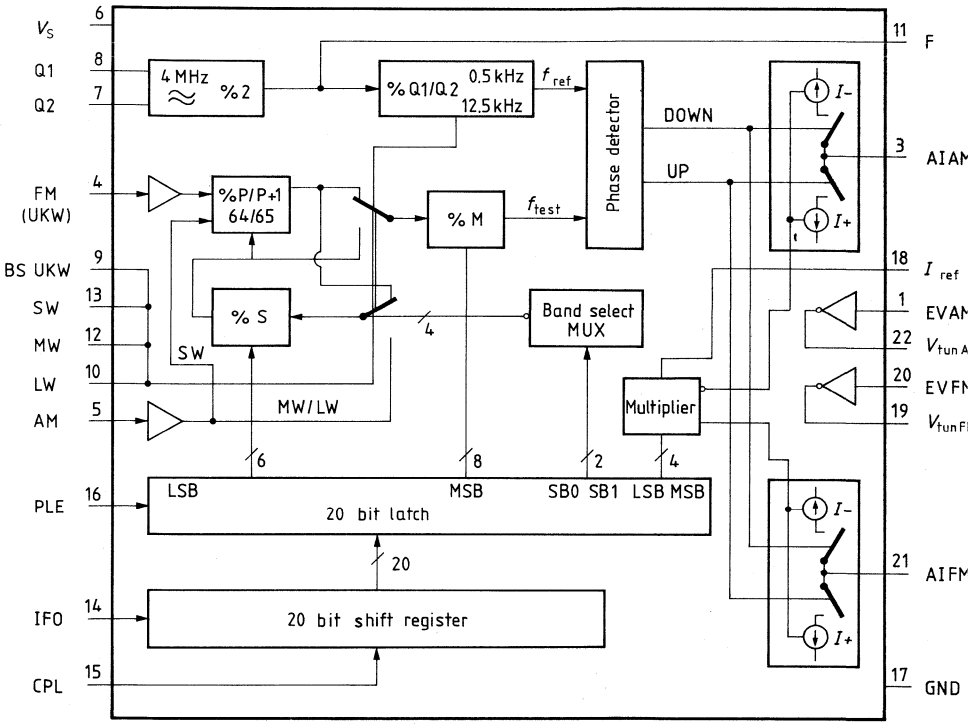
Relationship between IFO bits of current multiplier and multiplication factor for the output current of the charge pump.

IFO BIT				Multiplication factor *M*	Multiplication factor *M*
2^{16}	2^{17}	2^{18}	2^{19}	FM	AM
L	L	L	L	0	15
H	L	L	L	1	14
L	H	L	L	2	13
H	H	L	L	3	12
L	L	H	L	4	11
H	L	H	L	5	10
L	H	H	L	6	9
H	H	H	L	7	8
L	L	L	H	8	7
H	L	L	H	9	6
L	H	L	H	10	5
H	H	L	H	11	4
L	L	H	H	12	3
H	L	H	H	13	2
L	H	H	H	14	1
H	H	H	H	15	0

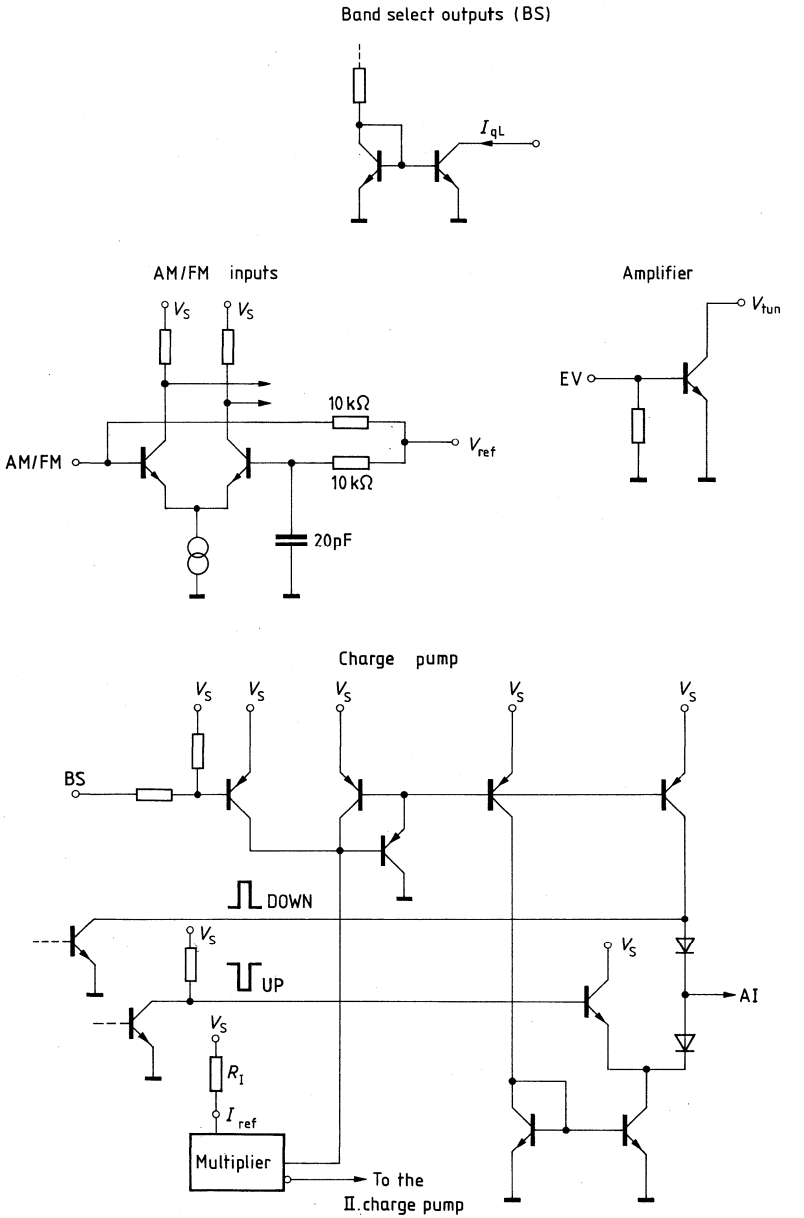
Pin configuration

Pin No.	Symbol	Function
1	EV AM	Amplifier input AM
2		N.C.
3	AI AM	Charge pump output AM
4	FM	Signal input VHF
5	AM	Signal input SW/MW/LW
6	V_S	Supply voltage
7	Q2	Crystal
8	Q1	Crystal
9	UKW	Band select output VHF
10	LW	Band select output LW
11	F	Oscillator output
12	MW	Band select output MW
13	SW	Band select output SW
14	IFO	Data input
15	CPL	Shift register input
16	PLE	Enable input for shift register
17	GND	Ground
18	I_{ref}	Current adjustment for charge pump
19	$V_{tun\,FM}$	Tuning voltage FM
10	EV FM	Amplifier input FM
21	AI FM	Charge pump output FM
22	$V_{tun\,AM}$	Tuning voltage AM

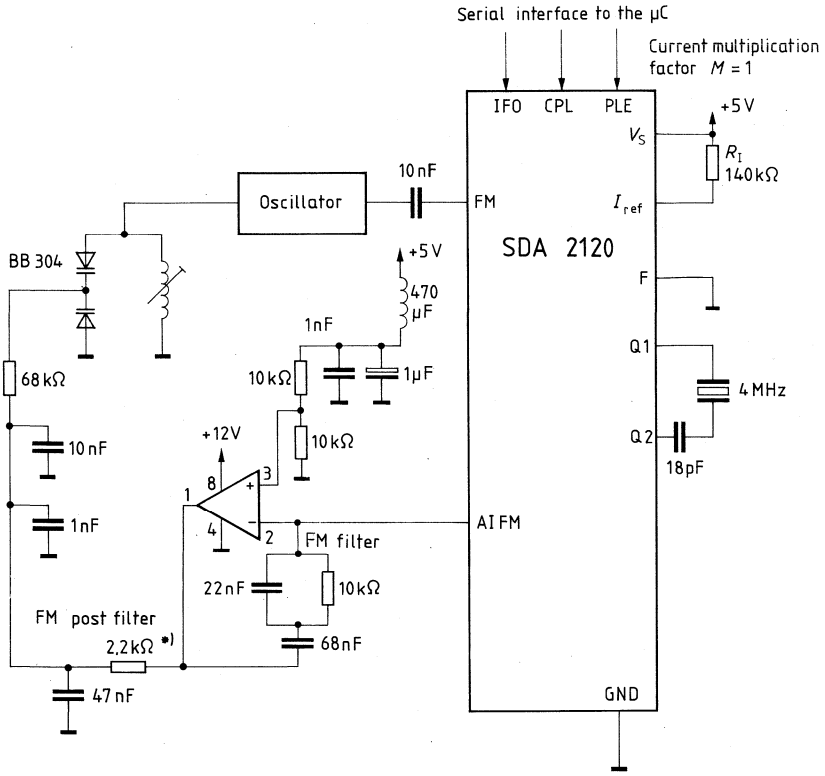
Block diagram



Circuitry of inputs and outputs (schematic)

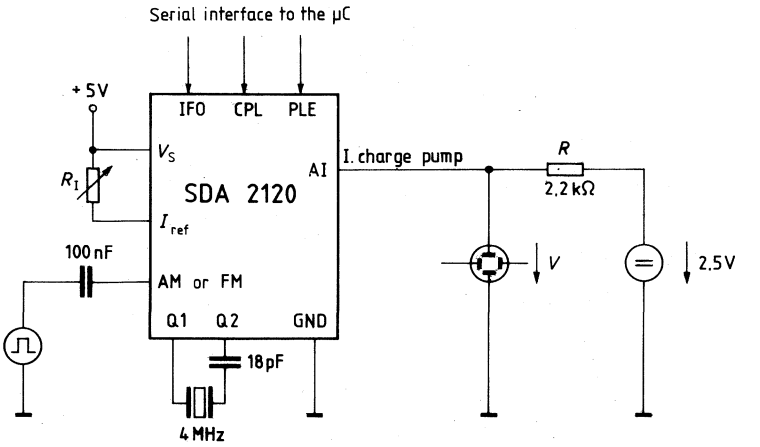


Test circuit for residual ripple of the FM tuning voltage



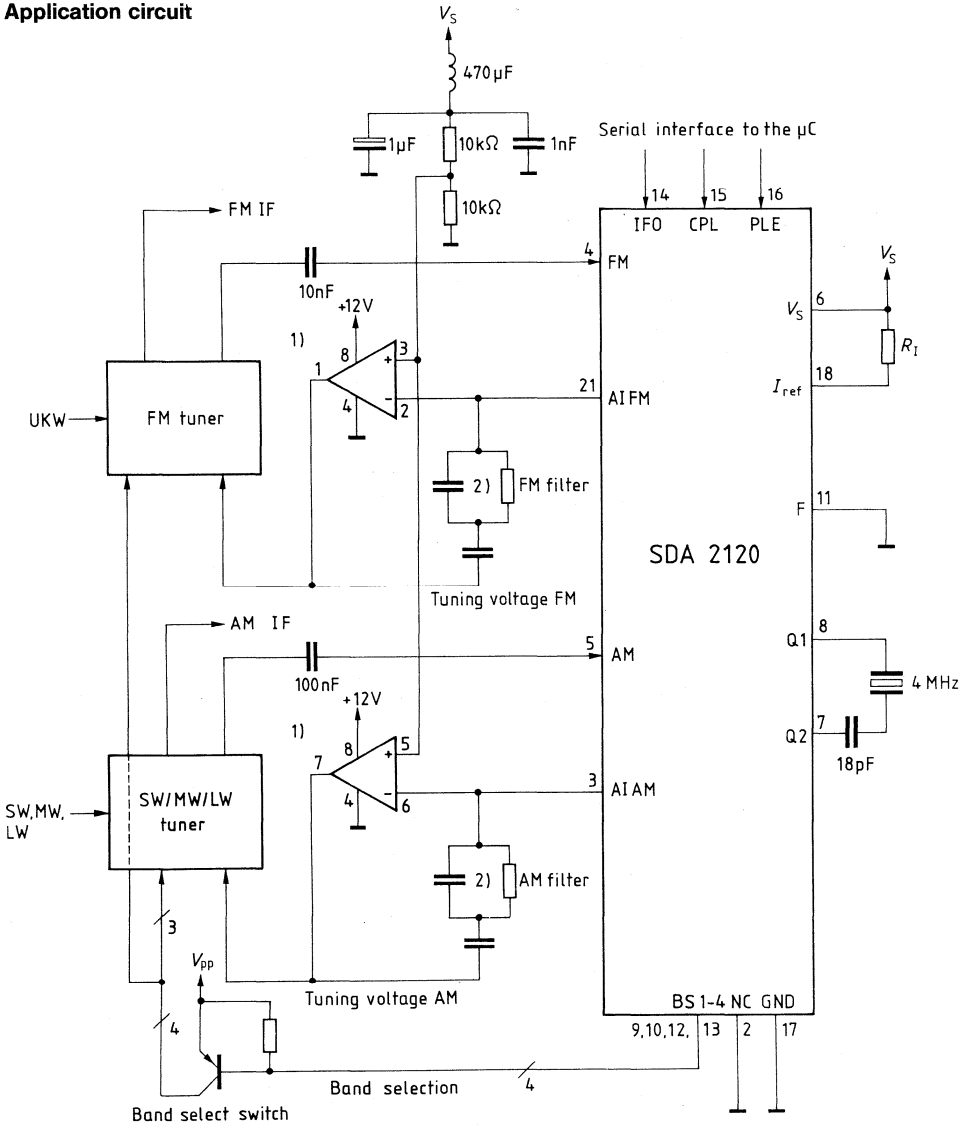
*) The mentioned filter constants are only approximate values. They have to be matched to the actual tuner by the user.

Test circuit for charge pump output current



To activate the "charge pump", there must be a difference between the frequency of the AM/FM inputs and the frequency of the µC.

Application circuit



1) Double FET operating amplifier: MC 34002, CA 3240, TL 082, LF 353 or similar types.
2) The filter values must be matched to the actual tuner by the user.

Bipolar IC

Type	Ordering code	Package outline
SDA 2131	Q67000-A2044	DIP 22

The SDA 2131 includes a static display driver for 16 LEDs featuring a 10 mA output current, each. The serial data interface enables a simple connection to the microcomputer.

Features

- Integrated load resistances, thus few external components are required
- Number of LEDs software-selectable
- Blanking capability through DC-controlled input
- Simple connection to a microcomputer

Maximum ratings

Supply voltage range	V_{S7}	−0.3 to 7	V
Input voltage range	$V_{I4,5,6}$	−0.3 to 7	V
Output voltage range (outputs blocked) (pins 1 to 3, 9 to 16, 18 to 22)	V_{qH}	−0.3 to 7	V
Input voltage C range	V_{C8}	−0.3 to V_S	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	R_{thSA}	65	K/W

The anode voltage of the LEDs and the number of simultaneously active outputs should be selected so that a total power dissipation of 800 mW in the IC is not exceeded.

Operating range

Supply voltage range	V_{S7}	4.5 to 5.5	V
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics ($V_S = 5$ V; $T_{amb} = 25$ °C)

		min	typ	max	
Supply current (all LEDs ON) ($I_q = 10$ mA)	I_{S7}		10	15	mA
Quiescent current ($I_q = 0$; C = "L")	I_{S7}		2.5	3.5	mA
Switching voltage	$V_{S4,5,6}$	0.8	1.4	2.0	V
H input current ($V_H = 5.5$ V)	$I_{H4,5,6}$			1	µA
L input current ($V_L = 0.4$ V)	$-I_{L4,5,6}$			10	µA
Output current ($V_q = 2.9$ V) (pins 1 to 3, 9 to 16, 18 to 22)	I_q	8	10	12.5	mA
Output leakage current ($V_q = V_S$) (pins 1 to 3, 9 to 16, 18 to 22)	I_{ql}			10	µA
Switching voltage C	V_{S8}	1.5	2.1	2.7	V
H input current C ($V_{H8} = 5$ V)	I_{H8}		0.6	0.9	mA
L input current C ($V_{L8} = 0$ V)	$-I_{L8}$			1	µA
H input current C (at switching voltage)	I_{H8}			15	µA

Switching times

CLK (pin 5)	H pulse width	t_{HCLK}	1			µs
	L pulse width	t_{LCLK}	2			µs
	Set-up time	t_{SCLK}	0			µs
	Hold time	t_{hCLK}	0			µs
D (pin 4)	Set-up time	t_{SD}	0.5			µs
	Hold time	t_{hD}	0.5			µs
E (Pin 6)	H pulse width	t_{HE}	50			µs
	L pulse width	t_{LE}	0.5			µs
	Set-up time	t_{SE}	1.5			µs
	Hold time	t_{hE}	1			µs
A	delay time	t_A	10			µs

Circuit description

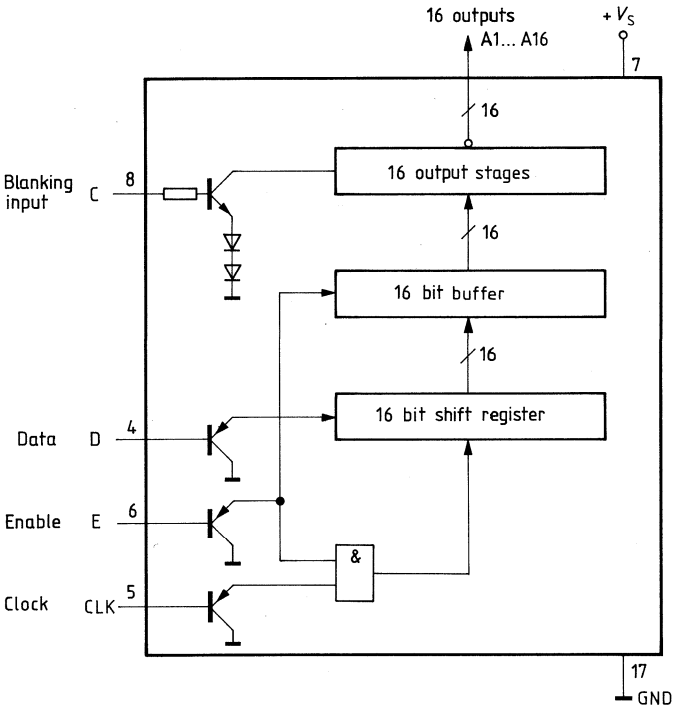
A serial interface consisting of data input D, enable input E, and clock input CLK, to connect the IC to a microprocessor. The 16 bit information ("H" at input D corresponds to the current flow at outputs A1 to A16) is loaded into a 16 bit shift register via the serial data input, beginning with LSB. Data transfer is initiated by the HL slope of the clock pulse at CLK. The data transfer D can take place only during the H state of the enable input E. A buffer accepts the data from the shift register during the HL slope of the enable input. The buffer directly drives the outputs A1 to A16.

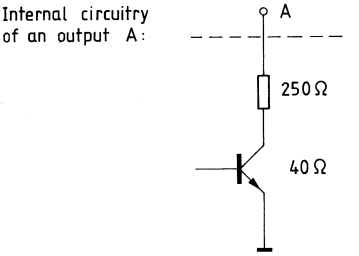
The output is limited by an internal resistor of 290 Ω.

Through input C the outputs can be switched off ($V_{C8} = 0$ V).

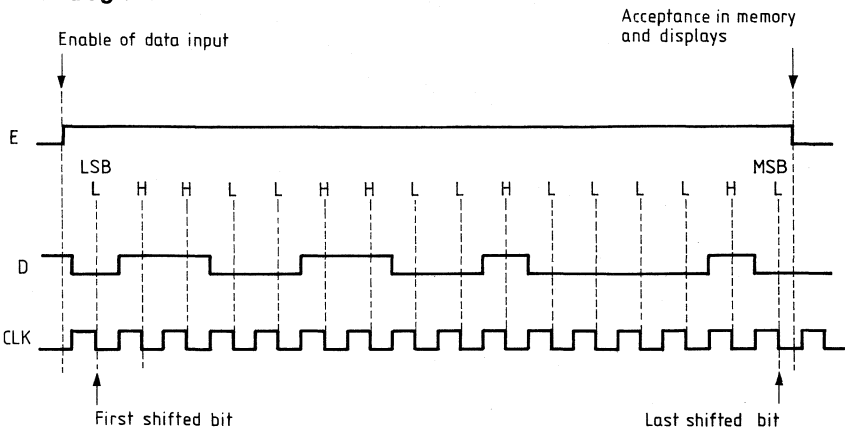
The inputs D, E, and CLK, and the input C are TTL-compatible.

Block diagram





Pulse diagram

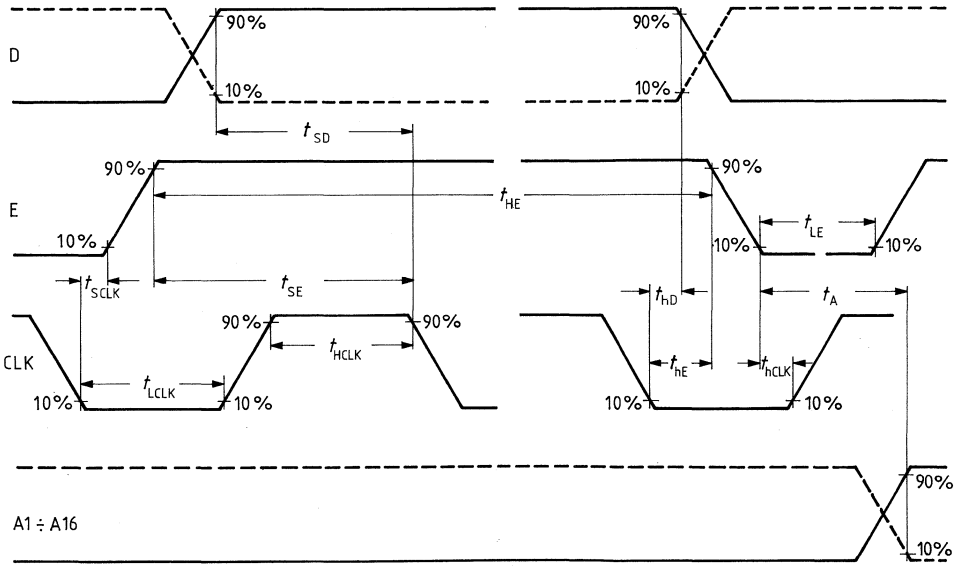


Memory contents after the falling edge of E

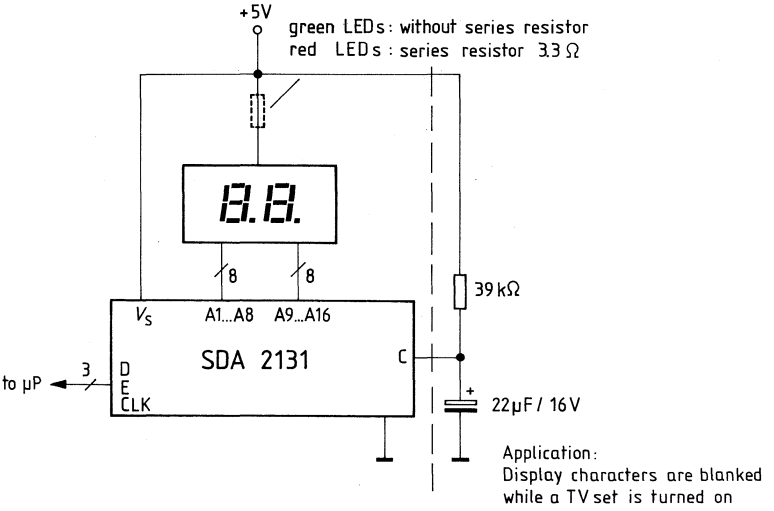
LSB MSB
L H H L L H H L L H L L L L H L

The first information shifted to D with CLK is displayed at A1.

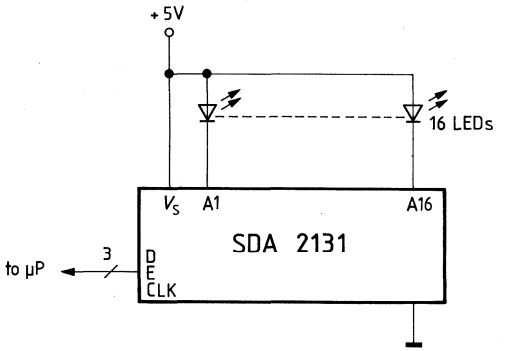
Pulse diagram



Application circuit 1
2 digit 7-segment display



Application circuit 2
Point display (1 of 16 diodes illuminated)



Pin configuration

Pin No.	Symbol	Function
1	A14	Output 14 for LED cathode
2	A15	Output 15 for LED cathode
3	A16	Output 16 for LED cathode
4	D	Input for data
5	CLK	Input for clock
6	E	Input for enable
7	V_S	Supply voltage
8	C	Input for blanking
9	A1	Output 1 for LED cathode
10	A2	Output 2 for LED cathode
11	A3	Output 3 for LED cathode
12	A4	Output 4 for LED cathode
13	A5	Output 5 for LED cathode
14	A6	Output 6 for LED cathode
15	A7	Output 7 for LED cathode
16	A8	Output 8 for LED cathode
17	GND	Ground
18	A9	Output 9 for LED cathode
19	A10	Output 10 for LED cathode
20	A11	Output 11 for LED cathode
21	A12	Output 12 for LED cathode
22	A13	Output 13 for LED cathode

Preliminary data

Bipolar circuit
MOS handling

Type	Ordering code	Package outline
SDA 2201	Q 67000-H 2428	DIP 8

The SDA 2201 contains an integrated preamplifier and an ECL divider with a divider ratio of 1 : 64 and symmetrical ECL push-pull outputs. The frequency range covers up to 1.1 GHz. The component is intended for use in TV receivers with frequency selection according to the frequency synthesis concept.

Features

- Low power consumption
- Few external components
- Symmetrical push-pull input

Maximum ratings

Supply voltage	V_S	6	V
Input voltages (peak-to-peak)	V_{i2}, V_{i3}	2.5	V
Divider outputs	V_{q6}, V_{q7}	V_S −2 to V_S	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	R_{thSA}	115	K/W

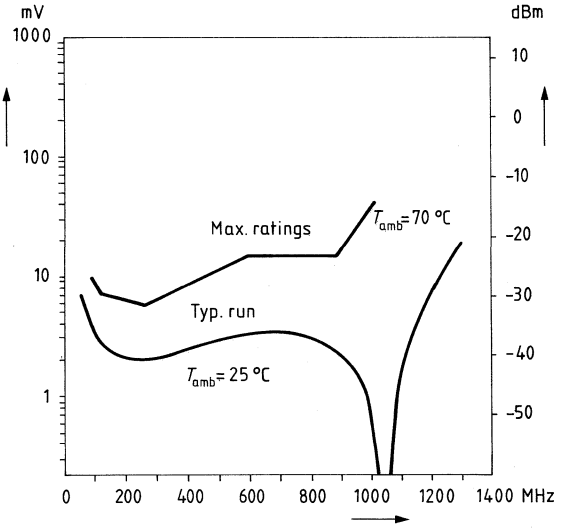
Operating range

Supply voltage range	V_S	4.5 to 5.5	V
Input frequency range	f_{i2}	80 to 1100	MHz
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics (V_S = 4.7 to 5.5 V; T_{amb} = 0 to 70 °C)

		min	typ	max	
Current consumption inputs blocked, outputs free	I_S			80	mA
Input level ("input sensitivity")	V_{i1}				
80 MHz		−27		3	dBm
120 MHz		−30		3	dBm
250 MHz		−32		3	dBm
600 MHz		−23		3	dBm
900 MHz		−23		3	dBm
1000 MHz		−15		3	dBm
Output voltage swing (peak-to-peak) C_{load} = 15 pF	V_{q1}, V_{q2}	0.5	1.0		V

Typical input sensitivity of the divider



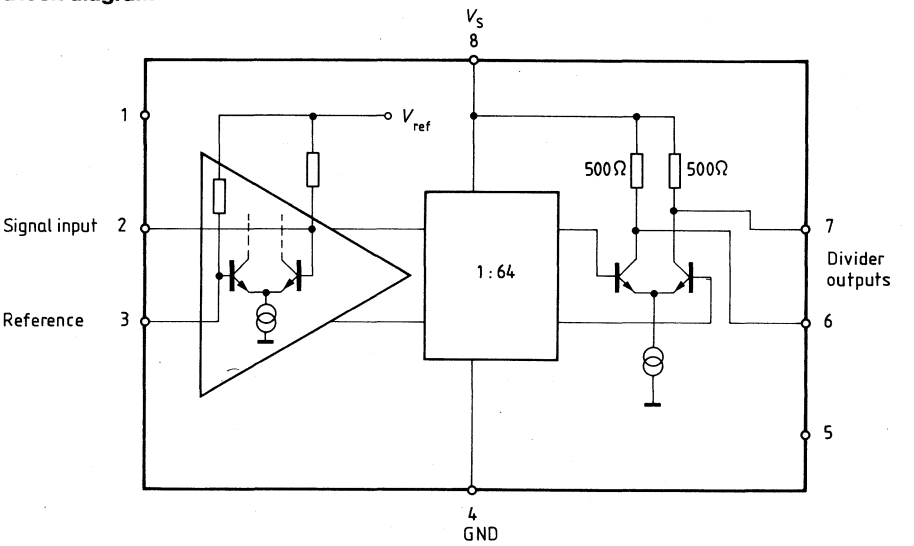
Circuit description

The IC includes an amplifier provided with symmetrical pull-push inputs. When driving the signal inputs in an asymmetrical mode, the reference input should be grounded by a capacitor with low series inductance.

The integrated divider circuit consists of several status-controlled master slave flipflops with a 1:64 divider ratio.

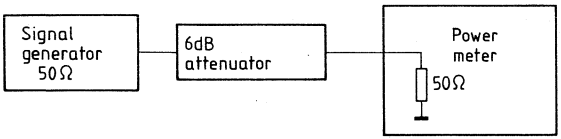
The symmetrical push-pull outputs of the divider have an internal resistance of 500 ohms. The DC voltage level is connected to the supply voltage $+V_S$ (high = $+V_S$); typical output swing is 1 V (peak-to-peak).

Block diagram

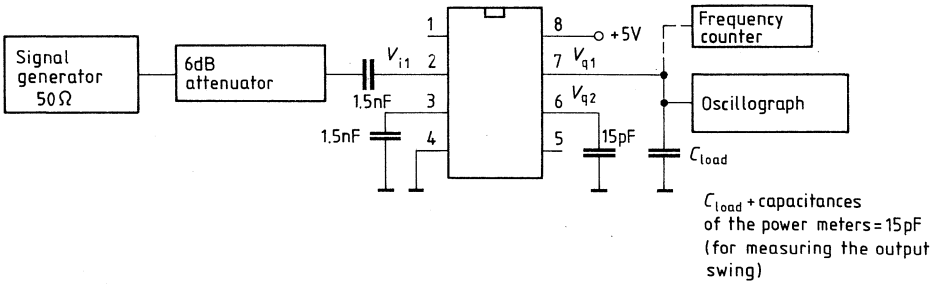


Test and measurement circuit

Calibration of the signal generator



Mesurement of the input sensitivity and the output swing



Pin configuration

Pin No.	Symbol	Function
1	N.C.	Not connected
2	I 1	Input I 1
3	I 2	Input I 2
4	GND	Ground
5	N.C.	Not connected
6	Q 2	Divider output Q 2
7	Q 1	Divider output Q 1
8	V_S	+ Supply voltage

Preliminary data **Bipolar circuit**

Type	Ordering code	Package outline
SDA 2208	Q67000-A2201	DIP 20

The SDA 2208 is designed as a remote control transmitter for direct driving of infrared transmitter diodes. The commands are generated by an input matrix (i.e. keyboard) in the form of biphase codes. Distributed over 8 levels, there are a max. of 512 commands available, or 64 commands per level.

Maximum ratings

Supply voltage range	V_S	−0.3 to 10.5	V
Matrix rows	V_{row}	−0.3 to V_S	V
Matrix columns	V_{col}	−0.3 to V_S	V
Programming pin (PPIN)	V_{PP}	−0.3 to V_S	V
Oscillator input (OSC)	V_{OSC}	−0.3 to 2	V
Infrared output (IRA)			
inhibited	V_q	−0.3 to 10.5	V
in operation	V_q	−0.3 to 8	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C

Operating range

Supply voltage	V_S	4 to 10	V
Ambient temperature range	T_{amb}	0 to 70	°C
Oscillator frequency	f_{OSC}	430 to 530	kHz
Frequency deviation (tolerance of the external circuitry = 0)			
at ceramic resonator	Δf_{OSC}		
at *LC* circuit	Δf_{OSC}		

Characteristics ($4\ V \leqq V_S \leqq 10\ V$; $0\ °C \leqq T_{amb} \leqq 70\ °C$)

		min	typ	max	
Current consumption					
standby mode	I_S			1	µA
transmitting phase	I_S			10	mA
Output IRA, current consumption					
inhibited	I_q		< 1	10	µA
conductive ($2 < V_q < 6\ V$)	I_q	500		1000	mA
Connecting resistance (row-column or column-PPIN)	R_{RC}			500	Ω

Pin configuration

Pin No.	Function
1	Ground
2	Output IRA
3	Supply voltage V_S
4	R2
5	R7
6	R1
7	R6
8	R8
9	R4
10	R3
11	R5
12	PPIN
13	CH
14	CE
15	CB
16	CC
17	CG
18	CD
19	CF
20	Oscillator input OSC

Detailed description of functions

Voltage supply

Being absent in the quiescent state, voltage consumption will begin subsequently to connecting the component's matrix. However, after the matrix has been disconnected, the IC will automatically complete the message before returning to the quiescent state.

Clock input

The clock input is eqipped with a ceramic resonator. This resonator oscillates with its parallel resonant frequency. In addition, an external clock signal can be fed into the OSC pin. As an alternative, the oscillator can be operated by using an *LC* circuit with a coupling capacitor.

Input matrix

The matrix is comprised of 8 rows and 8 columns, whereby the supply voltage V_S is used as column A. Messages are transmitted by connecting the respective rows with the columns.

As a result, the transmitter is switched on and a message is generated. A message includes a start command, a varying number of information commands (depending, like the length of the message, on the duration of the matrix connection) as well as an end command.

If less than 8 rows are required for the key matrix, a smaller-sized package can be used for the IC.

Programming via PPIN

The programming pin (PPIN) is used to provide access to all command sets or 512 commands, since the 8x8 matrix limits the use to one command set or 64 commands only. By having the command sets subdivided into 8 levels of 64 commands each, a specific level can be selected by either keeping the PPIN open or by combining it with one of the seven column inputs (SPB to SPH).

Connecting the PPIN with one column alone does not increase the standby-current consumption I_S.

Operating errors and their prevention

As a prerequisite for errorfree message output with at least one information command, the matrix connection has to be free from interference at a clock frequency-dependent, minimum duration (approx. 60 ms at 500 kHz clock frequency). The applied circuit is equipped with a preventive mechanism (key bouncing) against erroneous outputs by means of automatic resetting during any detected distortions. In addition, operating errors such as connecting more than one respective row and column are recognized, ending the transmission of the message by continuously transmitting end commands. Operating errors can only be cancelled by disconnecting all matrix connections. When operating the level selection key (PPIN function), it has to be activated before or simultaneously with the matrix key. Otherwise, the level key will not be effective. Also, simultaneous depressing of several level keys has the same affect on the message as an erroneous matrix operation.

Composition of the message

After the device has been switched on, command No. 511 (10 bit word length) will respond as start command to indicate to the receiver the onset of transmission. Depending on the duration of the matrix connection, a series of identical information commands will appear. If the message is ended by disconnecting the matrix connection, not more than one additional information command will be issued which is immediately followed by the end command. The end command is identical with the start command.

Command structure

Each command is comprised of a presignal, an infrared interval, a start bit and 9 information bits.

The presignal will appear for $256/f_{CLK}$. During this time, a simple amplitude adjustment of the input amplifier can be performed by the receiver.

The infrared interval appears between the end of the presignal and the onset of the start bit. Again, the receiver is provided with enough time to recognize transmission distortions based on the limits of the transmission range.

The start bit has been permanently programmed as :1: and is used for synchronization purposes between transmitter and receiver.

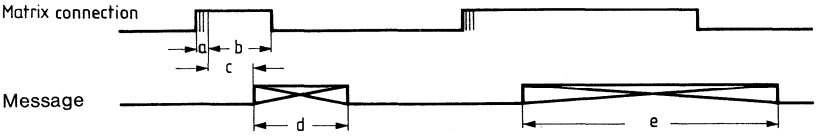
The bit structure is illustrated in the pulse diagram.

Output driver stage

By providing a fully integrated driver stage, the infrared transmitting diodes can be directly connected to the infrared output IRA. Once a range has been defined, the diode current is maintained on a constant level to stabilize the transmitting power of the infrared diodes.

Pulse diagrams

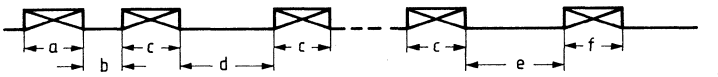
Basic operating process



for 500 kHz
b = 60.928 ms
c = 26.624 ms
d = 177.664 ms

a) bounce
b) minimum key operating time to complete message with one information command
c) delay between the on-set of interference-free matrix connection and begin of message transmission
d) message with one information command
e) message with several identical information commands

Composition of message



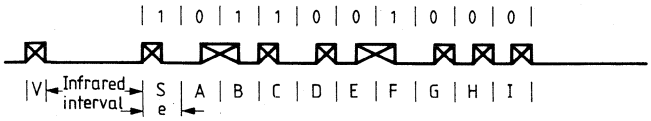
for 500 kHz
a = c = f = 13.312 ms
b = 19.968 ms
d = e = 177.76 ms

a) start command 10 bits
b) time interval between start and information command
c) information command 10 bits
d) time interval between identical information commands
e) time interval between information and end command
f) end command 10 bits

The timespan of an interference-free matrix connection determines the number of identical information commands.

Pulse diagrams

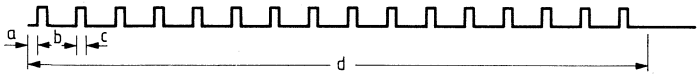
Command structure in biphase code



Time duration single bit e: $512/f_{CLK}$
presignal V: $256/f_{CLK}$
infrared interval: $5 \times 256/f_{CLK}$

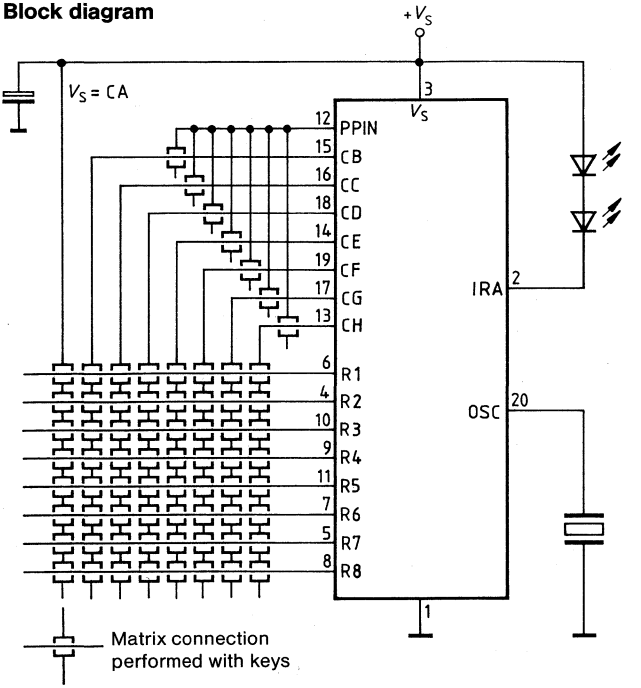
start bit S is always 1
bits A to I are addressable

Structure of the carried half bit (as well as the presignal)



$a = c = 4/f_{CLK}$
$b = 16/f_{CLK}$
$d = 256/f_{CLK}$
16 pulses per half bit

Block diagram



Truth table

No. of the command	Matrix connection row – column	Binary code IRA information command A B C D E F G H I
0	1A	0 0 0 0 0 0 0 0 0
1	1B	1 0 0 0 0 0 0 0 0
2	1C	0 1 0 0 0 0 0 0 0
3	1D	1 1 0 0 0 0 0 0 0
4	1E	0 0 1 0 0 0 0 0 0
5	1F	1 0 1 0 0 0 0 0 0
6	1G	0 1 1 0 0 0 0 0 0
7	1H	1 1 1 0 0 0 0 0 0
8	2A	0 0 0 1 0 0 0 0 0
9	2B	1 0 0 1 0 0 0 0 0
10	2C	0 1 0 1 0 0 0 0 0
11	2D	1 1 0 1 0 0 0 0 0
12	2E	0 0 1 1 0 0 0 0 0
13	2F	1 0 1 1 0 0 0 0 0
14	2G	0 1 1 1 0 0 0 0 0
15	2H	1 1 1 1 0 0 0 0 0
16	3A	0 0 0 0 1 0 0 0 0
17	3B	1 0 0 0 1 0 0 0 0
18	3C	0 1 0 0 1 0 0 0 0
19	3D	1 1 0 0 1 0 0 0 0
20	3E	0 0 1 0 1 0 0 0 0
21	3F	1 0 1 0 1 0 0 0 0
22	3G	0 1 1 0 1 0 0 0 0
23	3H	1 1 1 0 1 0 0 0 0
24	4A	0 0 0 1 1 0 0 0 0
25	4B	1 0 0 1 1 0 0 0 0
26	4C	0 1 0 1 1 0 0 0 0
27	4D	1 1 0 1 1 0 0 0 0
28	4E	0 0 1 1 1 0 0 0 0
29	4F	1 0 1 1 1 0 0 0 0
30	4G	0 1 1 1 1 0 0 0 0
31	4H	1 1 1 1 1 0 0 0 0
32	5A	0 0 0 0 0 1 0 0 0
33	5B	1 0 0 0 0 1 0 0 0
34	5C	0 1 0 0 0 1 0 0 0
35	5D	1 1 0 0 0 1 0 0 0
36	5E	0 0 1 0 0 1 0 0 0
37	5F	1 0 1 0 0 1 0 0 0
38	5G	0 1 1 0 0 1 0 0 0
39	5H	1 1 1 0 0 1 0 0 0
40	6A	0 0 0 1 0 1 0 0 0

Truth table (cont'd)

No. of the command	Matrix connection row – column	Binary code IRA information command A B C D E F G H I
41	6B	1 0 0 1 0 1 0 0 0
42	6C	0 1 0 1 0 1 0 0 0
43	6D	1 1 0 1 0 1 0 0 0
44	6E	0 0 1 1 0 1 0 0 0
45	6F	1 0 1 1 0 1 0 0 0
46	6G	0 1 1 1 0 1 0 0 0
47	6H	1 1 1 1 0 1 0 0 0
48	7A	0 0 0 0 1 1 0 0 0
49	7B	1 0 0 0 1 1 0 0 0
50	7C	0 1 0 0 1 1 0 0 0
51	7D	1 1 0 0 1 1 0 0 0
52	7E	0 0 1 0 1 1 0 0 0
53	7F	1 0 1 0 1 1 0 0 0
54	7G	0 1 1 0 1 1 0 0 0
55	7H	1 1 1 0 1 1 0 0 0
56	8A	0 0 0 1 1 1 0 0 0
57	8B	1 0 0 1 1 1 0 0 0
58	8C	0 1 0 1 1 1 0 0 0
59	8D	1 1 0 1 1 1 0 0 0
60	8E	0 0 1 1 1 1 0 0 0
61	8F	1 0 1 1 1 1 0 0 0
62	8G	0 1 1 1 1 1 0 0 0
63	8H	1 1 1 1 1 1 0 0 0

	G H I
Command 0 to 63: PPIN free	0 0 0
Command 64 to 127: PPIN connected with CA	1 0 0
Command 128 to 191: PPIN connected with CB	0 1 0
Command 192 to 255: PPIN connected with CC	1 1 0
Command 256 to 319: PPIN connected with CD	0 0 1
Command 320 to 383: PPIN connected with CE	1 0 1
Command 384 to 447: PPIN connected with CF	0 1 1
Command 448 to 511: PPIN connected with CG	1 1 1

In every command set, the assignment command – matrix connection (row – column) is analogous to the group 0 to 63.

Example:

Command 64 is generated, when PPIN is connected with CB, and R1 with CA.

Preliminary data **Bipolar circuit**

Type	Ordering code	Package outline
SDA 2311	Q 67000-A 2314	DIP 8

Preliminary data

The SDA 3211 has been designed for application in TV receivers using frequency selection according to the frequency synthesis concept. The component includes a switchable preamplifier and an ECL divider with a 1:64 divider ratio and symmetrical ECL push-pull outputs with emitter followers. The frequency range can be extended up to 1 GHz.

Features

- Switchable inputs
- Low power consumption
- Few external components

Maximum ratings

Supply voltage	V_S	6	V
Input voltage (peak-to-peak)	V_1, V_2	2.5	V
Divider outputs	I_5, I_6	−10 to 10	mA
Band selection input	V_4	20	V
Max. power dissipation	P_3	0.45	W
Junction temperature	T_j	90	°C
($T_{amb} = 25$ °C)			
Storage temperature range	T_{stg}	−55 to 125	°C
Thermal resistance (system-air)	R_{thSA}	120	K/W

Operating range

Supply voltage range	V_3	4.7 to 5.5	V
Input frequency range	f_1, f_2	80 to 1000	MHz
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics (V_S = 4.7 to 5.5 V; T_{amb} = 0 to 70 °C)

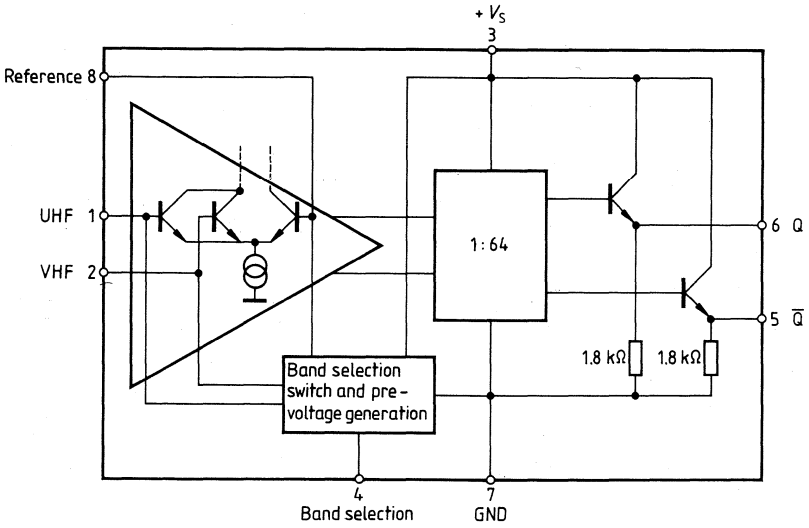
		Test circuit No.	min	type	max	
Input level UHF						
V_4 = "High"						
("Input sensitivity")						
80 to 100 MHz		2	−24		3	dBm
100 to 800 MHz		2	−27		3	dBm
800 to 950 MHz		2	−16		3	dBm
950 to 1000 MHz		2	−12		3	dBm
T_{amb} = 0 to 55 °C						
800 to 950 MHz		2	−21		3	dBm
950 to 1000 MHz		2	−18		3	dBm
Input level VHF						
V_4 = "Low"						
80 to 100 MHz		3	−24		3	dBm
100 to 500 MHz		3	−27		3	dBm
Current consumption	I_3			50	70	mA
Output voltage swing (peak-to-peak) (Load see test circuit)	V_{q5}/V_{q6}	4	0.6			V
Band selection input						
H level	V_{i4}		3		18	V
L level	V_{i4}		−0.5		0.6	V
Band selection current V_4 = 5 V	I_4				2	mA
Band selection current V_4 = 0 V	$-I_4$				1	mA

Circuit description

The IC amplifier includes a UHF, VHF, and a reference input. The UHF or the VHF input will be disabled in accordance with the "H" or "L" level at the band selection input. The HF input signals have to be coupled in the capacitive mode. The reference input is disabled by a capacitance with low series inductance connected to ground.

The divider of the IC consists of several state-controlled master-slave flipflops which determine the 1:64 divider rate. The push-pull outputs of the divider are emitter follower outputs with integrated pull-up resistances (1.8 kΩ against ground). The typical "High" level of the outputs is V_S—0.7 V and the typical voltage swing is 1 V (peak-to-peak).

Block diagram

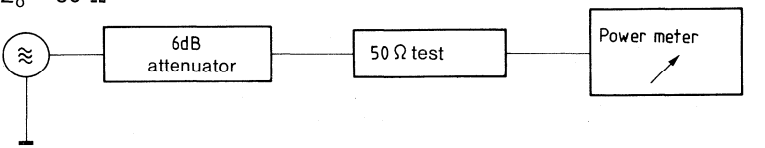


Pin configuration

Pin No.	Symbol	Function
1	UHF	UHF input
2	VHF	VHF input
3	$+V_S$	Supply voltage $+V_S$
4	BS	Band selection input
5	$\overline{Q}$	Divider output
6	Q	Divider output
7	GND	Ground
8	REF	Reference input

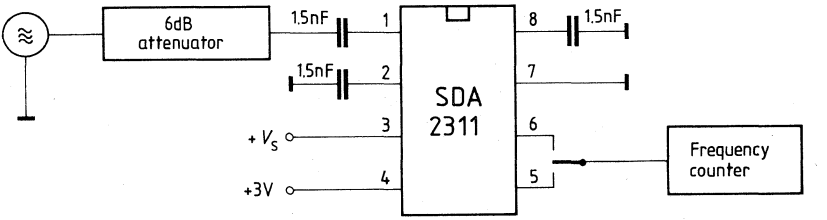
Test and measurement circuits

Signal generator
$Z_o = 50\ \Omega$



Test circuit 1: Calibration of the signal generator

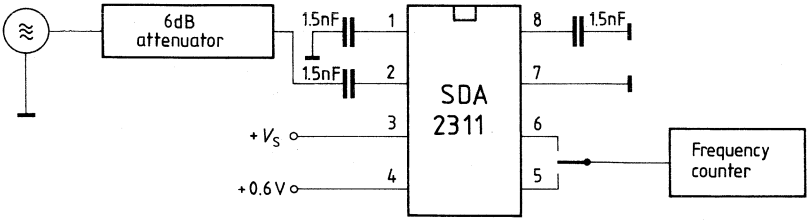
Signal generator
$Z_o = 50\ \Omega$



Test circuit 2: Measurement of the UHF input sensitivity

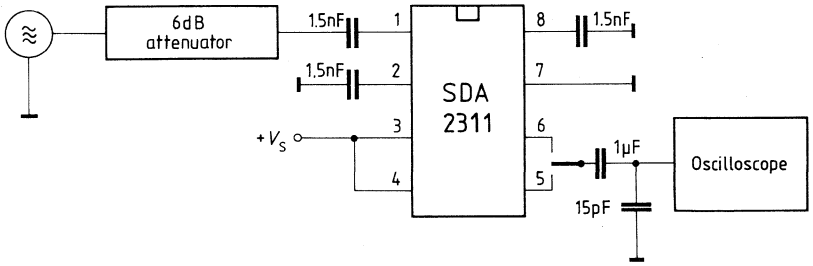
Test and measurement circuits

Signal generator
$Z_o = 50\ \Omega$



Test circuit 3: Measurement of the VHF input sensitivity

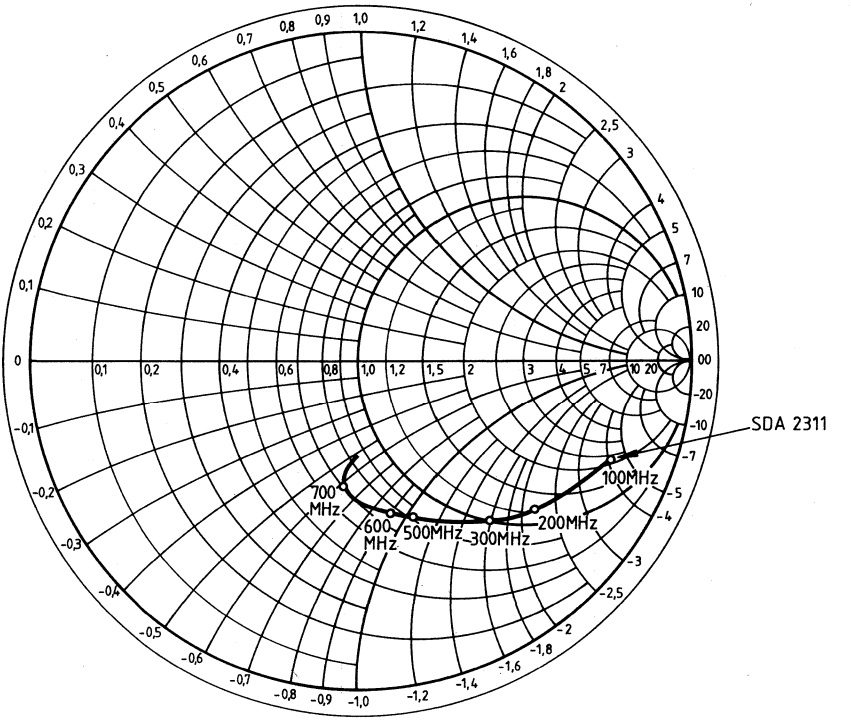
Signal generator
$Z_o = 50\ \Omega$



Test circuit 4: Measurement of the output level

Characteristics

S parameter S 11 (typical)
to determine input impedance
Reference resistance $Z_0 = 75\ \Omega$



Preliminary data **Bipolar circuit**

Type	Ordering code	Package outline
SDA 3002	Q 67000-A 2267	DIP 18

The SDA 3002 is fabricated in ASBC technology. In connection with a VCO (tuner) and a high-speed 1:64 divider, it forms a digitally programmable phase-locked loop for producing TV sets with PLL frequency-synthesis tuning.

The PLL enables crystal-controlled setting of the tuner oscillator frequency for a 62.5 kHz resolution in the TV bands III, IV, and V.

A serial interface provides for simple connection to a microprocessor. The latter loads the prescaler and the band selection outputs with the appropriate information. Status information from the PLL (locked/unlocked) appears at the LOCK output.

Features

- No external integrator required
- Noise-immune message transmission
- Software-controlled integration time constant
- Microprocessor-compatible

Maximum ratings

Supply voltage	V_S	−0.3 to 7.5	V
Inputs			
Q1, Q2, I_{ref}	V_I	−0.3 to V_S	V
IFO, CPL	V_I	−0.3 to V_S +0.5	V
PLE	V_I	−0.3 to 7.8	V
F, $\overline{F}$	V_I	−0.3 to V_S + 0.5	V
Outputs			
PD	V_Q	−0.3 to V_S	V
UD	V_Q	−0.3 to 33	V
	I_{QL}	−7	mA
BS, $\overline{VHF}$, $\overline{UHF}$, Bd I/III, standard	V_Q	−0.3 to 16	V
LOCK	I_Q	−1 to 5	mA
Junction temperature	T_j	140	°C
Storage temperature range	T_{stg}	−55 to 150	°C
Thermal resistance (system-air)	R_{thSA}	80	K/W

Operating range

Supply voltage range	V_S	4.5 to 7.15	V
Input frequency	$f_F, f_{\overline{F}}$	16	MHz
Divider factor	N	1024 to 16383	
Resistance for I_{ref} $I_{ref} = (V_S - 0.8)/R_I$	R_I	80	kΩ
Tuning voltage range open collector	V_{tun}	0.3 to 33	V
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics ($V_S = 5\ V \pm 0.5\ V$; $T_{amb} = 0$ to 70 °C)

		min	typ	max	
Supply current	I_S	15	22	30	mA
Signal inputs F/$\overline{F}$					
Input voltage	V_{16H}			$V_S + 0.2$	V
	V_{16L}	3.8			V
Input current	I_{16}			50	µA
$V_{16} = 5\ V$					
Input sensitivity at sine push-pull; $f = 16$ MHz (peak-to-peak)	V_{16}	120		1200	mV
Inputs (IFO, CPL, PLE)					
Input voltage	V_{8H}	2.4			V
	V_{8L}			0.8	V
Input current					
$V_{8H} = 5\ V$	I_{8H}			8	µA
$V_{8L} = 0.4\ V$	I_{8L}			−550	µA
Band select outputs					
Reverse current	I_{3H}			10	µA
$V_{3H} = 15\ V$					
Current drain	I_{3H}	0.5		3	mA
$2\ V \leqq V_3 \leqq 15\ V$					
Tuning section PD, UD, I_{ref}, LOCK					
Charge pump current	I_{13}			± 500	µA
$I_{pump} = 10 \times I_{ref}$					
Tuning voltage	V_{15L}			0.3	V
$I_{15L} = 1.5\ mA$					
Reverse current	I_{15H}			20	µA
$V_{15H} = 33\ V$					
Reference current	I_{14}	30		40	µA
ext. $R = 120\ k\Omega$					
Output voltage	V_{12H}	4.5			V
int. $R_L = 3\ k\Omega$					
$I_{12H} = -100\ \mu A$					
$I_{12L} = 100\ \mu A$	V_{12L}			0.7	V
IFO, PLE					
Set-up time for					
enable	t_{SE}	2			µs
data	t_{SD}	2			µs
Hold time for:					
enable	t_{HE}	2			µs
data	t_{HD}	2			µs
CPL					
H pulse width	t_{CH}	2			µs
L pulse width	t_{CL}	2			µs

Circuit description

A switchable 32/33 counter is triggered by the ECL inputs F/$\overline{F}$. The counter, in connection with a 5-bit and a 9-bit programmable, synchronous counter, forms a programmable, 14-bit synchronous divider using the dual-modulus technique, the 5-bit counter controlling the switchover from 32 to 33 (see block diagram 1). Divider ratios of $N = 1024$ to 16383 are possible.

The 18-bit shift register incl. latch is subdivided into 14 bits for storing the divider ratio N, 1 bit for selecting the pump current, 1 bit for standard switching and 2 bits for controlling the four band-selection outputs. The message is shifted in via the serial data input IFO with the HL edge of the shift clock CPL when the enable input PLE is also on high level. After the complement of the divider ratio, beginning with the LSB, has been entered in binary code, the select bit 2^{14} for the pump current, the control bit 2^{15} for the standard switching and the band-selection control bits 2^{16} and 2^{17} complete the process (see table).

A built-in control circuit checks the word length (18 bits) of the data message. The 18-bit latch accepts the data from the shift register when the enable input PLE is on low level.

The IC includes a crystal-controlled, 4-MHz clock oscillator. The output signal from the crystal oscillator ($f_{OSC} = 4$ MHz) is divided down to 0.97656 kHz (reference signal) by a reference divider. The asynchronous, permanent divider (divider factor 1 : 64) provides a frequency resolution of 62.5 kHz.

The divided input signal is compared with the reference signal in a digital phase detector. If the falling edge of the input signal appears prior to the falling edge of the reference signal, the DOWN output of the phase detector turns to high level for the duration of this phase difference. In the reverse case the UP output turns to high level. If the two signals are in phase, both outputs remain in the low level. The UP/DOWN outputs control the two current sources I^+ and I^- (charge pump). If the two outputs are L, the charge-pump output will turn to the high-impedance state (tristate). The logic NOR of the UP and DOWN outputs provides the status information for the LOCK output.

The output current of the charge pump (source current = drain current) is set by an external resistor across the pins I_{ref} and V_{CC}. In addition, the output current can be output by the control bit for the pump current, either unaltered or increased by a factor of 10 (see table).

The current pulses generated by the charge pump are integrated to form the tuning voltage by means of an active lowpass filter (internal amplifier and external RC circuitry). The dc output signal of the lowpass filter appears at V_{tun} and serves as a tuning voltage for the VCO. The output stage of the amplifier also includes a transistor with open collector for generating tuning voltages greater than $V_{CC} = 5$ V. The external collector resistance can be connected to voltages of up to 33 V.

The band-selection outputs (Bd I/III, VHF, UHF, standard, BS) contain current drains with open collectors for switching voltages greater than $V_{CC} = 5$ V. In this way transistors operating as band-selection switches can be connected directly without current-limiting resistors (see application circuit).

Pin configuration

Pin No.	Symbol	Function
1	Q1	Crystal
2	Q2	Crystal
3	Standard	Standard switchover output
4	BS	Band selection output BS
5	VHF	Band selection output VHF
6	UHF	Band selection output UHF
7	Bd I/III	Band selection output I/III
8	PLE	Enable input for shift register
9	GND	Ground
10	CPL	Shift clock pulse input
11	IFO	Data input
12	LOCK	Lock output
13	PD	Amplifier input/charge pump output
14	I_{ref}	Current adjustment for charge pump
15	V_{tun}	Tuning voltage output
16	F	Signal input
17	$\overline{F}$	Signal input
18	V_S	Supply voltage

Loop-filter calculations

Loop bandwidth: $\sqrt{\frac{I_p \times K_{VCO}}{C_1 \times P \times N}} = \omega_R$

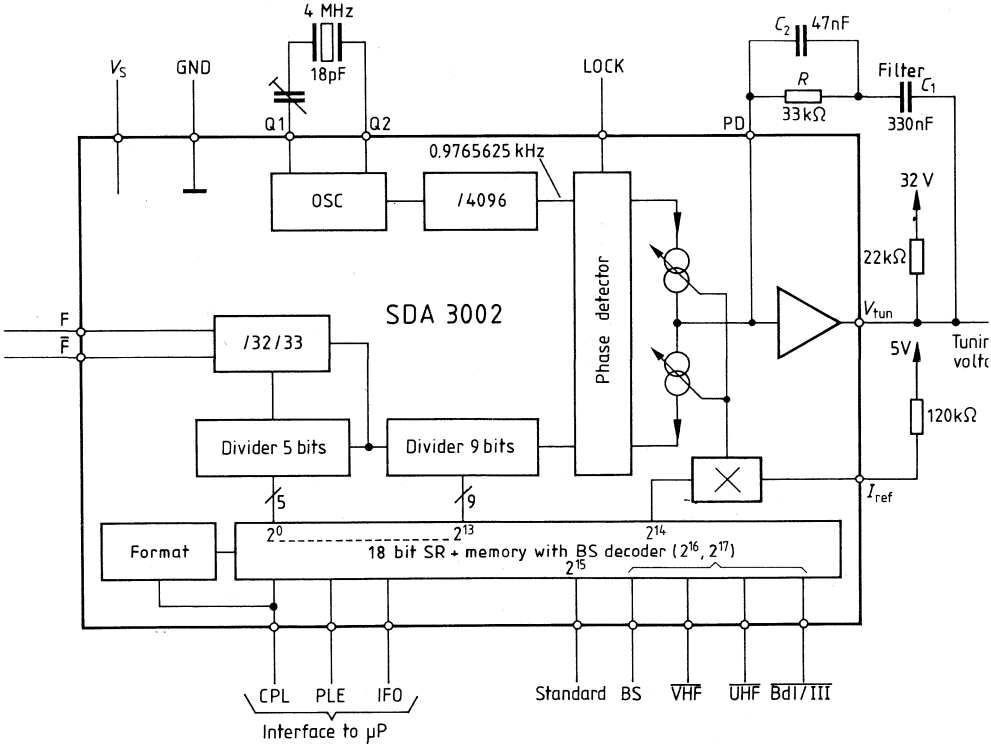
Attenuation $1/2 \times \omega_R \times R \times C_1 = \xi$

P = prescaler
N = programmable prescaler
I_p = pump current
K_{VCO} = tuner characteristic
R, C_1 = loop filter

Example for channel 47:

P = 64 N = 11520 I_p = 200 µA K_{VCO} = 18.7 MHz/V R = 33 kΩ C_1 = 330 nF
ω_R = 124 Hz f_R = 20 Hz ξ = 0.675 Standard dimensioning: $C_2 \approx C1/5$

Block diagram

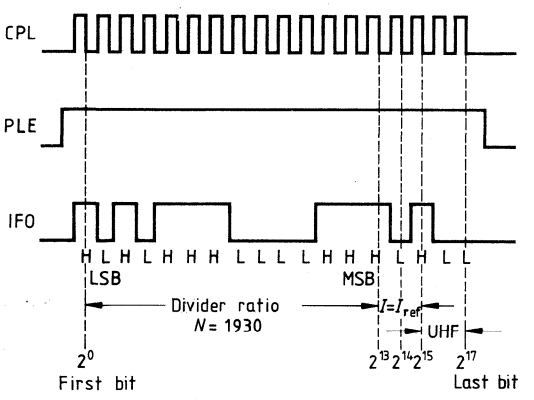


Truth table

Function	"IFO" 2^{16}	BIT 2^{17}	Band selection outputs Bd I/III	VHF	UHF	BS
UHF	L	L	H	H	L	H
VHF/Bd I	L	H	H	L	H	H
VHF/Bd III	H	L	L	L	H	H
BS	H	H	L	L	H	L

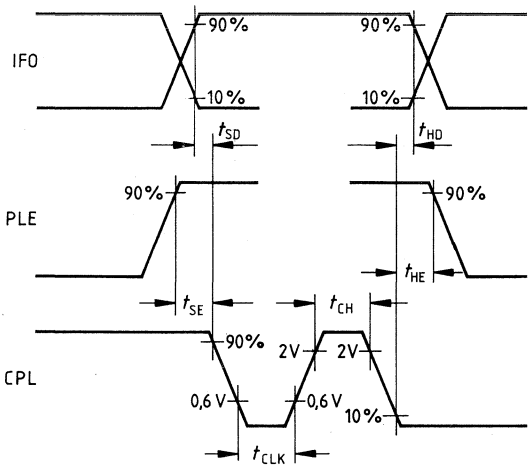
Pump current	IFO 2^{14}	BIT	BIT 2^{15} Output Standard
$I = I_{ref}$	L		L
$I = 10 \times I_{ref}$	H		H

Pulse diagram

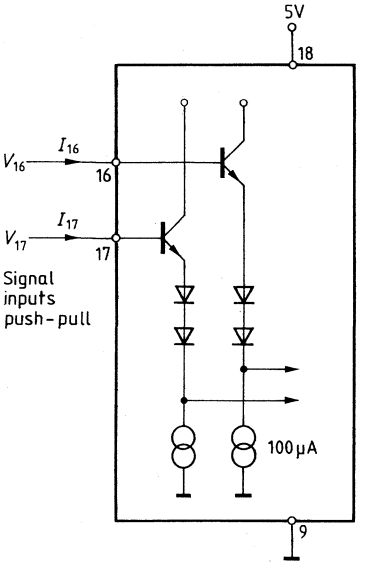


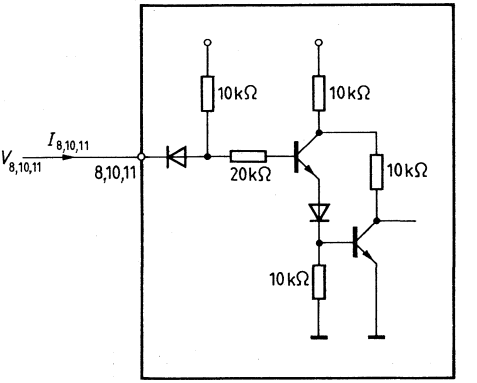
Pulse diagram

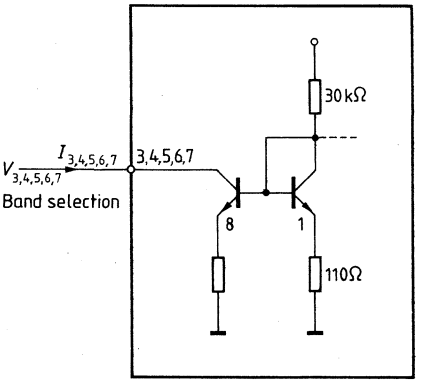
Set-up and hold times



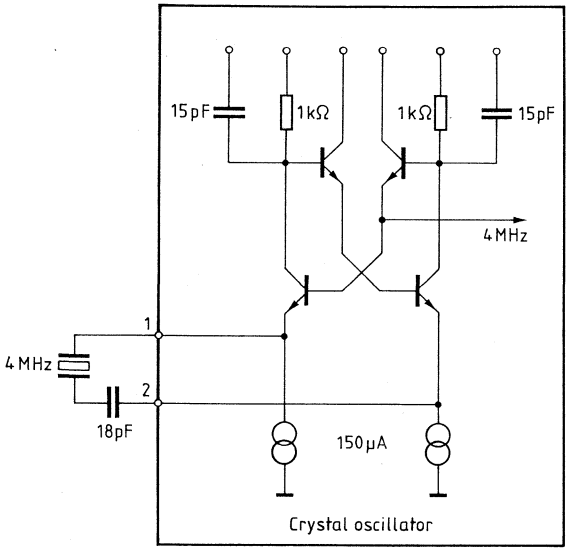
Test and measurement circuits

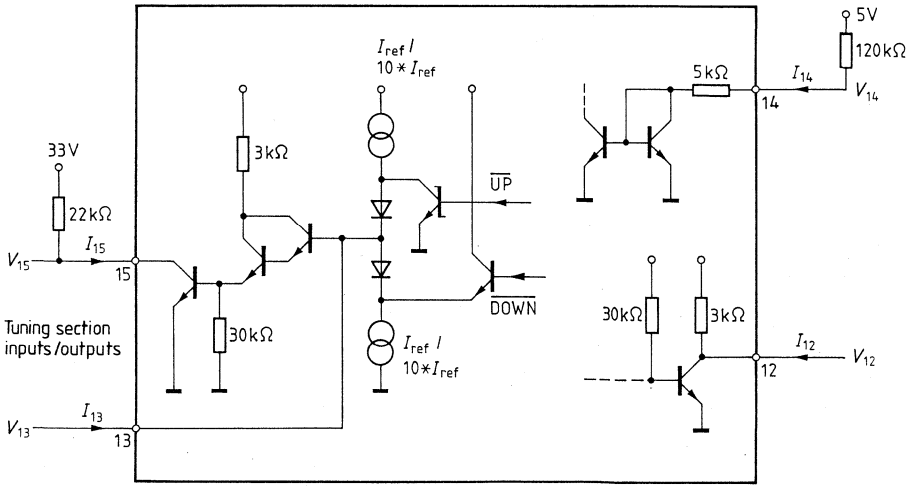






Test and measurement circuits

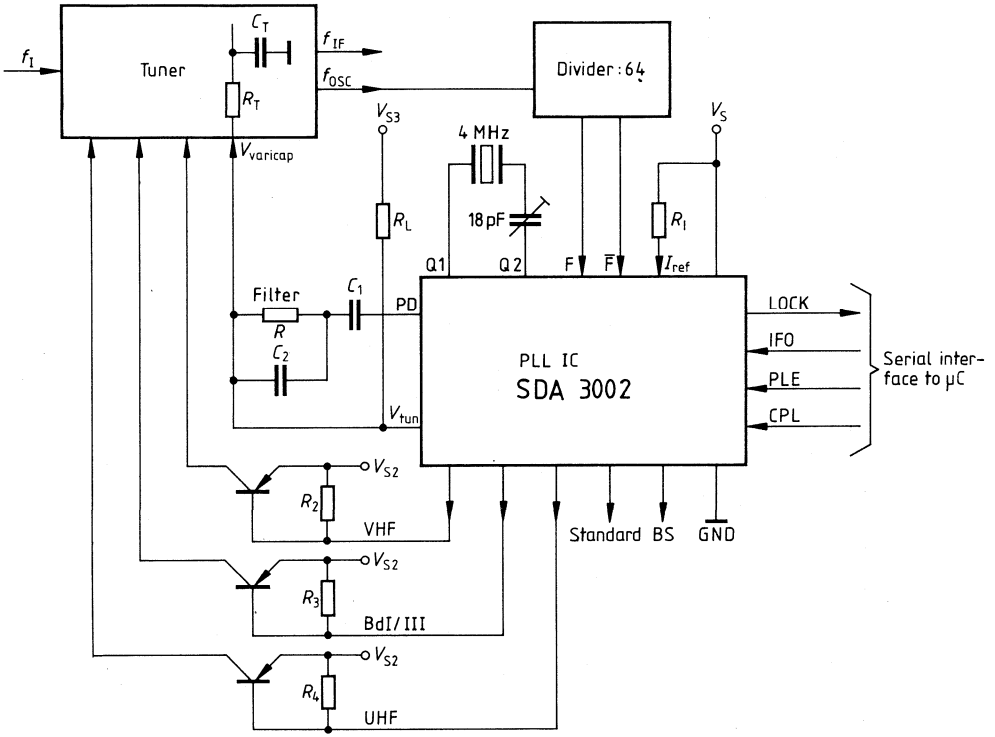




Application circuit

Design proposal

$R_I = 120\ k\Omega$ ($I_p = 35/350\ \mu A$)
$R_L = 22\ k\Omega$, $R_2 \ldots R_4 = 22\ k\Omega$
Loop filter: $R = 33\ k\Omega$, $C_1 = 330\ nF$, $C_2 = 47\ nF$
Post filter (in the tuner): $R_T = 10\ k\Omega$, $C_T = 47\ nF$



MOS circuit

Type	Ordering code	Package outline
SDA 3010	Q 67120-C 86	Piggy-back 40/24 pins

SDA 3010 (SDA 2010 – ROMless)

Features

- 8 bit CPU, RAM, IN/OUT
  in piggy back package with 40/24 pins
- Four analog outputs with 6 bit resolution
- 30 digital IN/OUT lines
  two serial interfaces
  two 8-bit interfaces
  two 4-bit interfaces
  two test inputs
- 64 byte RAM
- 10 µs cycle time — 1 or 2 cycles per instruction
- Zero passage detector
- Interface for modulated digital signal
- Interval timer/counter
- 5 V supply voltage
- Instructions – subset of SAB 8048
- Pin connection for SAB 2716 EPROM on the top side of the package

Brief description[1)]
Piggy-back EPROM microcomputer SDA 3010

The application-specific SDA 3010 is of identical design as the SDA 2010, SDA 2020, and SDA 2030 with the exception of the ROM program which has been replaced by the circuitry and socket to accomodate the piggy back EPROM, e.g. the Intel 2716 2 K x 8 EPROM. The combination SDA 3010 with CPU, RAM, E/A and EPROM socket simulates a complete single-chip microcomputer.

When installed in a system, the SDA 3010 will perform in the same way as its planned mask-programmed version.

With the exception of the SDA 2020 and SDA 2030 which require an adapter socket with 40 to 28 pins, the selected configuration enables system field tests during the final electrical and mechanical stages. This approach facilitates troubleshooting and software development for the SDA 2010, SDA 2020 and SDA 2030. In addition, an error-free software can be developed prior to manufacturing the ROM mask for the final product.

1) Detailed information upon request.

The SDA 3010 is equipped with a 2 Kbyte program memory (ROM), a 64 byte data memory (RAM), and four 6-bit D/A converters. The 30 digital E/A lines include two 4 and 8 bit ports each, two test inputs and two serial interfaces. Each serial interface consists of a data and pulse line. Test input T0 processes signals modulated with approx. 30 kHz and is equipped with a digital demodulator which derives the envelope curve from the modulated digital signal. Since the digital demodulator forwards an unmodulated signal without changing it, the T0 test input can also function as a normal digital input during operations with standard H/L levels. Test input T1 includes a zero passage detector and can be used as a normal digital input as well. The component is equipped with its own oscillator and timer/counter.

The instruction set includes 65 instructions (1-2 bytes) which can be processed in max. 2 cycles. Numerical problems can be processed in either binary or BCD arithmetic mode. The large number of bit-handling instructions increases the efficiency of the controller functions.

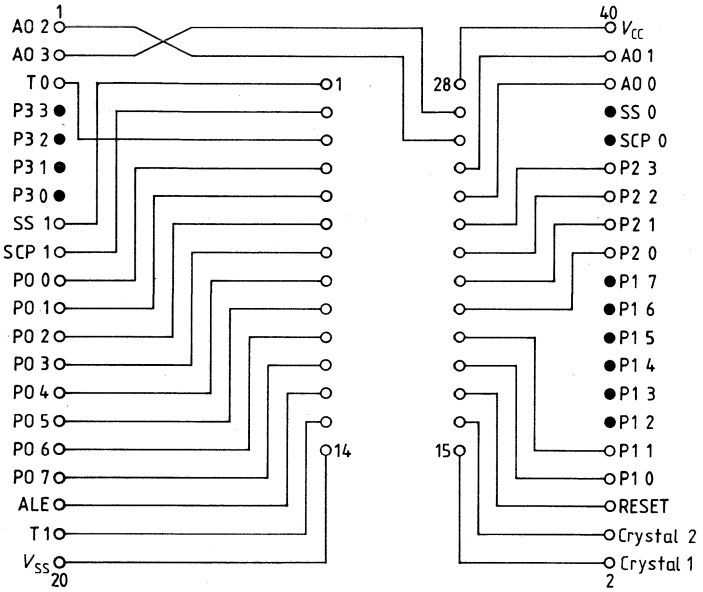
Maximum ratings

Maximum ratings must be carefully observed to prevent permanent damages to the IC.

Supply voltage range	V_{CC}	0.5 to 7	V
Ambient temperature range in operation	T_{amb}	−20 to 85	°C
Storage temperature range	T_{stg}	−55 to 125	°C
Voltage between any pin and ground	V	−0.5 to 7	V
Total power dissipation	P_{tot}	1	W

Adapter socket

40 pins → 28 pins



SDA 3010 → SDA2020 and SDA 2030

DC voltage characteristics

(T_{amb} = 0 to 70 °C; $V_{CC} = V_{SB}$ = 5.5 V ±1 V; V_{SS} = 0 V)

		Test conditions	min.	max.	
L input voltage (ports, SS 0, SS 1, RESET, 00-07)	V_{iL}		−0.5	0.8	V
H input voltage (ports, SS 0, SS 1, 00-07)	V_{iH}	V_{CC} = 5.0 V ±10%	2.0	V_{CC}	V
H input voltage (ports, SS0, SS 1, 00-07)	V_{iH1}	V_{CC} = 6.0 V ±0.5 V	2.4	V_{CC}	V
H input voltage (RESET, X 1)	V_{iH2}		3.0	V_{CC}	V
L output voltage (port 0-3, ALE, AR0-AR 9)	V_{qL}	I_{qL} = 1.6 mA		0.45	V
L output voltage (SS 0, SS 1, SCP 0, SCP 1)	V_{qL1}	I_{qL} = 4 mA		0.45	V
L output voltage (A 0-A 3)	V_{qL2}	I_{qL} = 4 mA		0.45	V
H output voltage (port 0-3, ALE, AR 0-AR 9)	V_{qH}	I_{qH} = 50 µA	2.4		V
H output voltage (SS 0, SS 1, SCP 0, SCP 1)	V_{qH1}	I_{qH} = 150 µA	2.4		V
H output voltage (A 0-A 3)	V_{qH2}	I_{qH} = 4 mA	V_{CC} −0.45		V
H input current (T 0-T 1)	I_{iH}	$V_{iH} = V_{CC}$		10	µA
L input current (port 0-3, SS 0, SS 1)	$-I_{iL}$	V_{iL} = 0.45 V	30	340	µA
Input voltage at T 1 (peak-to-peak)	V_{T1}	C_{inp} = 1 µF	1	3	V
Zero passage detector Current consumption without EPROM	I_{CC}			80	mA

AC voltage characteristics

(T_{amb} = 0 to 70 °C; $V_{CC} = V_{SB}$ = 5.5 V ±1 V; V_{SS} = 0 V)

Cycle time	t_C	3 MHz crystal (≡10 µs)	10	50	µs
ALE pulse width	t_{ALE}	t_C = 10 µs	1.3		µs
Oscillator spread frequency	Δf_{OSC}	f = 2.5 MHz, R = 15 kΩ	−20	+20	%
Period of an unmodulated signal at test input T 0	t_{MTO}	3 MHz crystal	60		µs
Frequency of a modulated signal at test input T 0	f_{TR}	3 MHz crystal	30	35	kHz
Frequency range of the zero passage detector (input T 1)	f_{T1}		0.03	1	kHz

Pin configuration

Bottom side

Pin No.	Symbol	Function
40	V_{CC}	+5 V
20	V_{SS}	Ground 0 V
21, 22	X1, X2	Connection for crystal or similar
10 to 17	P0 0...7	Quasi-bidirectional 8-bit port
24 to 31	P1 0...7	Quasi-bidirectional 8-bit port
32 to 35	P2 0...3	Quasi-bidirectional 4-bit port
7 to 4	P3 0...3	Quasi-bidirectional 4-bit port
38, 39, 1, 2	A0...A3	4 analog outputs. The analog values are output as rectangular signals with a frequency of approx. 2 kHz, during which the duty cycle corresponds to the analog value.
37, 8	SS0, SS1	Serial interface IN/OUT pin
36, 9	SCP0, SCP1	Serial interface clock pulse
23	RESET	Reset input for the initialization of the computer. Resets program counter, erases the status FFs. Sets all digital outputs to H state. (active H)
3	T0	Input that can be tested with the conditional jump instructions JT0 and JNT0. The input contains a digital demodulator and can be used for the separation of the envelope curve from a modulated signal.
19	T1	Input that can be tested with the conditional jump instructions JT1 and JNT1. Serves simultaneously as an external counter input. (Selection of functions with instruction STRT CNT). The input can also be used for zero passage recognition of low frequency alternating voltages.
18	ALE	This output generates one clock pulse signal per cycle.

Top side

1 to 8, 22, 23, 19	AR0...AR10	Address output for SAB 2716 EPROM (program counter)
9 to 11, 13 to 17	00...07	Data input (commands)
12, 19, 20	V_{SS}	Ground
20, 29	V_{CC}	+5 V

Instruction set of SDA 3010

	Mnemonic	Description	Bytes	Cycles	Hexadecimal opcode
Accumulator	ADD A, Rr	Add register to A	1	1	68–6F
	ADD A,@ R	Add data memory to A	1	1	60–61
	ADD A, # data	Add immediate to A	2	2	03
	ADDC, A, Rr	Add register with carry	1	1	78–7F
	ADDC A, @ R	Add data memory with carry	1	1	70–71
	ADDC A, # data	Add immediate with carry	2	2	13
	ANL A, Rr	And register to A	1	1	58–5F
	ANL A, @ R	And data memory to A	1	1	50–51
	ANL A,# data	And immediate to A	2	2	53
	ORL A, Rr	Or register to A	1	1	48–4F
	ORL A, @ R	Or data memory to A	1	1	40–41
	ORL A, # data	Or immediate to A	2	2	43
	XRL A, Rr	Exclusive Or register to A	1	1	D8–DF
	XRL A, @ R	Exclusive Or data memory to A	1	1	D0–D1
	XRL A,# data	Exclusive Or immediate to A	2	2	D3
	INC A	Increment A	1	1	17
	DEC A	Decrement A	1	1	07
	CLR A	Clear A	1	1	27
	CPL A	Complement A	1	1	37
	DA A	Decimal adjust A	1	1	57
	SWAP A	Swap nibbles of A	1	1	47
	RL A	Rotate A left	1	1	E7
	RLC A	Rotate A left through carry	1	1	F7
	RR A	Rotate A right	1	1	77
	RRC A	Rotate A right through carry	1	1	67

Instruction set of SDA 3010

	Mnemonic	Description	Bytes	Cycles	Hexadecimal opcode
IN/OUT	IN A, Pp	Input port to A	1	2	08, 09, OC, OD
	OUT Pp, A	Output A to port	1	2	90, 39, 3C, 3D
	IN A, Sn	Input serial port to A0	1	2	OE–OF
	OUT Sn, A	Output A0 to serial port			3E–3F
Register	INC Rr	Increment register	1	1	18–1F
	INC @ R	Increment data memory	1	1	10–11
Sub-routes	CALL	Jump to subroutine	1	2	14, 34, 54, 74, 94, B4, D4, F4,
	RET	Return	1	2	83
Branches	JMP adr	Jump unconditional	2	2	04, 24, 44, 64, 84, A4, C4, E4
	JMPP @ A	Jump indirect	1	2	B3
	DJNZ Rr adr	Decrement register and jump on R not zero	2	2	E8–EF
	JC adr	Jump on carry = 1	2	2	F6
	JNC adr	Jump on carry = 0	2	2	E6
	JZ adr	Jump on A zero	2	2	C6
	JNZ adr	Jump on A not zero	2	2	96
	JT0 adr	Jump on T0 = 1	2	2	36
	JNT0 adr	Jump on T0 = 0	2	2	26
	JT1 adr	Jump on T1 = 1	2	2	56
	JNT1 adr	Jump on T1 = 0	2	2	46
	JTF adr	Jump on timer flag	2	2	16
Flags	CLR C	Clear carry	1	1	97
	CPL C	Complement carry	1	1	A7

Instruction set of SDA 3010

	Mnemonic	Description	Bytes	Cycles	Hexadecimal opcode
Transfer instructions	MOV A, Rr	Move register to A	1	1	F8–FF
	MOV A, @ R	Move data memory to A	1	1	F0–F1
	MOV A, # data	Move immediate to A	2	2	23
	MOV Rr, A	Move A to register	1	1	A8–AF
	MOV @ R, A	Move A to data memory	1	1	A0–A1
	MOV Rr#data	Move immediate to register	2	2	B8–BF
	MOV @R,# data	Move immediate to data memory	2	2	B0–B1
	XCH A, Rr	Exchange A and register	1	1	28–2F
	XCH A, @ R	Exchange A and data memory	1	1	20–21
	XCHD A,@ R	Exchange nibble of A and register	1	1	30–31
	MOVP A, @ A	Move to A from current page	1	2	A3
Timer/Counter	MOV A, T	Read timer/counter	1	1	42
	MOV T, A	Load timer/counter	1	1	62
	STRT T	Start timer	1	1	55
	STRT CNT	Start counter	1	1	45
	STOP TCNT	Stop timer/counter	1	1	65
	MOV DA, A	Move to DA – converter	1	2	91
	NOP	No operation	1	1	00

Symbols and abbreviations

A	Accumulator	Rr	Register label (r = 0 to 7)
adr	11 bit program memory address	Sn	S interface label (n = 0; 1)
CNT	Event counter	T	Timer
DA	D/A converter	T0, T1	Test 0, test 1
data	8 bit binary number	#	Refers to immediate data
P	Mnemonic for "in-page" operation	@	Refers to indirect addressing
Pp	Port label (p = 0 to 3)		

MOS circuit

Type	Ordering code	Package outline
SDA 3110	Q 67120-C 87	Piggy-back 28/24 pins

SDA 3110 (SDA 2110 – ROMless)

Features

- 8-bit CPU, RAM, IN/OUT in piggy back package with 28/24 pins
- 21 digital IN/OUT lines
  one serial interface
  one 8-bit interface
  two 4-bit interfaces
- one 1-bit interface
  two test inputs
- 40 byte RAM
- 10 µs cycle time — 1 or 2 cycles per instruction
- Zero passage detector
- Interface for modulated digital signal
- Interval timer/counter
- 5 V supply voltage
- Stand-by operation of the RAM
- Instructions – subset of SAB 8048
- Pin connection for SAB 2716 EPROM on the top side of the package

Brief description[1)]
Piggy back EPROM microcomputer SDA 3110

The application-specific SDA 3110 is of identical design as the SDA 2110 and SDA 2111 with the exception of the ROM program which has been replaced by the circuitry and socket to accomodate the piggy-back EPROM, e.g. the Intel 2716 2 K x 8 EPROM. The combination SDA 3110 with CPU, RAM, E/A and EPROM socket simulates a complete single-chip microcomputer.

When installed in a system, the SDA 3110 will perform in the same way as its planned mask-programmed version. With the exception of the SDA 2111 which requires an adapter socket with 28 to 22 pins, the selected configuration enables system field tests during the final electrical and mechanical stages.

This approach facilitates troubleshooting and software development for the SDA 2110 and SDA 2111. In addition, an error-free software can be developed prior to manufacturing the ROM mask for the final product.

1) Detailed information upon request.

The SDA 3110 is equipped with a 1 Kbyte useful program memory (ROM) and a 40 byte data memory (RAM) which can be operated in stand-by mode at largely reduced power loss. The 21 digital E/A lines include an 8-bit port, two 4-bit ports, two test inputs, one serial interface, and one 1-bit interface. Test input T0 processes signals modulated with approx. 30 kHz and is equipped with a digital demodulator which derives the envelope curve from the modulated digital signal. Since the digital demodulator forwards an unmodulated signal without changing it, the T0 test input can also function as a normal digital input during operations with standard H/L levels.

Test input T1 includes a zero passage detector and can be used as a normal digital input as well. The serial interface includes a data and pulse line.

The component is equipped with its own oscillator and timer/counter.

The instruction set includes 66 instructions (1-2 bytes) which can be processed in max. 2 cycles. Numerical problems can be processed in either binary or BCD arithmetic mode. The large number of bit-handling instructions increases the efficiency of the controller functions.

Maximum ratings

Maximum ratings must be carefully observed to prevent permanent damages to the IC.

Supply voltage range	V_{CC}	−0.5 to 7	V
Ambient temperature range in operation	T_{amb}	−20 to 85	°C
Storage temperature range	T_{stg}	−55 to 125	°C
Voltage between any pin and ground	V	−0.5 to 7	V

DC voltage characteristics

(T_{amb} = 0 to 70 °C; $V_{CC} = V_{SB}$ = 5.5 V ±1 V; V_{SS} = 0 V)

		Test conditions	min	max	
L input voltage (ports, SS 0, SS 1, RESET 00-07)	V_{iL}		−0.5	0.8	V
H input voltage (ports, SS 0, SS 1, 00-07)	V_{iH}	V_{CC} = 5.0 V ±10%	2.0	V_{CC}	V
H input voltage (ports, SS 0, SS 1, 00-07)	V_{iH1}	V_{CC} = 6.0 V ±0.5 V	2.4	V_{CC}	V
H input voltage (RESET, X 1)	V_{iH2}		3.0	V_{CC}	V
L output voltage (ports, ALE, A0-A 9)	V_{qL}	I_{qL} = 1.6 mA		0.45	V
L output voltage (SS 0, SS 1, SCP 1)	V_{qL1}	I_{qL} = 4 mA		0.45	V
H output voltage (ports, ALE, A0-A 9)	V_{qH}	I_{qH} = 50 µA	2.4		V
H output voltage (SS 0, SS 1, SCP 1)	V_{qH1}	I_{qH} = 150 µA	2.4		V
H input current (T 0, T 1)	I_{iH}	$V_{iH} = V_{CC}$		10	µA
L input current (ports, SS 0, SS 1)	$-I_{iL}$	V_{iL} = 0.45 V	30	340	µA
Input voltage at T 1 (peak-to-peack)	V_{T1}	C_{inp} = 1 µF	1	3	V
Zero passage detector Current consumption without EPROM	I_{CC}			60	mA

AC voltage characteristics

(T_{amb} = 0 to 70 °C; $V_{CC} = V_{SB}$ = 5.5 V ±1 V; V_{SS} = 0 V)

Cycle time	t_C	3 MHz crystal (= 10 µs)	10	50	µs
ALE pulse width	t_{ALE}	t_C = 10 µs	1.3		µs
Oscillator spread frequency	Δf_{OSC}	f = 2.5 MHz, R = 15 kΩ	−20	+20	%
Period of an unmodulated signal at test input T 0	t_{MTO}	3 MHz crystal	60		µs
Frequency of a modulated signal at test input T 0	f_{TR}	3 MHz crystal	30	35	kHz
Frequency range of the zero passage detector (input T 1)	f_{T1}		0.03	1	kHz

Pin configuration

Bottom side

Pin No.	Symbol	Function
28	V_{CC}	+5 V
1	V_{SB}	+5 V standby supply
14	V_{SS}	Ground 0 V
15, 16	X 1, X 2	Connection for crystal or similar
4 to 11	P0 0 to 7	Quasi-bidirectional 8-bit port
18 to 21	P2 0 to 3	Quasi-bidirectional 4-bit port
22 to 25	P3 0 to 3	Quasi-bidirectional 4-bit port
26	SS0	1 bit interface IN/OUT pin
27	SS1	Serial interface S1 IN/OUT pin
2	SCP1	Serial interface S1 clock pulse
17	RESET	Reset input for the initialization of the computer (active H). Resets program counter, erases the status FFs. Sets all digital outputs to H state.
3	T0	Input that can be tested with the conditional jump instructions JT0 and JNT0. The input contains a digital demodulator and can be used for the separation of the envelope curve from a modulated signal.
13	T1	Input that can be tested with the conditional jump instructions JT1 and JNT1. Serves simultaneously as an external counter input. (Selection of functions with instruction STRT CNT). The input can also be used for zero passage recognition of low frequency alternating voltages.
12	ALE	This output generates one clock pulse signal per cycle.

Top side

1 to 8	A0 to A7	Address output for SAB 2716 (program counter)
22, 23	A8, A9	Address output for SAB 2716 (program counter)
9 to 11	00 to 02	Data input (commands)
13 to 17	03 to 07	Data input (commands)
12, 18 to 20	V_{SS}	Ground
20, 24	V_{CC}	+5 V

Instruction set of SDA 3110

	Mnemonic	Description	Bytes	Cycles	Hexadecimal opcode
Accumulator	ADD A, Rr	Add register to A	1	1	68–6F
	ADD A, @ R	Add data memory to A	1	1	60–61
	ADD A, # data	Add immediate to A	2	2	03
	ADDC A, Rr	Add register with carry	1	1	78–7F
	ADDC A, @ R	Add data memory with carry	1	1	70–71
	ADDC A, # data	Add immediate with carry	2	2	13
	ANL A, Rr	And register to A	1	1	58–5F
	ANL A, @ R	And data memory to A	1	1	50–51
	ANL A, # data	And immediate to A	2	2	53
	ORL A, Rr	Or register to A	1	1	48–4F
	ORL A, @ R	Or data memory to A	1	1	40–41
	ORL A, # data	Or immediate to A	2	2	43
	XRL A, Rr	Exclusive Or register to A	1	1	D8–DF
	XRL A, @ R	Exclusive Or data memory to A	1	1	D0–D1
	XRL A, # data	Exclusive Or immediate to A	2	2	D3
	INC A	Increment A	1	1	17
	DEC A	Decrement A	1	1	07
	CLR A	Clear A	1	1	27
	CPL A	Complement A	1	1	37
	DA A	Decimal adjust A	1	1	57
	SWAP A	Swap nibbles of A	1	1	47
	RL A	Rotate A left	1	1	E7
	RLC A	Rotate A left through carry	1	1	F7
	RR A	Rotate A right	1	1	77
	RRC A	Rotate A right through carry	1	1	67

Instruction set of SDA 3110

	Mnemonic	Description	Bytes	Cycles	Hexadecimal opcode
IN/OUT	IN A, Pp	Input port to A	1	2	08, OC, OD
	OUT Pp, A	Output A to port	1	2	90, 3C, 3D
	IN A, S1	Input serial port to A0	1	2	OF
	IN A, S0	Input 1 bit port to A0	1	2	OE
	OUT S1, A	Output A0 to serial port	1	2	3F
	OUT S0, A	Output A0 to 1 bit port		2	3E
Sub-routines	CALL	Jump to subroutine	1	2	14, 34, 54, 74, 94, B4, D4, F4,
	RET	Return	1	2	83
Branches	JMP adr	Jump unconditional	2	2	04, 24, 44 64, 84, A4, C4, E4
	JMPP@ A	Jump indirect	1	2	B3
	DJNZ Rr, adr	Decrement register and jump on R not zero	2	2	E8–EF
	JC adr	Jump on carry = 1	2	2	F6
	JNC adr	Jump on carry = 0	2	2	E6
	JZ adr	Jump on A zero	2	2	C6
	JNZ adr	Jump on A not zero	2	2	96
	JT0 adr	Jump on T0 = 1	2	2	36
	JNT0 adr	Jump on T0 = 0	2	2	26
	JT1 adr	Jump on T1 = 1	2	2	56
	JNT1 adr	Jump on T1 = 0	2	2	46
	JTF adr	Jump on timer flag	2	2	16
Flags	CLR C	Clear carry	1	1	97
	CPL C	Complement carry	1	1	A7

Instruction set of SDA 3110

	Mnemonic	Description	Bytes	Cycles	Hexadecimal opcode
Transfer instructions	MOV A, Rr	Move register to A	1	1	F8–FF
	MOV A, @ R	Move data memory to A	1	1	F0–F1
	MOV A, # data	Move immediate to A	2	2	23
	MOV Rr, A	Move A to register	1	1	A8–AF
	MOV @ R, A	Move A to data memory	1	1	A0–A1
	MOV Rr # data	Move immediate to register	2	2	B8–BF
	MOV @R, #data	Move immediate to data memory	2	2	B0–B1
	XCH A, Rr	Exchange A and register	1	1	28–2F
	XCH A, @ R	Exchange A and data memory	1	1	20–21
	XCHD A, @ R	Exchange nibble of A and register	1	1	30–31
	MOVP A, @ A	Move to A from current page	1	2	A3
Timer/Counter	MOV A, T	Read timer counter	1	1	42
	MOV T, A	Load timer/counter	1	1	62
	STRT T	Start timer	1	1	55
	STRT CNT	Start counter	1	1	45
	STOP TCNT	Stop timer/counter	1	1	65
Register	INC Rr	Increment register	1	1	18–1F
	INC @ R	Increment data memory	1	1	10–11
	NOP	No operation	1	1	00

Symbols and abbreviations

A	Accumulator	Rr	Register label (r = 0 to 7)
adr	10 bit program memory address	Sn	S interface label (n = 0; 1)
CNT	Event counter	T	Timer
DA	D/A converter label	T0, T1	Test 0, test 1
data	8 bit binary number	#	Refers to immidiate data
P	Mnemonic for "in-page" operation	@	Refers to indirect addressing
Pp	Port label (p = 0, 2, 3)		

MOS circuit

Type	Ordering code	Package outline
SDA 3205	Q 67100-Y 578	DIP 18

The SDA 3205 receiver IC, developed in MOS depletion technology, interprets the IR signals of the transmitter IC SDA 3206.

With the SDA 3205, 16 programs and 1 analog function can be selected. Moreover, the IC contains an ON/OFF input or output, respectively.

Features

- The program outputs are short-circuit proof and can be externally set.
- The SDA 3205 can be operated with the on-chip oscillator or with an external clock.

Maximum ratings (all voltages referred to $V_{DD} = 0$ V)

Supply voltage range	V_{SS}	−0.3 to 18	V
Input voltage range	V_i	V_{SS}−18 to V_{SS} +0.3	V
Total power dissipation	P_{tot}	500	mW
Power dissipation per output	P_q	100	mW
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	90	K/W

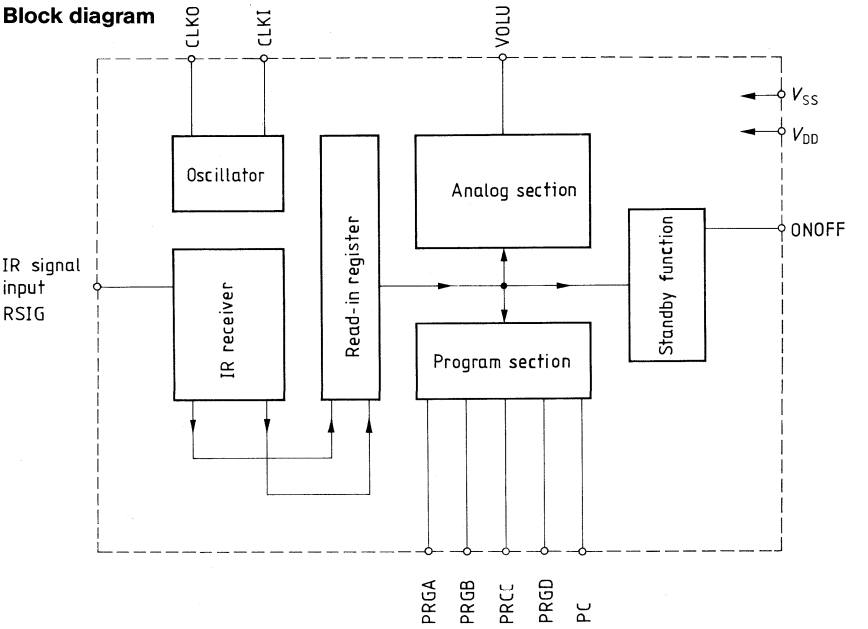
Operating range (referred to $V_{DD} = 0$ V)

Supply voltage range	V_{SS}	11 to 16	V
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics (referred to $V_{DD} = 0$ V, $T_{amb} = 0$ to 70 °C)

		min	typ	max	
Current consumption (outputs open)	I_{DD}		5	10	mA
Inputs Clock input CLKI					
L input voltage	V_{iL}	0		$V_{SS}-7$	V
H input voltage	V_{iH}	$V_{SS}-1$		V_{SS}	V
Input current	I_i			15	µs
Transition times	t_{THL}, t_{TLH}			4	µs
Frequency	f	20	60	70	kHz
Remote control signal input RSIG					
Input alternating voltage	V_{iH}	$V_{SS}-1$		V_{SS}	V
	V_{iL}	0		$V_{SS}-3.5$	V
Input resistance	R_i	0.2			MΩ
Inputs					
Program stepping input PC					
H input voltage	V_{iH}	$V_{SS}-1.5$		V_{SS}	V
L input voltage	V_{iL}	0		$V_{SS}-7$	V
H input current ($V_i = V_{SS}$) (internal pull low resistor)	I_{iH}			10	µA
Standby output ONOFF					
H input voltage ($I_{iH} < 1$ mA)	V_{iH}	$V_{SS}-1$ V		V_{SS}	V
Outputs					
Program memory outputs PRGA, PRGB, PRGC, PRGD					
H output voltage ($I_q = 0.1$ mA)	V_{qH}	$V_{SS}-0.5$		V_{SS}	V
L output voltage ($I_q = 10$ µA)	V_{qL}	0		1	V
Program stepping output PC					
H output voltage ($I_q = 0.3$ mA)	V_{qH}	$V_{SS}-1.5$		V_{SS}	V
L output voltage (no load)	V_{qL}	0		2	V
Analog functions output VOLU					
H output voltage ($I_q = 1$ mA)	V_{qH}	$V_{SS}-1.5$		V_{SS}	V
L output voltage ($I_q = 1$ µA)	V_{qL}	0		0.35	V
Standby output ONOFF					
H output voltage ($I_q = 0.3$ mA)	V_{qH}	$V_{SS}-1.5$		V_{SS}	V
L output voltage ($I_q = 1$ µA)	V_{qL}	0		0.35	V
Clock output CLKO					
H output voltage (no load)	V_{qH}	$V_{SS}-1$		V_{SS}	V
L output voltage (no load)	V_{qL}	0		1	V

Block diagram



Pin configuration

Pin No.	Symbol	Function
1	V_{SS}	Supply voltage
2	CLKO	Clock output
3	CLKI	Clock input
4	PRGD	Program control output
5	PRGC	Program control output
6	PRGB	Program control output
7	PRGA	Program control output
8	PC	Program change, strobe output
9		
10	VOLU	Volume control output
11	ONOFF	Standby output
12		
13		
14		
15	RSIG	IR input
16		
17	V_{DD}	Supply voltage
18		

Pins 9, 12, 13, 14, 16, and 18 are not allowed to be connected.

Circuit description

1. IR receiver (pin RSIG)

The IR signal is received, decoded and forwarded to the control logic. The IR signal consists of ac pulses with a frequency of approx. 30 kHz and a duration of 0.5 ms per cycle. The instructions are transmitted as 7-bit words (1 start bit, 6 information bits). The IR signals are repeated approximately every 120 ms.

2. Analog value memory (output VOLU)

The analog value can be varied in approx. 60 stages. The variation speed corresponds to the repetition frequency of the repeat instructions (approx. 8 Hz). The analog value is generated as square-wave voltage with a frequency of approx. 1 kHz, whereby the duty cycle corresponds to the analog value. The analog voltage is generated in an external low pass filter.

If the supply voltage begins to rise at 0, the analog value is set in the start position ($\nu_{VOLU} = 1/3$, with $\nu = t_{high}/T$).

The output is set at a low level internally
- if the IC is in standby,
- for approx. 128 ms if a program + or program − instruction has been received, prior to issuing the high pulse of the PC output.

As long as the IC is in standby, instructions to the analog memory remain undecoded.

After switch-on from standby, the analog output is set in the start position.

3. Program memory (outputs and inputs PRGA, PRGB, PRGC, PRGD)

The program memory consists of a 4 bit ring counter to call 16 programs.

The 16 programs can be called via remote control by incrementing or decrementing with the ring counter.

If the supply voltage begins to rise at 0, the program outputs are set at LLLH. The outputs of the program memory can be used as inputs, as well. They can be set and reset by a low-ohmic external control.

Strobe output, program stepping input PC

When the program memory has received an instruction via remote control, a positive pulse appears at the output PC after a certain delay time. The volume output VOLU is muted as soon as the delay time starts. Muting is reverted with the trailing edge of the PC pulse (refer to timing diagram 1). A capacitor can be additionally connected to the output PC in order to prolong muting (up to approx. 0.5 sec.).

The same muting mode is present when the supply voltage begins to rise at zero, while pin ON/OFF is at a low level (refer to timing diagram 2).

Pin PC can also be used as input. If a positive potential is applied externally, the program counter will increment by 1 step. The external capacitor thereby acts in debouncing mode (refer to timing diagram 3). As "standby", the output is statically positive. The PC pulse appears only once per pressure on the according transmitter key.

4. Other control functions

Standby output/input
(pin ONOFF)

The output is controlled by an RS flipflop
The high level (standby) appears
— when the supply voltage is switched on
— when the instruction "standby" is received

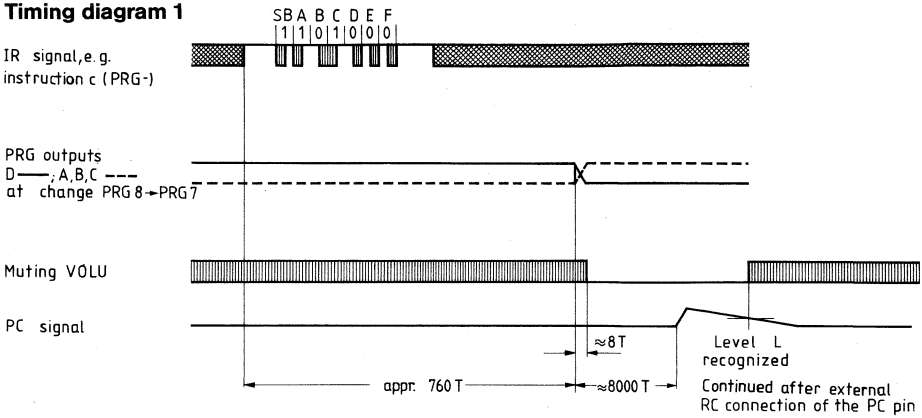
The low level (ON) appears, when the instruction program + or program — is received.

At low-ohmic control the pin ON/OFF also acts as input.

Instruction set for IR transmission

Instruction No.	Description
a	Standby
b	Program + /ON
c	Program — /ON
d	Vol +
e	Vol —
f	End instruction

Timing diagram 1

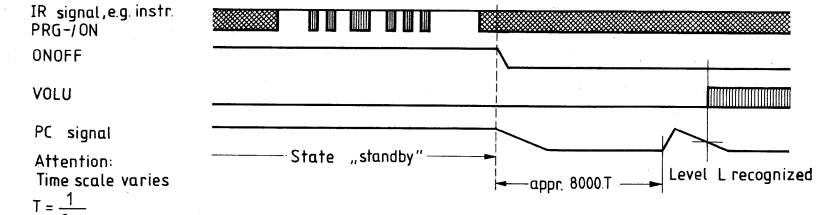


Attention: Time scale varied

$T = \frac{1}{f_{osc}}$

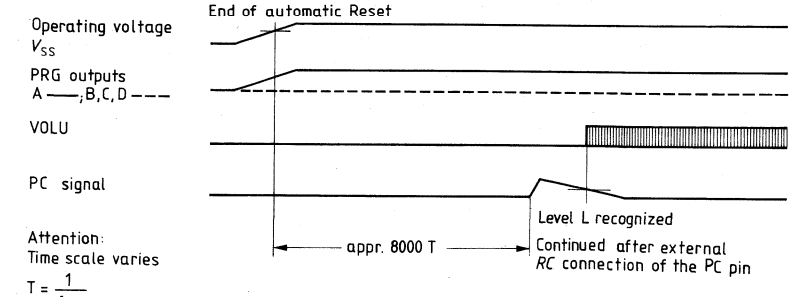
Timing diagram 2

Example a) Switching on by means of an IR instruction



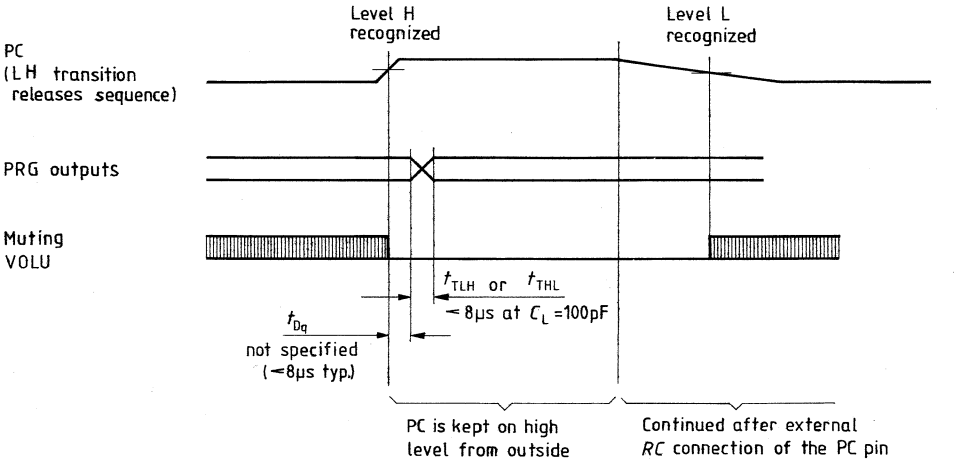
$T = \frac{1}{f_{osc}}$

Example b) ONOFF is connected to V_{DD} during the supply voltage rise via wiping contact

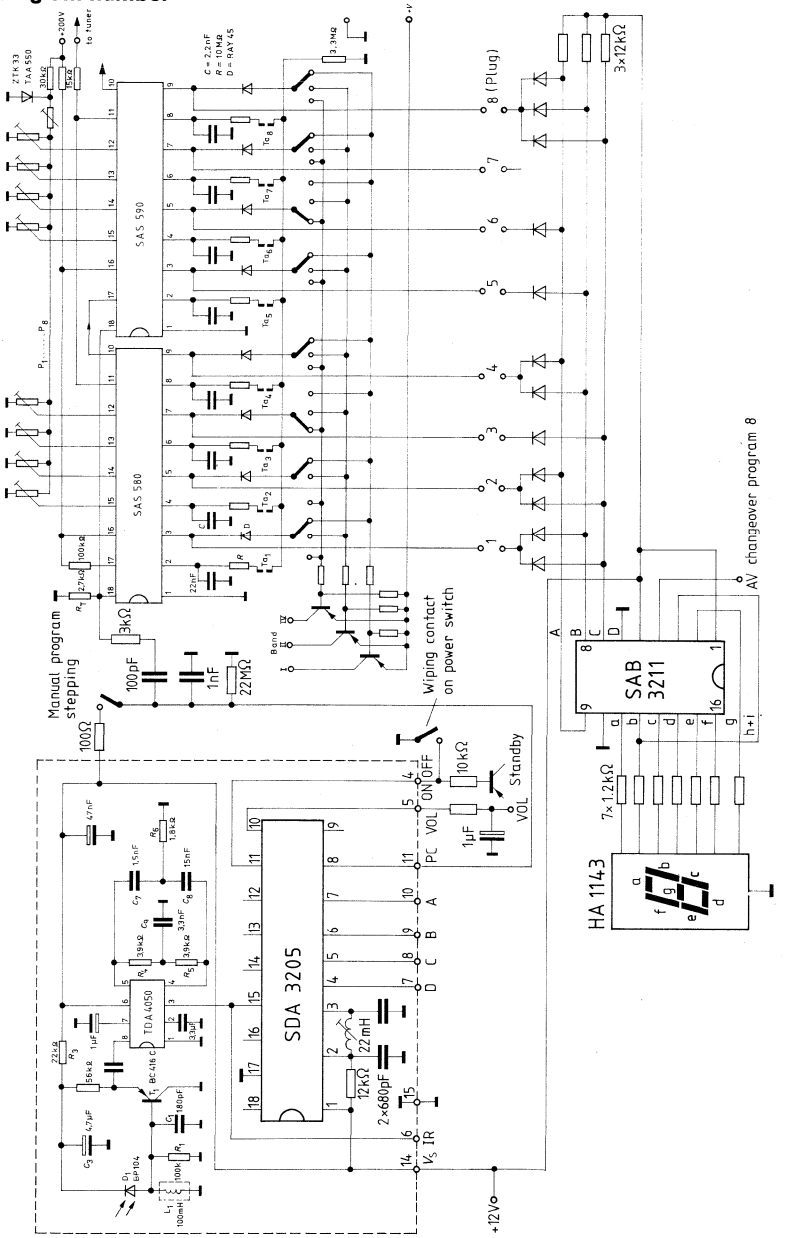


$T = \frac{1}{f_{osc}}$

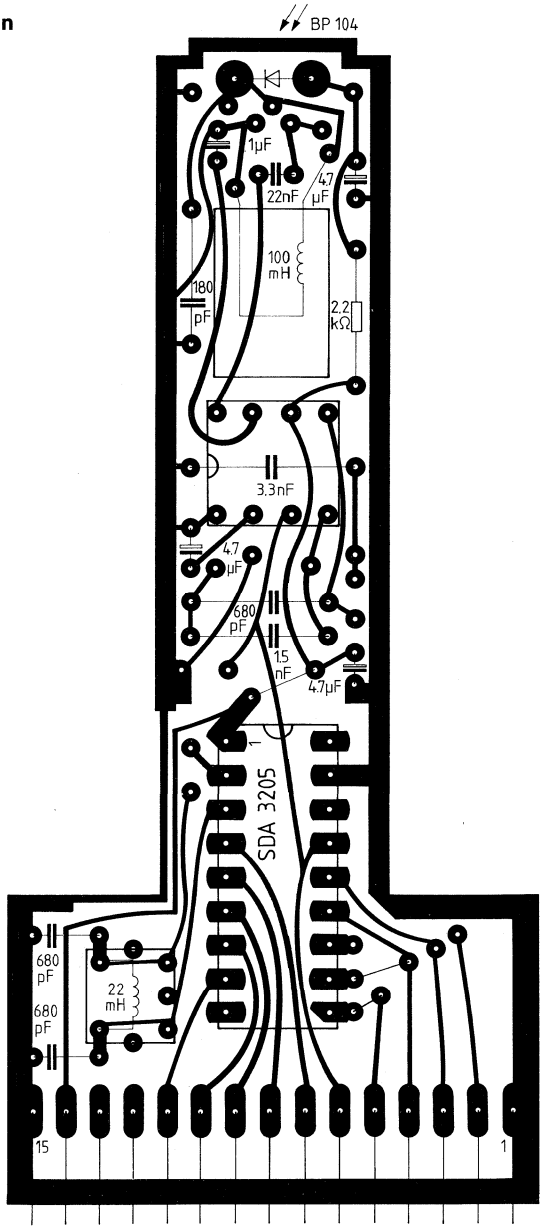
Timing diagram 3



Application circuit IR 60 V with program stepping and display of the program number



Plug-in location plan



MOS circuit

Type	Ordering code	Package outline
SDA 3206	Q 67100-Y 577	DIP 18

The SDA 3206 transmitter IC, developed in PMOS depletion technology, converts the input instructions into a 6-bit biphase code. The instructions are transmitted via an infrared transmitter stage onto an IR receiver stage of the SDA 3205.

Features

- Low current consumption of typically 3 mA (max. 5 mA). An external NPN transistor, controlled by the transmitter IC, disconnects the battery from the IC, thus substantially increasing the battery life time.
- 5 V to 10 V supply voltage

Maximum ratings (all voltages referred to $V_{DD} = 0$ V)

Supply voltage range	V_{SS}	−0.3 to 18	V
Input voltage range	V_i	V_{SS} −18 to V_{SS} +0.3	V
Total power dissipation	P_{tot}	500	mW
Power dissipation per output	P_q	100	mW
Storage temperature range	T_{stg}	−55 to 125	°C
Thermal resitance (system-air)	$R_{th\,SA}$	90	K/W

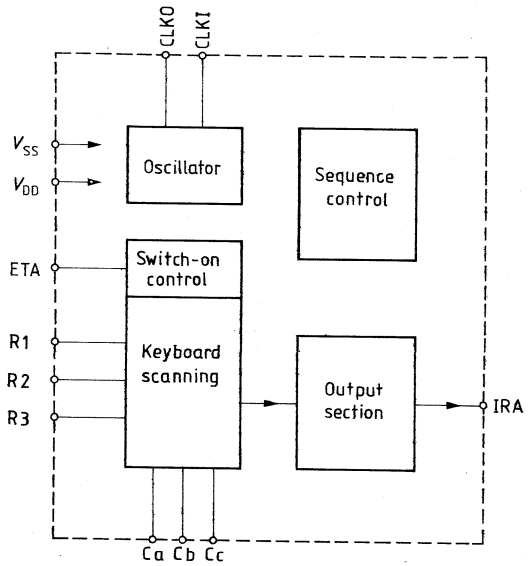
Operating range (referred to $V_{DD} = 0$ V)

Supply voltage range	V_{SS}	5 to 10	V
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics (all voltages referred to $V_{DD} = 0$ V)

		min	typ	max	
Current consumption without load	I_{DD}		3	5	mA
Oscillator					
Clock input CLKI					
H input voltage	V_{iH}	$V_{SS}-1$		V_{SS}	V
L input voltage	V_{iL}	0		$V_{SS}-4$	V
Clock output CLKO					
H output voltage	V_{qH}	$V_{SS}-1$		V_{SS}	V
L output voltage	V_{qL}	0		+1	V
Leakage current, total current					
of column output Ca, Cb, Cc, ETA, IRA ($V_q = -10$ V; $V_{SS} = 0$ V; $T_{amb} = 25°C$)				1	µA
Column resistors					
Ra, Rb, Rc towards $-V_S$	R_C	33		47	kΩ
Remote control signal — output IRA					
H output voltage ($I_{qH} = 4$ mA; $V_{SS} \geqq 6$ V)	V_{qH}	$V_{SS}-5$		V_{SS}	V
Switch-on transistor — output ETA					
H output current ($V_q = V_{SS} - 4$ V)	I_{qH}	0.1		0.5	mA

Block diagram



Pin configuration

Pin No.	Function
1	V_{SS}
2	Column a
3	Column b
4	Column c
5	
6	V_{DD}
7	ETA (switch-on transistor output)
8	IRA (infrared output)
9	Row 1
10	Row 2
11	Row 3
12	
13	
14	
15	
16	
17	CLKI (oscillator input)
18	CLKO (oscillator output)

Pins 5, 12, 13, 14, 15, 13 are not allowed to be connected.

Description of functions

Since the SDA 3206 operates at a wide range of supply voltage with low current consumption, it is suitable for battery supply. The IC contains a control output for an NPN transistor, which disconnects the IC from the battery if the keyboard is not activated.

Input keyboard

The transmitter includes an input matrix consisting of 3 columns and 3 rows. A column output has to be connected to a row input in order to input an instruction. As a result, the transmitter is switched on and a corresponding instruction is transmitted.

End instruction

After having actuated a key, the selected instruction is transmitted maximally one more time depending on the exact instant of the release. After the last transmission of the desired instruction the end instruction is transmitted which informs the receiver that the key has been released.

Output

The transmitter converts the incoming instruction into a biphase code (timing diagram 1). Prior to the 6 information bits, a start bit is transmitted.

The output signal is keyed with the clock frequency divided by 2 ($f_{CLK}/2$ approx. 30 kHz); the signal controls an infrared transmitter stage. The idling output is high-ohmic. Prior to an IR instruction, a presignal is released which facilitates the gain control in the IR preamplifier.

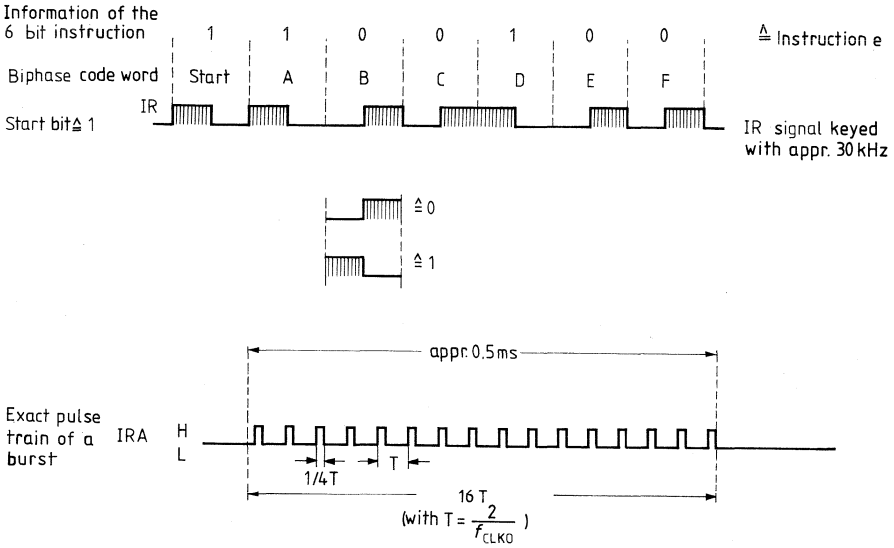
Timing

The clock frequency is set at 60 kHz. Instructions are transmitted at an interval of approx. 120 ms, with each of them lasting approx. 7 ms (timing diagram 1). The instructions cannot be recognized before a debounce time of 20 ms has elapsed.

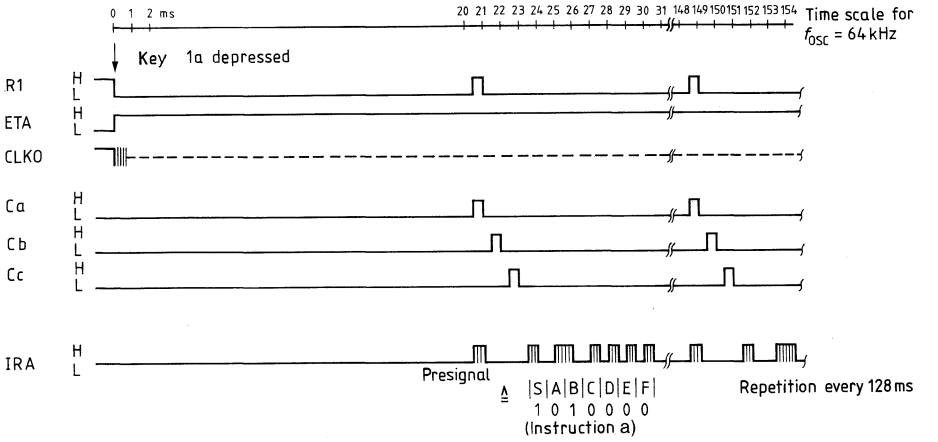
Instruction set with assignment of the instructions to the keys

Instruction	Code F E D	C B A	Logic operation
a	0 0 0	0 1 0	1c
b	0 0 0	1 0 0	2a
c	0 0 0	1 0 1	2b
d	0 0 1	0 0 0	3a
e	0 0 1	0 0 1	3b
f	1 1 1	1 1 0	End instruction

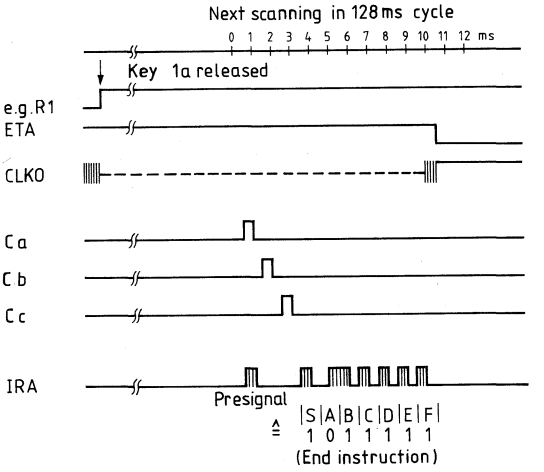
Timing diagram 1
(biphase coding without presignal)



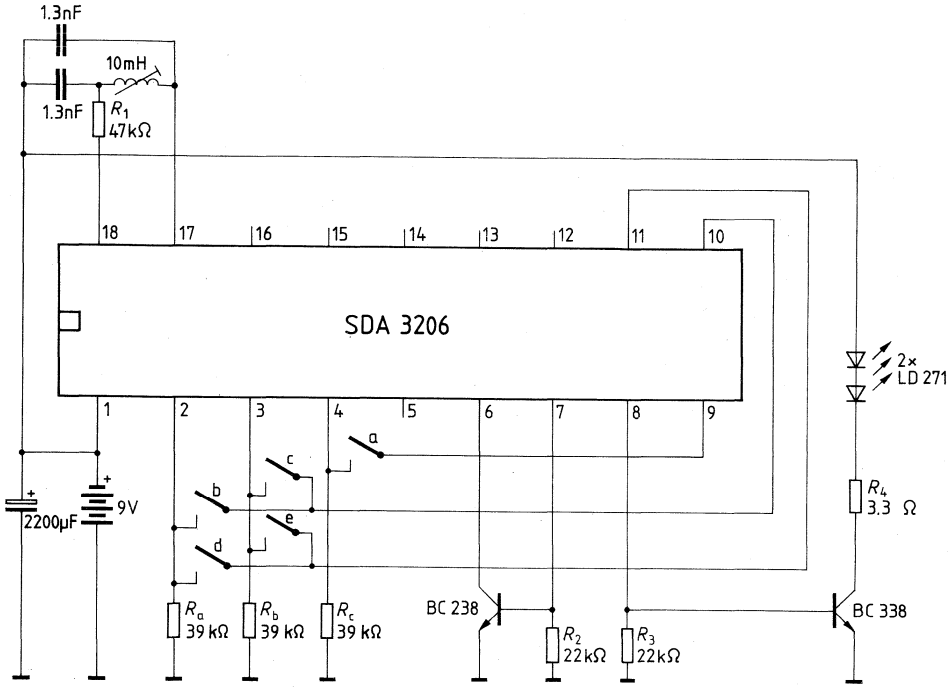
Timing diagram 2
(pressing a key)



Timing diagram 3
(releasing a key)



External connection
(example)



Bipolar circuit

Type	Ordering code	Package outline
SDA 4040	Q 67000-A 1462	DIP 14

Fast ECL divider with a divider ratio 1:256 for input frequencies of 80 MHz up to 1 GHz. Particularly suitable for use in TV sets with frequency synthesis.

Features

- Input frequency up to 1 GHz
- Few external components
- Separate inputs for UHF and VHF

Maximum ratings

Supply voltage	V_1, V_2	10	V
Input voltages (peak-to-peak)	V_8	2.5	V
	V_{10}	2.5	V
Switching voltage range	V_{14}	−0.5 to 7.2	V
Switching current	I_{14}	−10	mA
Output current range	I_{Q4}	−30 to 30	mA
Junction temperature	T_j	125	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	80	K/W

Operating range

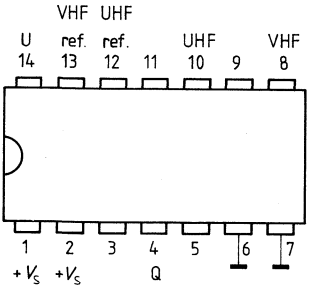
Supply voltage range	V_1, V_2	6.45 to 7.15	V
Input frequency range VHF	f_{i8}	80 to 300	MHz
UHF	f_{i10}	80 to 950	MHz
Ambient temperature range	T_{amb}	0 to 65	°C

■ Not for new design

Characteristics ($V_S = 6.8$ V; $T_{amb} = 25$ °C)

		min	typ	max	
Current consumption ($V_S = 7.15$ V)	I_1, I_2		70	95	mA
Input voltages VHF (sine)[1]					
$f_i =$ 80 MHz	V_{8rms}	200		700	mV
$f_i = 100$ MHz	V_{8rms}	100		700	mV
$f_i = 300$ MHz	V_{8rms}	100		700	mV
Input voltages UHF (sine)[1]					
$f_i =$ 80 MHz	V_{10rms}	300		700	mV
$f_i = 100$ MHz	V_{10rms}	250		700	mV
$f_i = 200$ MHz	V_{10rms}	150		700	mV
$f_i = 450$ MHz	V_{10rms}	100		700	mV
$f_i = 900$ MHz	V_{10rms}	200		700	mV
L switching voltage	V_{14L}			0.4	V
H switching voltage	V_{14H}	2.4			V
Switching current ($V_{14} = 0.4$ V)	$-I_{14}$			0.8	mA
L output voltage ($I_{qL} = 5$ mA)	V_{qL4}			0.4	V
H output voltage ($I_{qH} = -1$ mA)	V_{qH4}	2.4	3.5		V

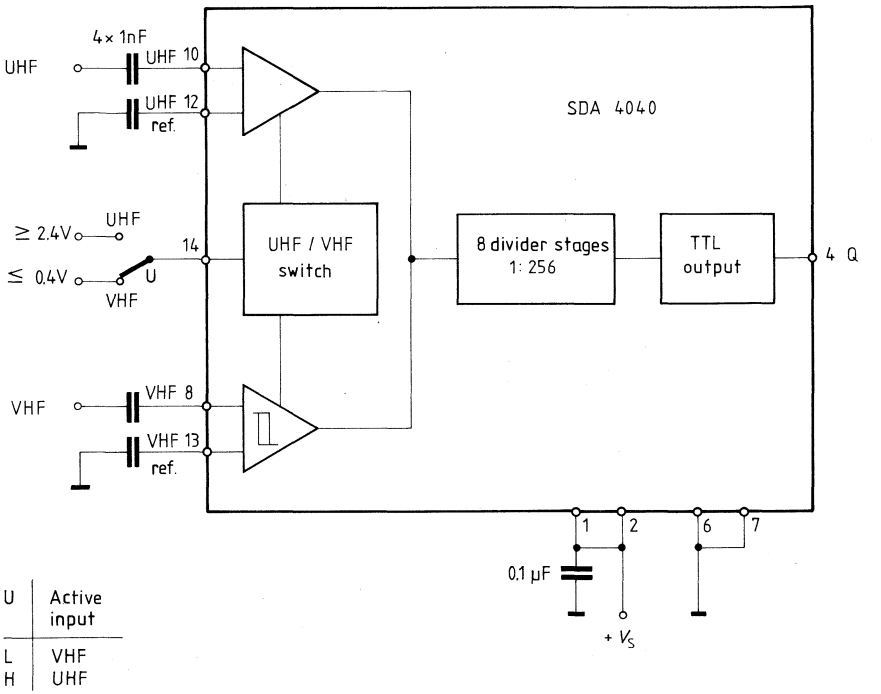
Pin configuration (top view)



1) For deviating ambient temperatures the input sensitivity may decrease down to 20%.

■ Not for new design

Block diagram and application circuit



If needed hysteresis can be achieved at the UHF input by connecting a resistor (e.g. 33 kΩ) between UHF_{ref} (pin 12) and ground (pins 6, 7). At the VHF input the hysteresis can be increased in the same way.

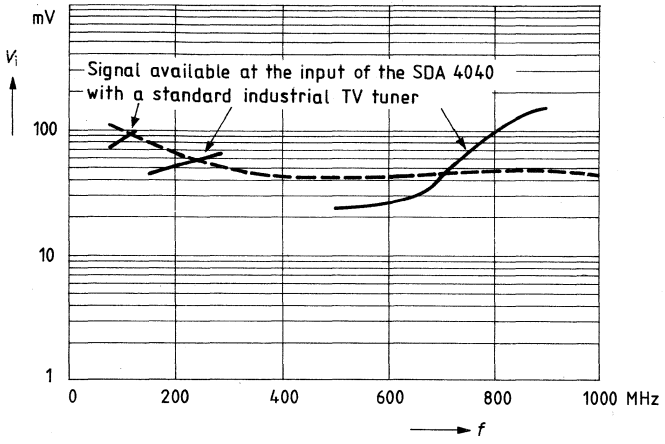
Circuit description

The IC SDA 4040 has been provided with a VHF and a UHF input. The VHF input is activated by applying "Low" to the switching input U. The UHF input is activated by applying "High" to pin U. The VHF input has a hysteresis of approx. 50 mV which improves the switching behavior during sine wave input signals of low frequencies. If necessary a hysteresis can be applied to the UHF input by means of an external resistor matrix.

The input signal is connected in a capacitive mode to the VHF or UHF input. The inputs are internally terminated with approx. 400 Ω. The pins VHF_{ref} and UHF_{ref} have to be grounded via capacitors (see application diagram).

■ Not for new design

Input sensitivity versus frequency



■ Not for new design

Bipolar circuit

Type	Ordering code	Package outline
SDA 4041	Q 67000-A 1463	DIP 18

The SDA 4041 is derived from the SDA 4040. It comprises two input amplifiers independent from each other as well as an 8-stage divider. This IC is particularly suitable for use in TV sets with frequency synthesis.

Features

- Input frequency up to 1 GHz
- Few external components
- Separate inputs for UHF and VHF
- ECL outputs

Maximum ratings

Supply voltage	V_S	6	V
Input voltages	V_4	2.5	V_{pp}
	V_5	2.5	V_{pp}
Switching voltage range	V_2	−0.5 to 20	V
Switching current	$-I_2$	10	mA
Junction temperature	T_j	125	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	65	K/W
(system-case)	$R_{th\,SC}$	20	K/W

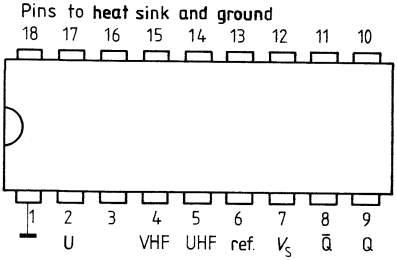
Operating range

Supply voltage range	V_S	4.7 to 5.5	V
Input frequency range VHF	f_{i4}	80 to 300	MHz
UHF	f_{i5}	80 to 950	MHz
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics ($V_S = 5$ V; $T_{amb} = 25$°C)

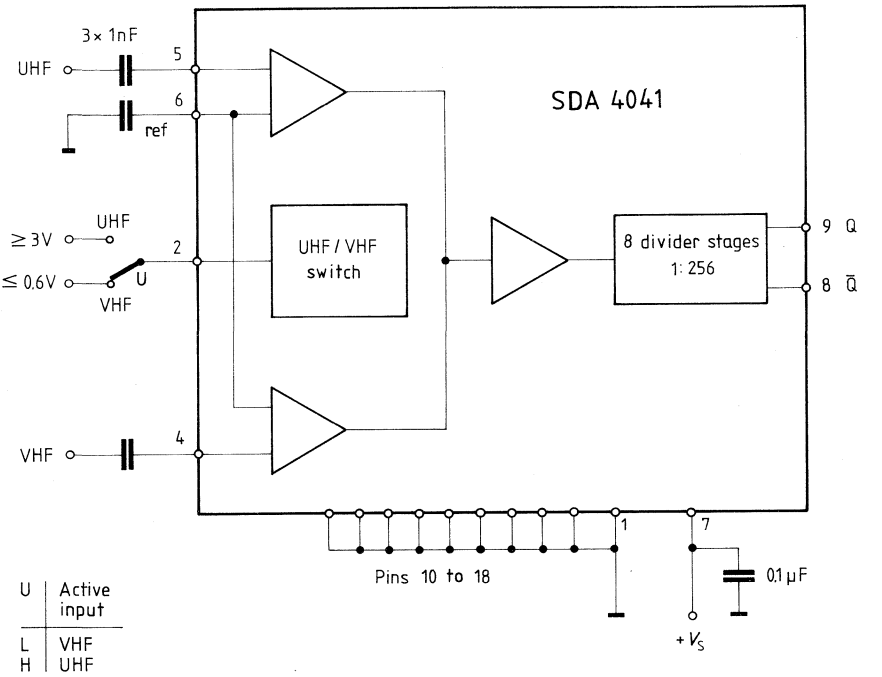
		min	typ	max	
Current consumption	I_7		95	130	mA
Input voltages VHF (sine)[1]					
$f_i =$ 80 MHz	$V_{4\,rms}$	40		500	mV
$f_i = 100$ MHz	$V_{4\,rms}$	30		500	mV
$f_i = 300$ MHz	$V_{4\,rms}$	20		500	mV
Input voltages UHF (sine)[1]					
$f_i =$ 80 MHz	$V_{5\,rms}$	40		500	mV
$f_i = 100$ MHz	$V_{5\,rms}$	30		500	mV
$f_i = 300$ MHz	$V_{5\,rms}$	20		500	mV
$f_i = 450$ MHz	$V_{5\,rms}$	20		500	mV
$f_i = 900$ MHz	$V_{5\,rms}$	40		300	mV
L switching voltage	V_{2L}			0.6	V
H switching voltage	V_{2H}	3			V
Switching current ($V_2 = 12$ V)	$-I_2$		1.5		mA
Output voltages (peak-to-peak)	V_{q8}, V_{q9}	0.75	1.0		V
Output resistance	R_{q8}, R_{q9}		250		Ω

Pin configuration (top view)



1) For deviating ambient temperatures the input sensitivity may decrease down to 20%.

Block diagram and application circuit



Pins 10 to 18 are internally interconnected by means of a metal web. They are also connected to the chip body and intended for cooling and ground connection.

Circuit despriction

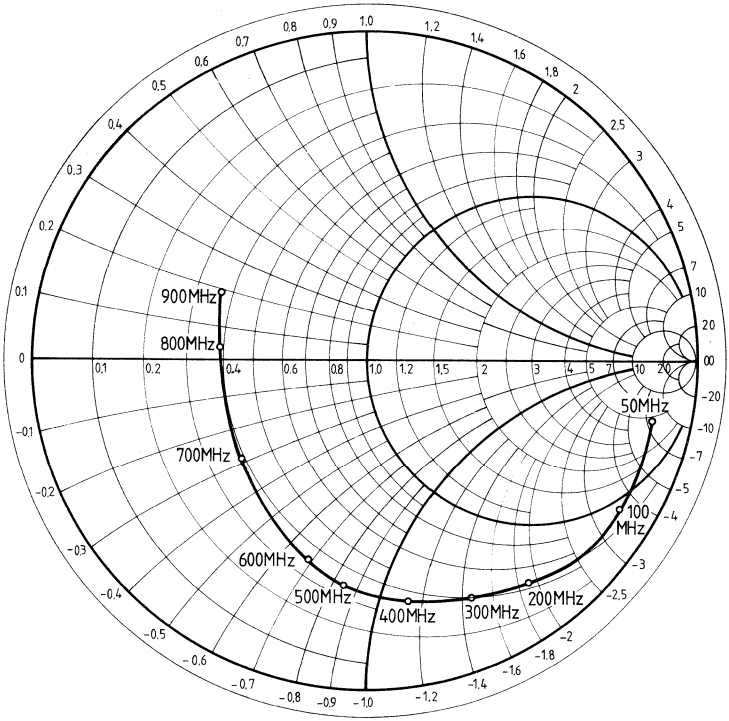
The IC SDA 4041 has been provided with a VHF and a UHF input. The VHF input is activated by applying "Low" to the switching input U. The UHF input is activated by applying "High" to pin U.

The input signal is connected in a capacitive mode to the VHF or UHF input. The connection "ref" has to be grounded. Preamplifiers at the inputs provide a high input sensitivity.

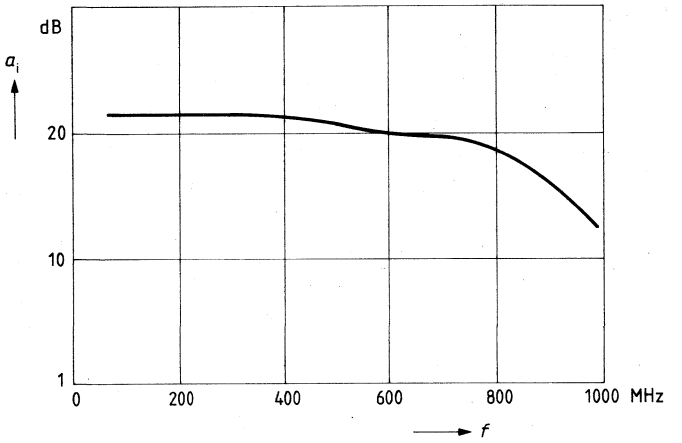
The outputs are antiphased and provide the ECL level.

Input reflection factor

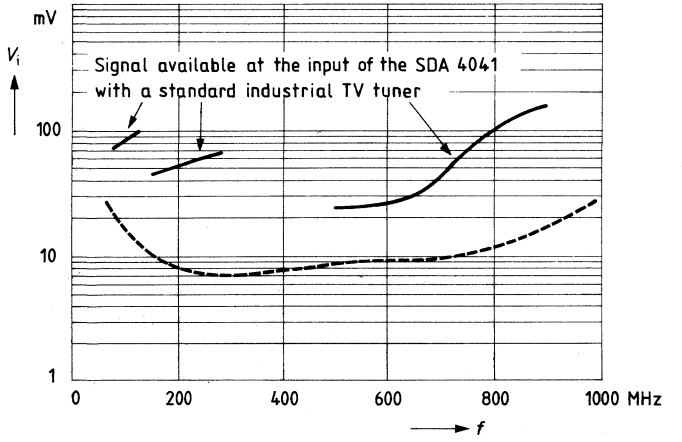
for determining the input impedance for the VHF as well as UHF input
$Z_o = 75\ \Omega$



Decoupling of VHF and UHF input versus input frequency



Input sensitivity versus input frequency



Preliminary data

Bipolar circuit
MOS handling

Type	Ordering code	Package outline
SDA 4042	Q67000-A1892	DIP 8

The SDA 4042 has been designed for application in TV receivers using the frequency control of the frequency synthesis concept. It includes a switchable preamplifier and an ECL divider with a 1:256 divider ratio and symmetrical ECL push-pull outputs. The frequency range can be extended up to 1.1 GHz.

Maximum ratings

Supply voltage	V_S	6	V
Input voltages (peak-to-peak)	V_{i1}, V_{i2}	2.5	V
Divider outputs	V_{q1}, V_{q2}	V_S–2 to V_S	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	–40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	115	K/W

Operating range

Supply voltage range	V_S	4.5 to 5.5	V
Input frequency range	f_i	80 to 1100	MHz
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics ($V_S = 4.7$ to 5.5 V; $T_{amb} = 0$ to 70 °C)

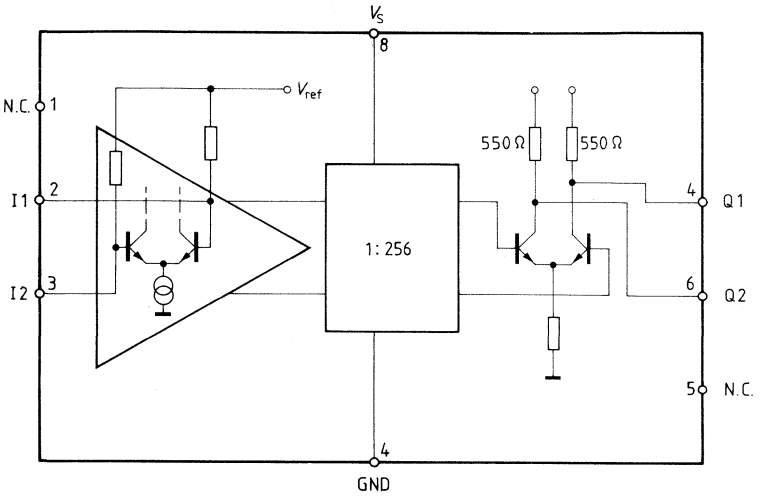
		min	typ	max	
Current consumption inputs blocked, outputs free	I_S			80	mA
Input level ("input sensitivity")	V_{i1}				
80 MHz		−27		3	dBm
120 MHz		−30		3	dBm
250 MHz		−32		3	dBm
600 MHz		−23		3	dBm
900 MHz		−23		3	dBm
1000 MHz		−15		3	dBm
Output voltage swing (peak-to-peak) $C_{load} = 15$ pF	V_{q1}, V_{q2}	0.5	1.0		V

Circuit description

The amplifiers of the IC features symmetrical push-pull inputs. When driving one signal input in an asymmetrical mode, the second input should be grounded by a capacitor with a low series inductance.

The divider of the IC consists of several status-controlled master-slave flipflops with a 1 : 256 divider ratio. The symmetrical push-pull outputs of the divider have an internal resistance of 550 Ω each. The DC voltage level of the outputs is connected to the supply voltage $+V_S$ (high $= +V_S$); the output swing is 1 V (peak-to-peak).

Block diagram

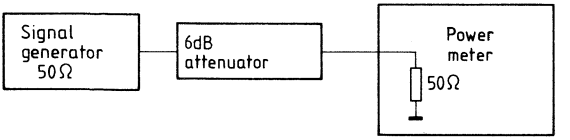


Pin configuration

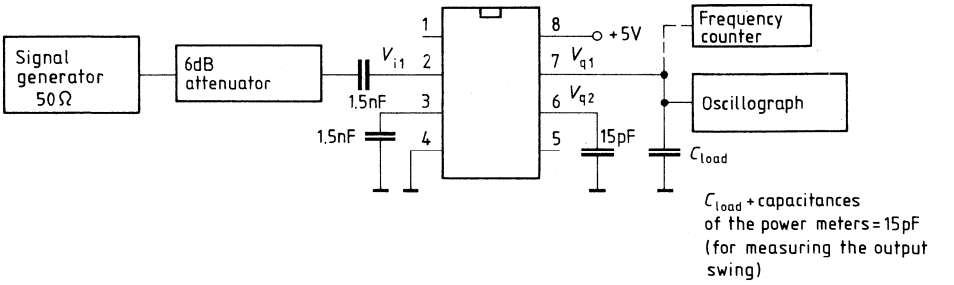
Pin No.	Symbol	Function
1	N.C.	Not connected
2	I1	Input 1
3	I2	Input 2
4	GND	Ground
5	N.C.	Not connected
6	Q2	Divider output 2
7	Q1	Divider output 1
8	$+V_S$	Supply voltage

Test and measurement circuit

Calibration of the signal generator



Measurement of the input sensitivity and the output swing



Bipolar circuit

Type	Ordering code	Package outline
TBA 120 S	Q67000-A657	DIP 14
TBA 120 AS	Q67000-A716	QUIP 14

The symmetrical 8-stage amplifier with symmetrical coincidence demodulator for amplifying, limiting, and demodulating frequency-modulated signals is especially suited for the sound IF section in TV sets and FM IF amplifiers in radio sets.

Features

- Outstanding limiting characteristics
- Wide range of operation (6 to 18 V)
- Few external components
- Voltage for AFC

Maximum ratings

Supply voltage[1]	V_S	18	V
Z current	I_{12}	15	mA
$t \leqq 1$ min	I_{12}	20	mA
Voltage	V_5	4	V
Current	I_3	5	mA
	I_4	2	mA
Storage temperature range	T_{stg}	−40 to 125	°C
Junction temperature	T_j	150	°C
Thermal resistance (system-air)	$R_{th\,SA}$	90	K/W

Operating range

Supply voltage range	V_S	6 to 18	V
Ambient temperature range	T_{amb}	−15 to 70	°C
Frequency range	f	0 to 12	MHz

1) The IC is not allowed to be plugged in or out when the supply voltage is switched on.

■ Not for new design

Characteristics ($T_{amb} = 25\,°C$, $V_S = 12\,V$; $f_{IF} = 5.5\,MHz$ or $10.7\,MHz$, respectively)

		min	typ	max	
Current consumption $R_5 = \infty$	I_S	10	14	18	mA
$R_5 = 0$	I_S	11	15.2	20	mA
IF voltage gain	G_V		68		dB
IF output voltage at limiting (each output)	$V_{q\,pp}$	170	250		mV
Output resistance (pin 8)	$R_{q\,8}$	1.9	2.6	3.3	kΩ
Bridging resistance	$R_{13\text{-}14}$			1	kΩ
AGC range of volume control	$\frac{V_{AF\,max}}{V_{AF\,min}}$	70	75		dB
DC level of output signal	V_8	6.2	7.4	8.5	V
Potentiometer resistance					
− 1 dB attenuation	R_5		3.7	4.7	kΩ
− 70 dB attenuation	R_5	1.0	1.4		kΩ
Voltage					
− 1 dB attenuation	V_5		2.4		V
− 70 dB attenuation	V_5		1.3		V
Signal-to-noise ratio ($V_i = 10\,mV$, $\Delta f = \pm 50\,kHz$)	$a_{S/N}$	75	85		dB
Total harmonic distortion ($V_i = 10\,mV$, $\Delta f = \pm 25\,kHz$)	THD		1.3	2.5	%
Noise voltage (in accordance with DIN 45405)	V_n		80	140	µV
Output resistance	$R_{q\,7\text{-}9}$		5.4		kΩ

Characteristics for $f_{IF} = 5.5\,MHz$ ($T_{amb} = 25\,°C$, $V_S = 12\,V$, $f_{IF} = 5.5\,MHz$, $\Delta f = \pm 50\,kHz$, $f_{mod} = 1\,kHz$, Q_B approx. 45)

AF output voltage ($V_i = 10\,mV$)	$V_{AF\,rms}$	0.7	1		V
Input voltage for limiting	$V_{i\,lim}$		30	60	µV
AM suppression $V_i = 500\,\mu V$, $m = 30\%$	a_{AM}	45	55		dB
$V_i = 10\,mV$, $m = 30\%$	a_{AM}	60	68		dB
Input impedance	Z_i		40/4.5		kΩ/pF

Characteristics for 10.7 MHz ($T_{amb} = 25\,°C$, $V_S = 12,\,V$, $f_{IF} = 10.7\,MHz$, $\Delta f = \pm 75\,kHz$, $f_{mod} = 1\,kHz$, Q_B approx. 45)

AF output voltage ($V_i = 10\,mV$)	$V_{AF\,rms}$	0.4	0.7		V
Input voltage for limiting	$V_{i\,lim}$		50	100	µV
AM suppression $V_i = 500\,\mu V$, $m = 30\%$	a_{AM}	40	50		dB
$V_i = 10\,mV$, $m = 30\%$	a_{AM}	60	68		dB
Input impedance	Z_i		20/4		kΩ/pF

■ Not for new design

Characteristics of the additive circuit

		min	typ	max	
Z voltage ($I_{12} = 5$ mA)	V_{12}	11.2	12	13.2	V
Z resistance	R_Z		30	55	Ω
Breakdown voltage	V_{CBO}	26	40		V
Breakdown voltage ($I_3 = 500$ µA)	V_{CEO}	13			V
Current gain ($V_{CE} = 5$ V, $I_C = 1$ mA)	G_I	25	80		

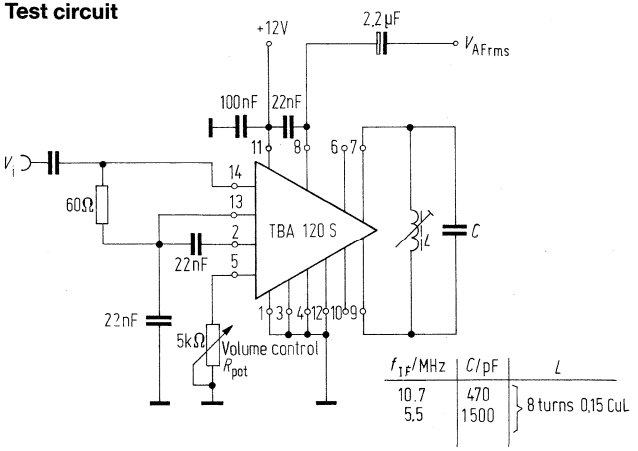
Pins 3 and 4 are connected to the collector or the base of a transistor, which may be used as an AF preamplifier ($I_C < 5$ mA) or as a bass/treble switch (dc on or off-switching of an *RC* circuit).

At pin 12, a Z diode (12 V) is accessible which can be used to stabilize the supply voltage of this IC or the voltage of other included circuit elements ($I_Z \leqq 15$ mA).

The IC TBA 120 S is manufactured in different groups according to the volume specifications. An attenuation of 30 dB requires a resistor to be switched to ground at pin 5 with a resistance value as allocated to the groups listed below. The group number is imprinted on the plastic package.

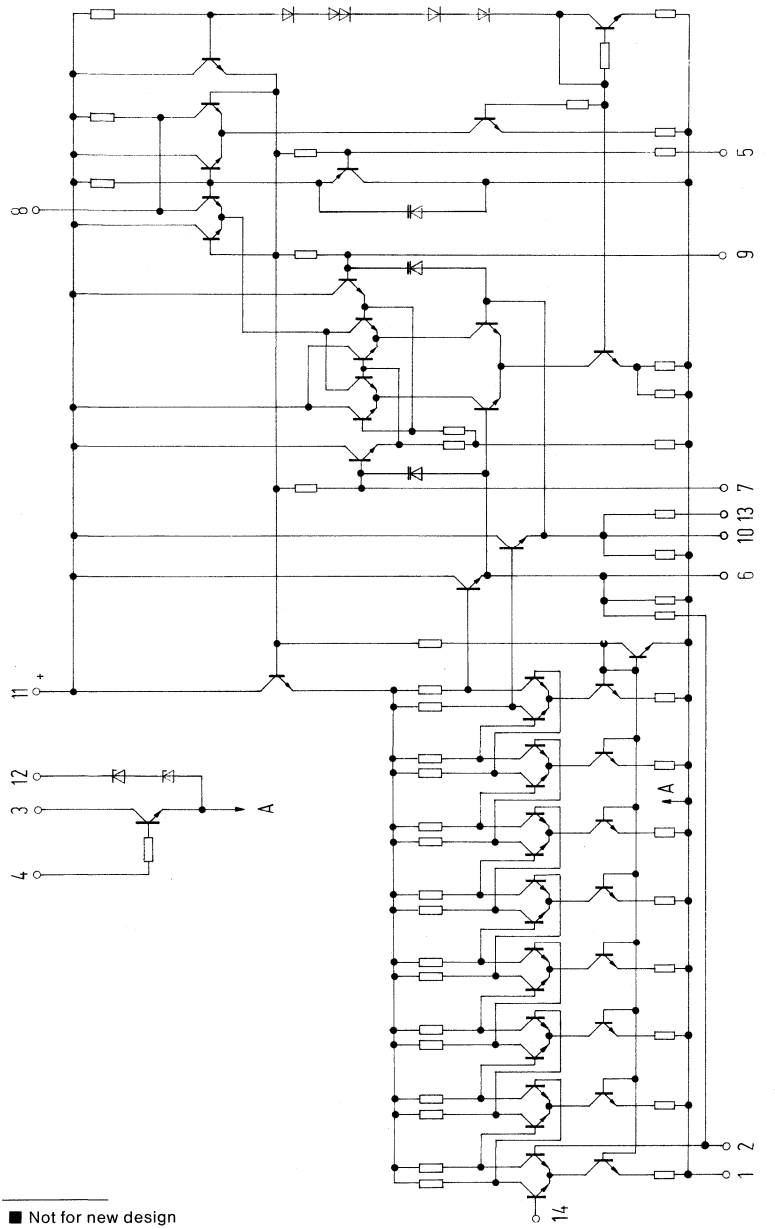
Group	II	III	IV	V
R_{pot}	1.9 to 2.2	2.1 to 2.5	2.4 to 2.9	2.8 to 3.3

Test circuit



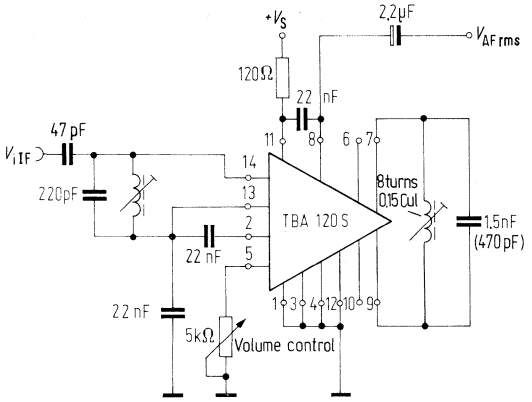
■ Not for new design

Circuit diagram



■ Not for new design

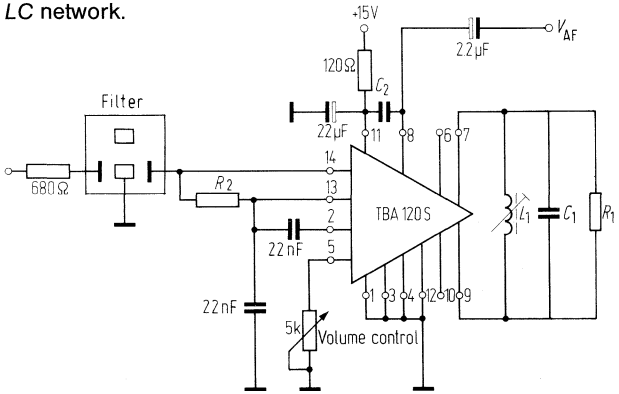
Application circuit 5.5 MHz (10.7 MHz)



Values in parentheses apply to 10.7 MHz

Application circuit with ceramic filter (Murata)

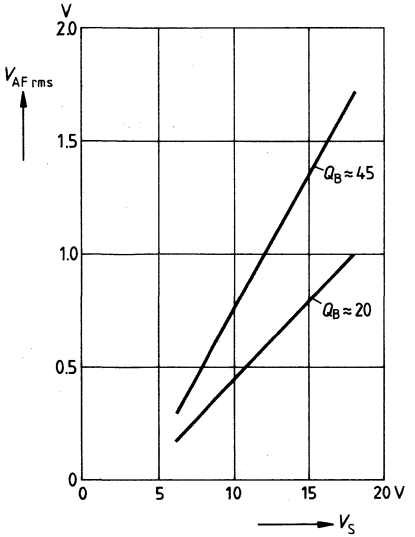
For good adjacent channel suppression the ceramic filter should be combined with an *LC* network.



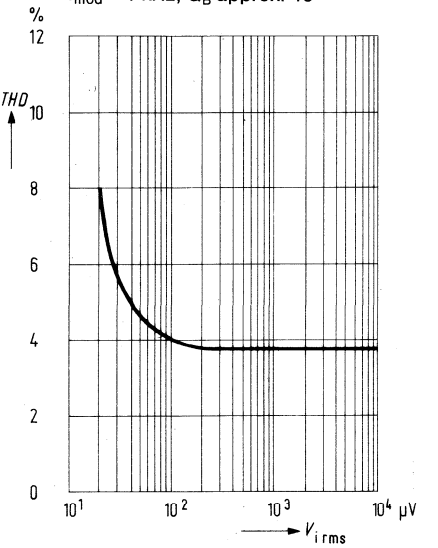
	Sound IF in TV sets	Sound IF in TV sets of American Std.	FM IF in radio mono sets	FM IF in RF stereo sets
C_1	1.5 nF	2.2 nF	470 pF	330 pF
C_2	22 nF	22 nF	22 nF	470 pF
L_1	8 turns, 0.15 CuL	8 turns, 0.15 CuL	8 turns, 0.15 CuL	12 turns, 0.15 CuL
R_1	∞	∞	∞	1 kΩ
R_2	680 Ω	1 kΩ	330 Ω	330 Ω
Filter (Murata)	SFE 5.5 MA	SFE 4.5 MA	SFE 10.7	SFE 10.7

■ Not for new design

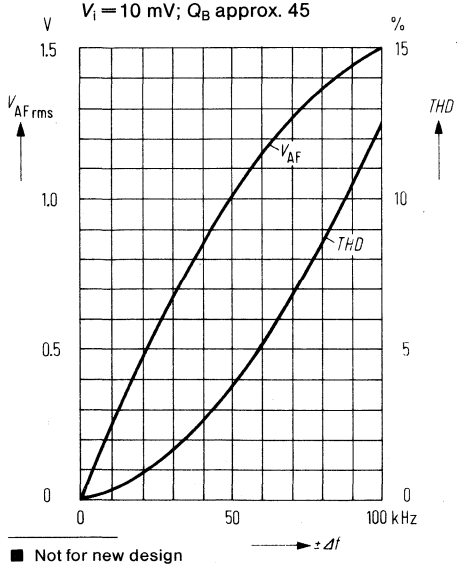
AF output voltage versus supply voltage
$f_Z = 5.5$ MHz; $\Delta f = \pm 50$ kHz,
$f_{mod} = 1$ kHz; $V_i = 10$ mV



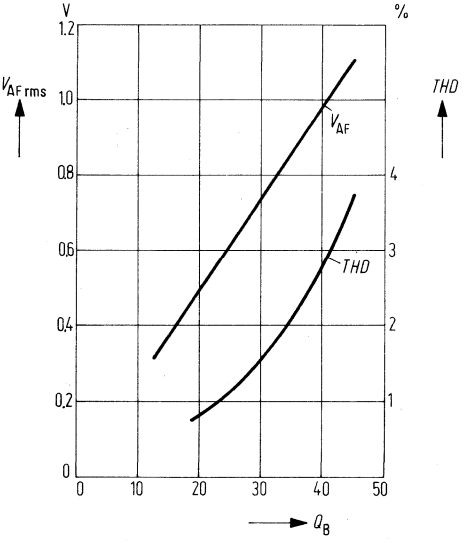
Total harmonic distortion versus input voltage
$V_S = 12$ V; $f_Z = 5.5$ MHz; $\Delta f = \pm 50$ kHz;
$f_{mod} = 1$ kHz; Q_B approx. 45



AF output voltage and total harmonic distortion v. frequency deviation
$V_S = 12$ V; $f_Z = 5.5$ MHz; $f_{mod} = 1$ kHz
$V_i = 10$ mV; Q_B approx. 45

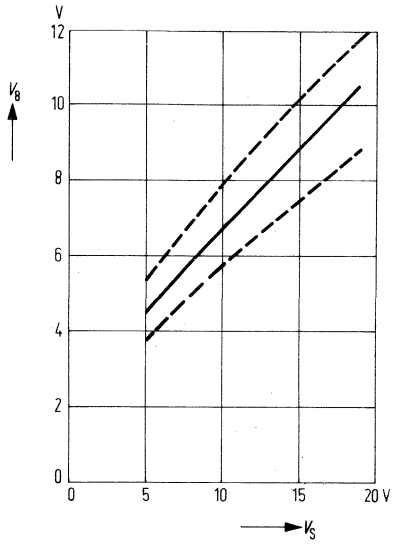


AF output voltage and total harmonic distortion versus Q_B factor
$V_S = 12$ V; $\Delta f = \pm 50$ kHz;
$f_{mod} = 1$ kHz; $V_i = 10$ mV

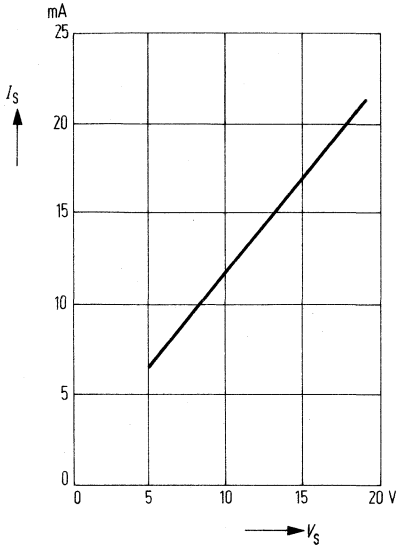


■ Not for new design

DC output voltage versus supply voltage

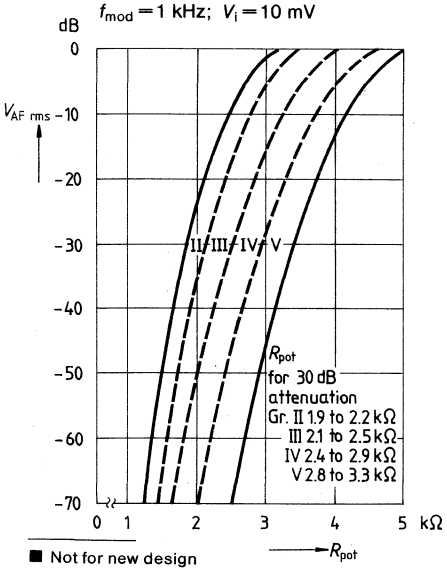


Current consumption versus supply voltage



Volume control versus potentiometer resistance

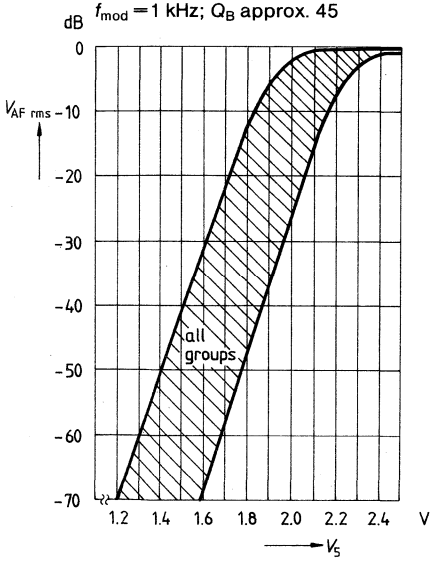
V_S = 12 V; f_Z = 5.5 MHz; Δf = ± 50 kHz
f_{mod} = 1 kHz; V_i = 10 mV



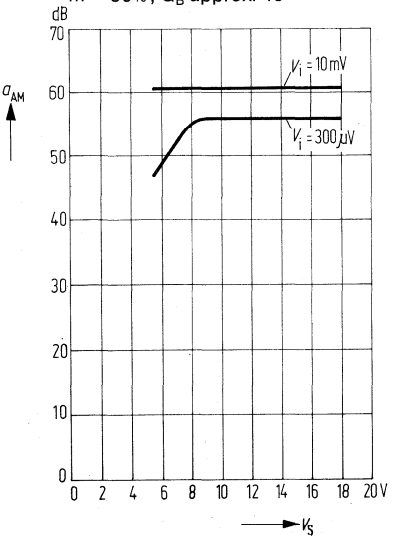
■ Not for new design

Volume control versus voltage to pin 5

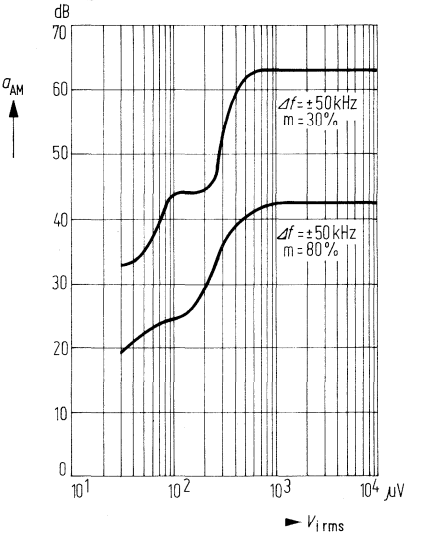
V_S = 12 V; f_Z = 5.5 MHz; Δf = ± 50 kHz
f_{mod} = 1 kHz; Q_B approx. 45



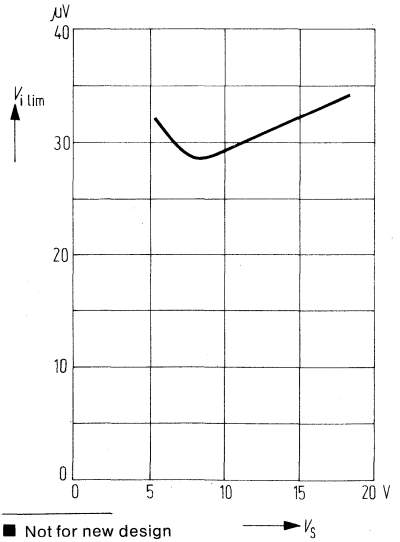
AM suppression versus supply voltage
$f_Z = 5.5$ MHz; $\Delta f = \pm 50$ kHz; $f_{mod} = 1$ kHz
$m = 30\%$; Q_B approx. 45



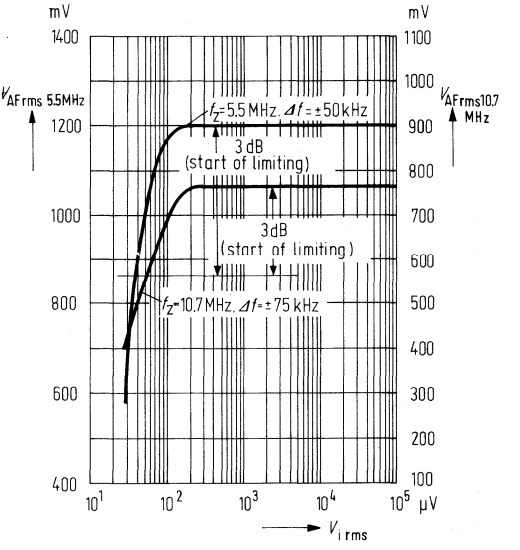
AM suppression versus input voltage
$V_S = 12$ V; $f_Z = 5.5$ MHz; $f_{mod} = 1$ kHz
Q_B approx. 45



Input voltage for limiting versus supply voltage
$f_Z = 5.5$ MHz; $\Delta f = \pm 50$ kHz;
$f_{mod} = 1$ kHz; Q_B approx. 45



AF output voltage versus input voltage
$V_S = 12$ V; $f_{mod} = 1$ kHz; Q_B approx. 45



■ Not for new design

FM IF Amplifier and Demodulator

TBA 120 T
TBA 120 U

Bipolar circuit

Type	Ordering code	Package outline
TBA 120 T	Q67000-A919	DIP 14
TBA 120 U	Q67000-A920	

The symmetrical 8-stage amplifier with symmetrical coincidence demodulator for amplifying, limiting, and demodulating frequency-modulated signals, is especially suited for the sound IF units in TV sets. In addition to the controlled AF output, an uncontrolled AF output and an AF input for the connection of video recorders is available.

Features

- Outstanding limiting qualities
- Few external components
- Terminal for video recorder
- AF output voltage independent of supply voltage
- Insensitive to hum
- Very little residual IF

TBA 120 T: Input and demodulator matched to ceramic resonators
TBA 120 U: Input and demodulator matched to *LC* networks.

Maximum ratings

Supply voltage	V_S	18	V
Voltage	V_5	6	V
Current	I_4	5	mA
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	90	K/W

Operating range

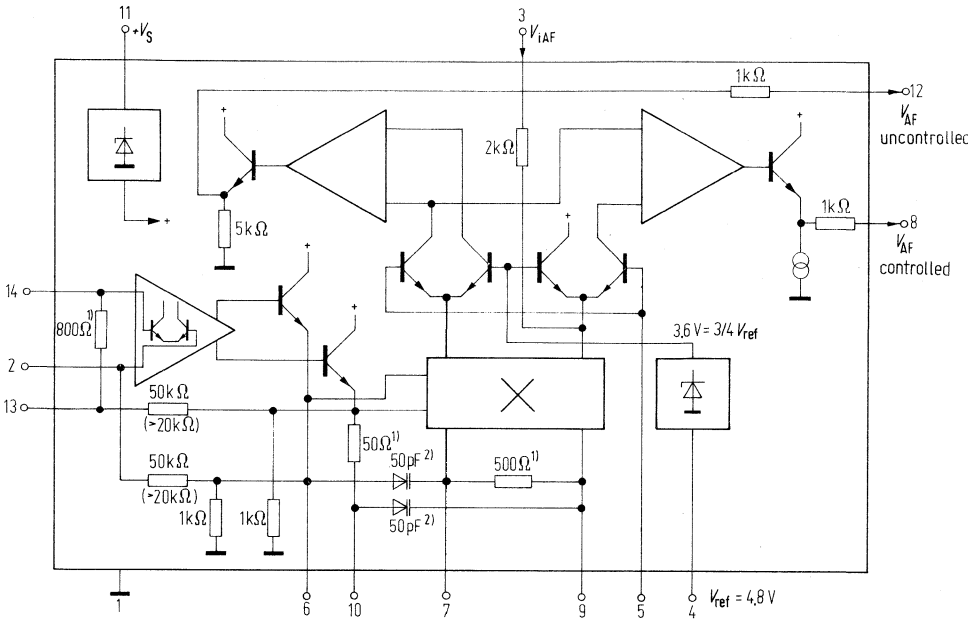
Supply voltage range	V_S	10 to 18	V
Ambient temperature range	T_{amb}	−15 to 70	°C
Frequency range	f	0 to 12	MHz

Characteristics ($V_S = 12$ V; $T_{amb} = 25$ °C, Q_B approx. 45, $f_{IF} = 5.5$ MHz)

		min	typ	max	
Current consumption	I_S	9.5	13.5	17.5	mA
IF voltage gain V_6/V_{14}	G_v		68		dB
IF output voltage with limiting at each output	V_{qpp}	175	250	325	mV
Output resistance	R_{q8}	0.8	1.1	1.4	kΩ
	R_{q12}	0.8	1.1	1.4	kΩ
Input resistance	R_{i3}	1.4	2.0	2.6	kΩ
Internal resistance	R_{i4}		12	16	Ω
DC level of output signal	V_8	3.4	4.0	4.7	V
($V_i = 0$)	V_{12}	4.4	4.9	6.3	V
Stabilized voltage	V_4	4.2	4.8	5.3	V
Residual IF voltage without deemphasis	V_8		20		mV
	V_{12}		30		mV
AF gain (AF not attenuated)	V_8/V_3	6	7.5	8.5	
Attenuation ($R_{4-5} = 5$ kΩ; $R_{5-1} = 13$ kΩ)	V_{AF8}	20	30	40	dB
Range of volume control	$\frac{V_{AF8\,max}}{V_{AF8\,min}}$	70	85		dB
Resistance	R_{4-5}[1]	1		10	kΩ
Input voltage for limiting ($\Delta f = \pm 50$ kHz; $f_{mod} = 1$ kHz)	$V_{i\,lim}$		30	60	µV
Hum suppression	V_8/V_{11}		35		dB
	V_{12}/V_{11}		30		dB
Signal-to-noise ratio ($V_i = 10$ mV)	$a_{S/N}$	80	85		dB
Noise voltage (in acc. with DIN 45405)	V_n			70	µV
Input impedance	R_{q7-9}		5.4		kΩ
TBA 120 T only:					
AF output voltage	$V_{8\,rms}$	650	900	1100	mV
($\Delta f = \pm 50$ kHz; $f_{mod} = 1$ kHz)	$V_{12\,rms}$	400	650	1000	mV
Input impedance	Z_i		800/5		Ω/pF
AM suppression	a_{AM}	50	60		dB
($V_i = 500$ µV; $\Delta f = \pm 50$ kHz; $m = 30\%$; $f_{mod} = 1$ kHz)					
Bridging resistance	R_{13-14}			1	kΩ
TBA 120 U only:					
AF output voltage	$V_{8\,rms}$	850	1200	1700	mV
($\Delta f = \pm 50$ kHz; $V_i = 10$ mV;	$V_{12\,rms}$	600	1000	1600	mV
$f_{mod} = 1$ kHz; $THD = 4\%$)					
Input impedance ($f_i = 5.5$ MHz)	Z_i	15/6	40/4.5		kΩ/pF
AM suppression	a_{AM}	50	60		dB
($\Delta f = \pm 50$ kHz; $V_i = 500$ µV; $f_{mod} = 1$ kHz; $m = 30\%$)					
Total harmonic distortion	THD		1.3	2.5	%
($\Delta f = \pm 25$ kHz; $V_i = 10$ mV; $f_{mod} = 1$ kHz)					

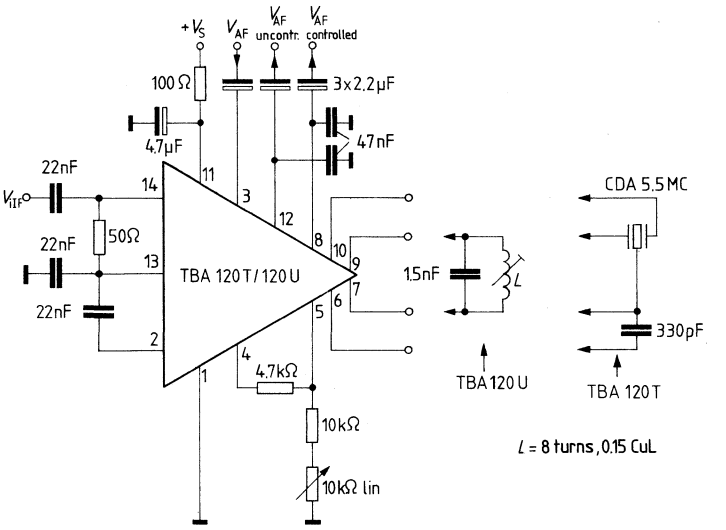
1) If DC volume control is not used, pin 4 has to be connected directly to pin 5.

Block diagram

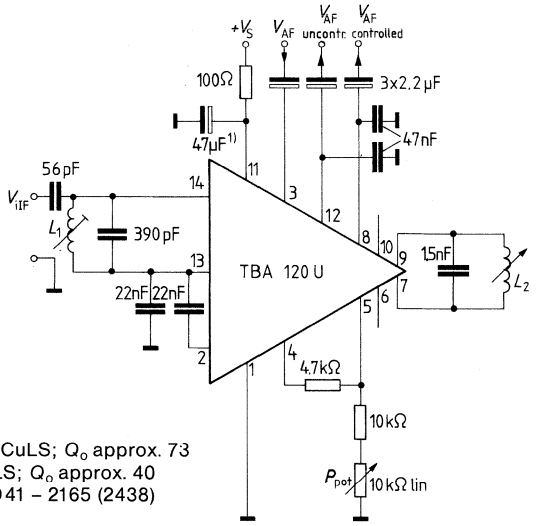


1) only TBA 120 T
2) only TBA 120 U

Test circuit (5.5 MHz)

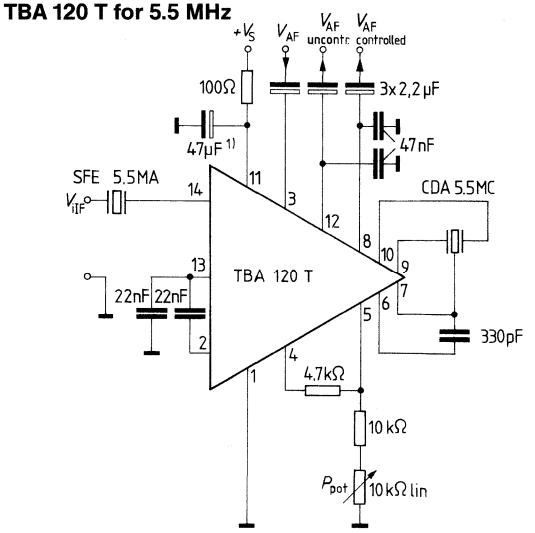


Application circuit TBA 120 U for 5.5 MHz



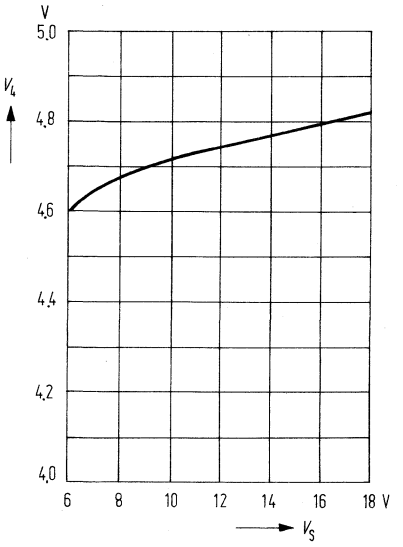
L_1: 20 turns 15x0.05 CuLS; Q_o approx. 73
L_2: 9 turns 0.25 CuLS; Q_o approx. 40
Coil assembly Vogt D41 – 2165 (2438)
without cup core

Application circuit TBA 120 T for 5.5 MHz

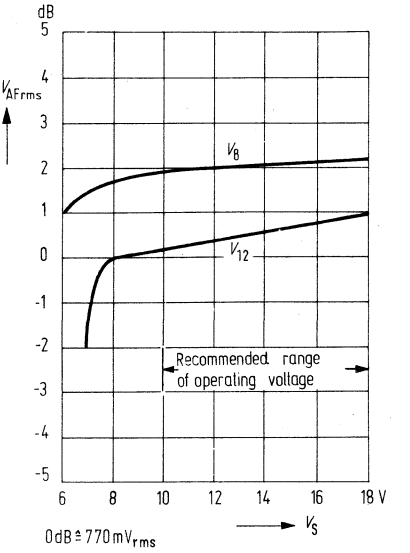


1) Omitting the electrolytic capacitor 47 µF at pin 11 changes the volume-control range.

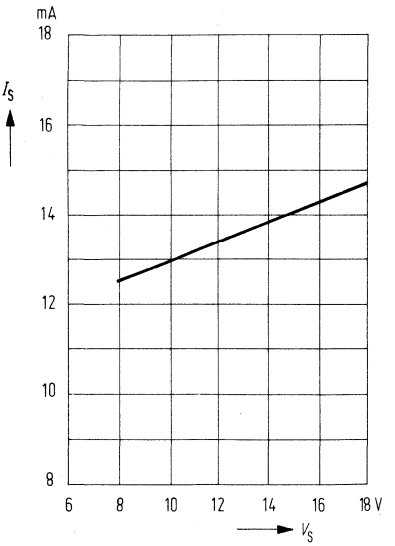
Z voltage versus supply voltage



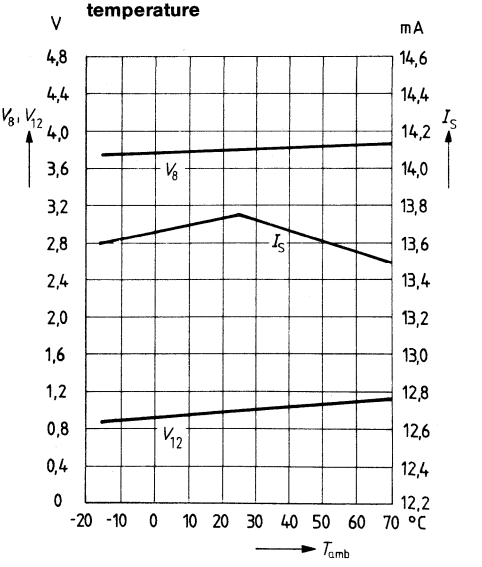
AF output voltage versus supply voltage



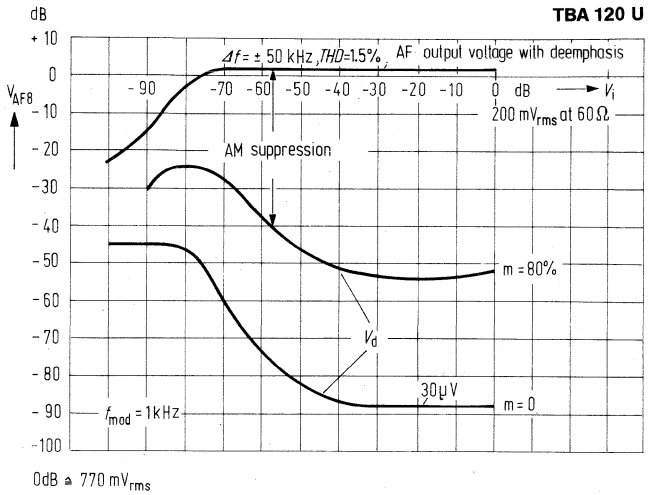
Current consumption versus supply voltage



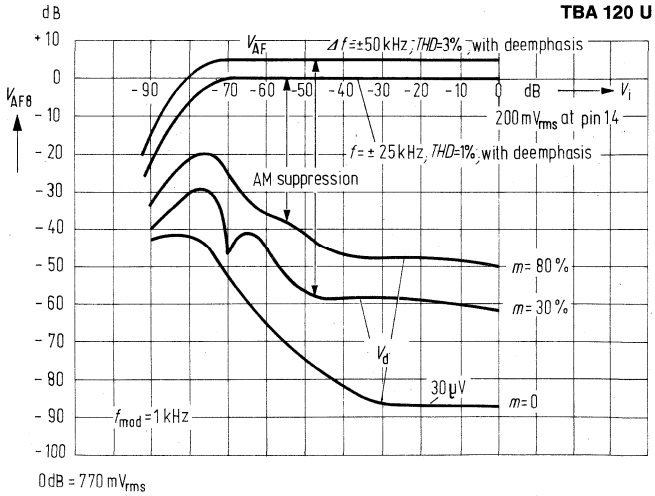
AF output voltage and current consumption versus ambient temperature



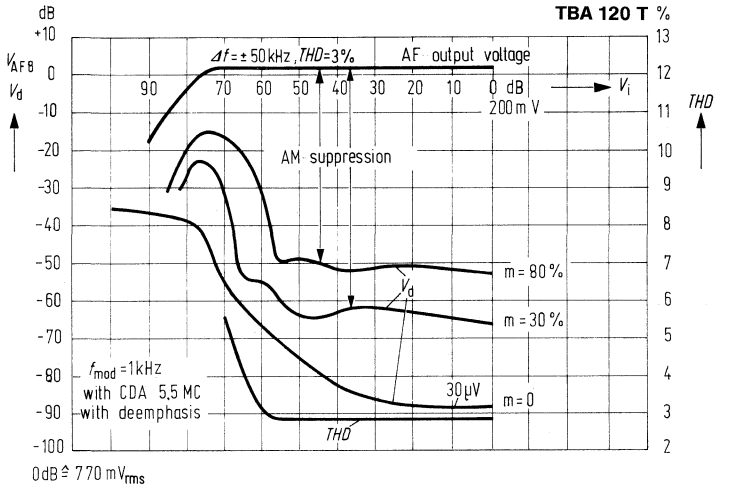
AF output voltage and disturbance voltage versus input voltage
(Input wired with SFE 5.5 MA/Murata)



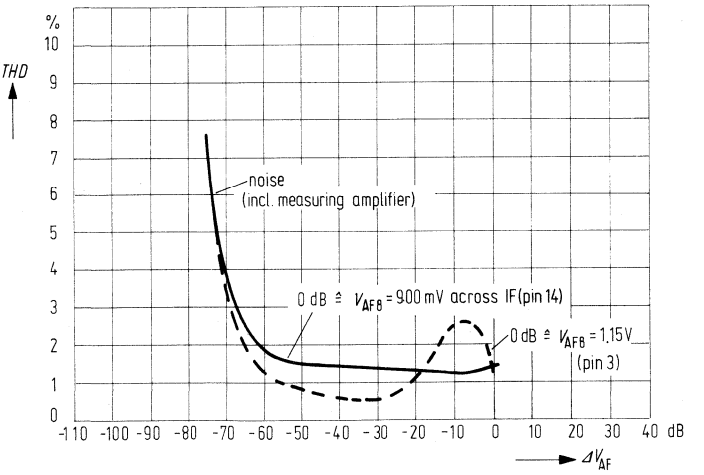
AF output voltage and disturbance voltage versus input voltage
(Input 60 Ω impedance broadband)



AF output voltage (pin 8), disturbance voltage, and total harmonic distortion versus input voltage

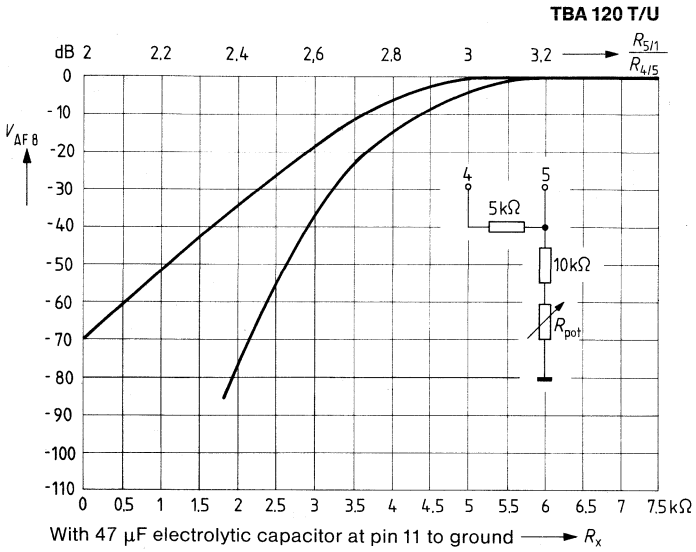


Total harmonic distortion versus volume control

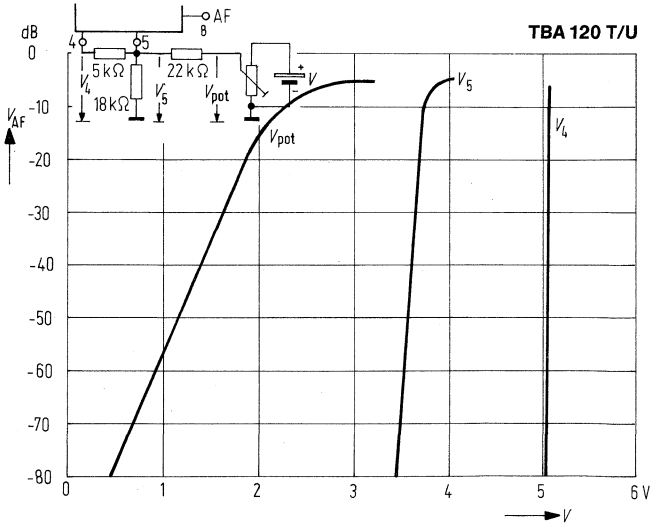


Spread

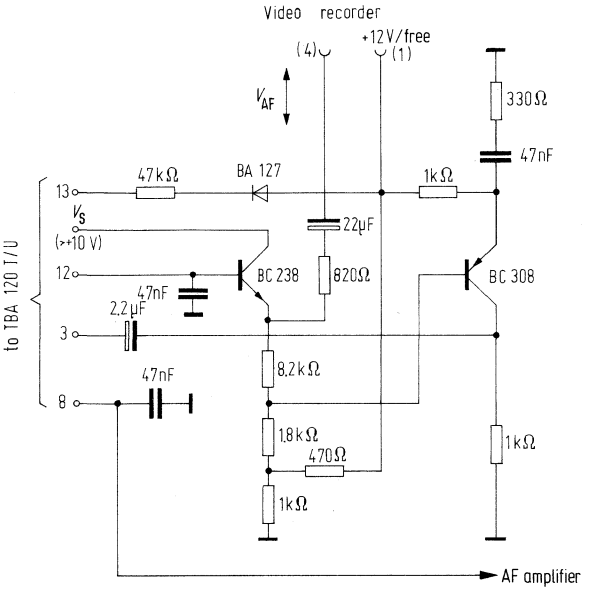
AF output voltage (pin 8) versus potentiometer resistance and versus ratio of resistance



AF output voltage (pin 8) versus voltage fed into pin 5



Circuit for direct connection to video recorders



Socket (1): Switching voltage: at playback +12 V
at recording: free
Socket (4): Simultaneous input and output for AF

Function

When the switching voltage is applied, the emitter follower BC 238 is blocked at the output, and the buffer stage BC 308 is switched on. A preemphasis is included to balance the deemphasis at the AF output. The IF amplifier becomes inoperable by means of the diode BA 127 and the 47 kΩ resistor. The remote-controlled volume regulator in the TBA 120 T/U is used for recording and playback.

Preliminary data **Bipolar circuit**

Type	Ordering code	Package outline
TBA 129	Q67000-A2330	DIP 8

This integrated circuit TBA 129 includes an 8-stage amplifier with a symmetrical demodulator to amplify, limit and demodulate frequency modulated IF signals. In addition, the IC is particularly suited for TV sound processing.

Features

- Excellent limiting qualities
- Few external components
- AF output voltage is independent of supply voltage
- Hum-resistant
- Negligible residual IF

Maximum ratings

Supply voltage	V_S	0 to 18	V
	V_1	0 to 3	V
	V_2	0 to 3	V
	V_4	0 to 3	V
	V_5	0 to 3.2	V
	V_6	0 to 3.2	V
Supply current	I_8	−1 to 1	mA
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	100 to 120	K/W

Operating voltage

Supply voltage range	V_S	10 to 18	V
Frequency range	f	0 to 12	MHz
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics ($V_S = 12$ V; $T_{amb} = 25$ °C)

		min	typ	max	
Current consumption	I_S	9.5	13.5	17.5	mA
IF voltage gain	G_v		68		dB
Input voltage for limiting start ($\Delta f = \pm 50$ kHz; $f_m = 1$ kHz)	$V_{i\,lim}$		30	60	µV
Output resistance	$R_{q\,8}$			100	Ω
DC voltage part of the output signal ($V_{iIF} = 0$ V)	V_8	3.4	4.0	4.7	V
IF residual voltage without deemphasis	V_8		30		mV
Hum suppression	$a_{hum\,7,8}$		30		dB
Signal-to-noise ratio ($V_i = 10$ mV)	$a_{S/N}$	80	85		dB
Input impedance	$Z_{i\,5\text{-}6}$		5.4		kΩ
AF output voltage ($\Delta f = \pm 50$ kHz; $f_m = 1$ kHz; $THD = 4\%$)	$V_{8\,rms}$	1	1.45		V
Input impedance ($f_{iIF} = 5.5$ MHz)	Z_i	15/6	40/4.5		kΩ/pF
AM suppression ($V_i = 500$ µV; $m = 30\%$)	a_{AM}	50	60		dB
Total harmonic distortion ($\Delta f = \pm 25$ kHz; $f_m = 1$ kHz; $V_i = 10$ mV)	THD		1.3	2.5	%

Circuit description

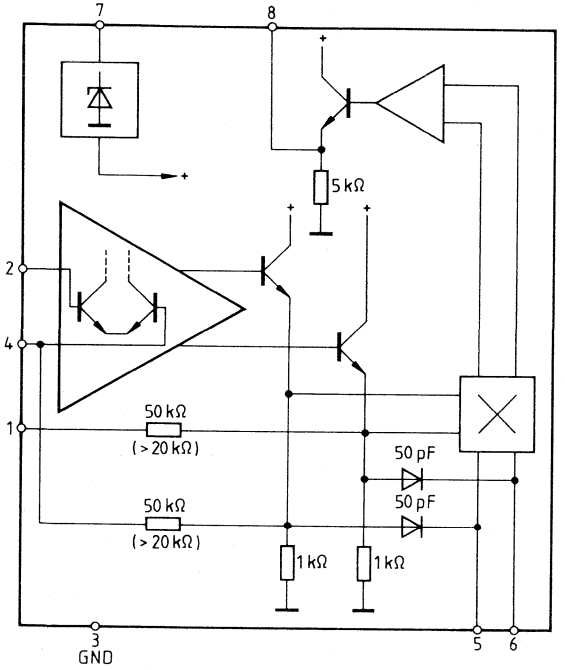
Symmetrical, 8-stage amplifier with symmetrical coincidence demodulator to amplify, limit, and demodulate frequency-modulated signals; especially suited for TV sound IF which need a low-ohmic AF output.

Application and data largely correspond to TBA 120 U.

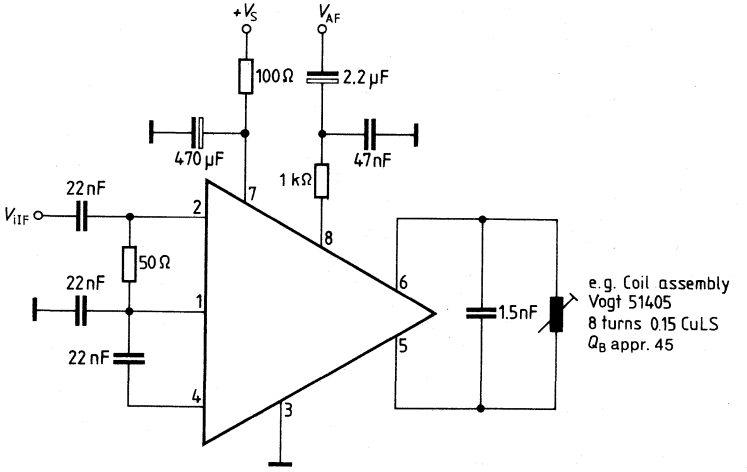
Pin configuration

Pin No.	Function
1	Operating point feedback
2	IF input
3	Ground
4	Operating point feedback
5	Tank circuit
6	Tank circuit
7	Supply voltage, plus
8	AF output

Block diagram



Test and measurement circuit



Type	Ordering code	Package outline
TBA 1440 G	Q67000-A1022	DIP 16
TBA 1441	Q67000-A1224	

Highly amplifying controlled video IF amplifier including controlled demodulator, low-ohmic video outputs for positive and negative signal, gated control, and delayed tuner control.

TBA 1440 G for PNP tuners
TBA 1441 for NPN tuners

Features

- High integration
- Large control range
- High input sensitivity
- Minimal 1.07 MHz disturbance
- Positive and negative signal
- Separate adjustment for white and black levels
- Excellent tuning behavior

Maximum ratings

Supply voltage	V_S	15[1])	V
Voltages	V_4	5	V
	V_5	20	V
	V_{14}	5	V
Ohmic resistance between pin 8 and 9	$R_{8\text{-}9}$	$\leqq 20$	Ω
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	90	K/W

Operating range

Supply voltage range	V_S	10.5 to 15	V
Ambient temperature range	T_{amb}	−25 to 60	°C

1) intermittently 16.5 V

Characteristics (V_{13} = 13 V; f_{IIF} = 38.9 MHz; T_{amb} = 25 °C; all data measured with respect to ground, unless otherwise stated)

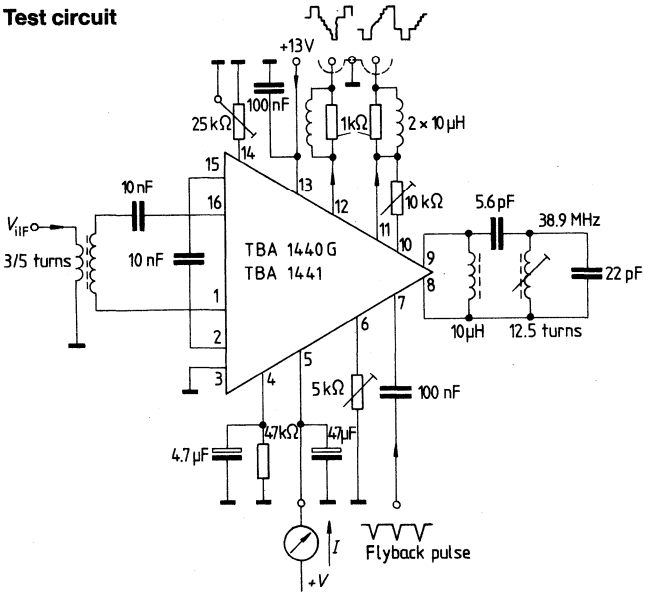
		min	typ	max	
Current consumption	I_{13}	33	42	61	mA
DC voltage at output 11 (V_{13} = 15 V; V_i = 0)					
$R_{14\text{-}3} = \infty$	V_{11}		5.5		V
$R_{14\text{-}3} = 0$	V_{11}		9.6		V
DC voltage at output 12 (V_{13} = 15 V; V_i = 0)					
$R_{14\text{-}3} = \infty$	V_{12}		1.9		V
$R_{14\text{-}3} = 0$	V_{12}		3.5		V
White level deviation	$\Delta V_{11}/\Delta V_{13}$		100		mV/V
	$\Delta V_{12}/\Delta V_{13}$		20		mV/V
Resistance for ΔV_{11} = 1 V	$R_{14\text{-}3}$		8.5		kΩ
AGC threshold V_{10} = sync pulse level for $R_{10\text{-}11} = 0$	$V_{10} = V_{11}$		1.9		V
Resistance for sync pulse level deviation of 1 V	$R_{10\text{-}11}$		2.4		kΩ
Sync pulse level with async or without gating pulses (peak level control)	$V_{11\,sync}$		0.5		V
Video output voltage	V_{video}		3		V
Control current for tuner prestage ($V_5 > 2$ V)	I_5	10	15		mA
(TBA 1440 G: 10 dB after AGC TBA 1441: 10 dB prior to AGC)					
IF control voltage for max gain	V_4	0		0.5	V
for min gain	V_4	2.5		5	V
Gating pulse voltage	$-V_7$	2		5	V
Residual IF (basic frequency)	$V_{11}; V_{12}$		10		mV
Output current to ground	$I_{11}; I_{12}$			5	mA
to plus	$I_{11}; I_{12}$			−1	mA
Input impedance at max gain	$Z_{1\text{-}16}$		1.8/2		kΩ/pF
at min gain	$Z_{1\text{-}16}$		1.9/0		kΩ/pF
Input voltage[1] for $V_{1\,pp}$ = 3 V	V_i	70	100	200	μV
Video bandwidth (−3 dB)	B_{video}	6	7		MHz
AGC range	ΔG		55		dB
Intermodulation ratio (1.07 MHz) with reference to color carrier[2]	a		45		dB
Output impedance	$Z_{q\,8\text{-}9}$		2/2.5		kΩ/pF

1) According to test circuit: V_i = rms sync pulse level at 60 Ω

2) Test level a_{cc} = − 3 dB

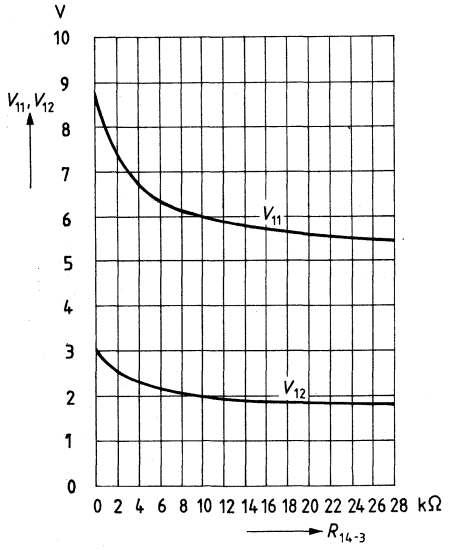
a_{sc} = −20 dB referred to picture carrier

Test circuit

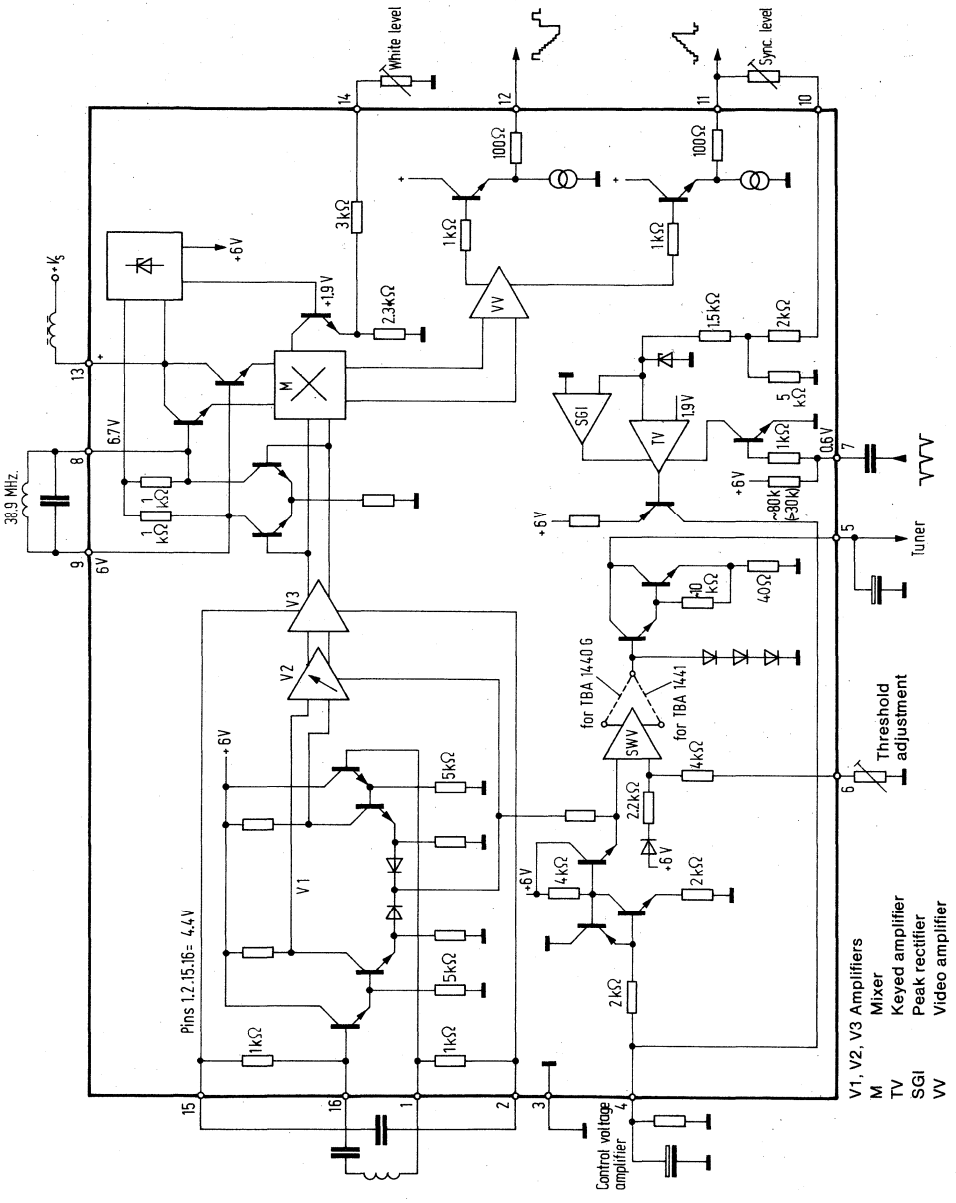


DC output voltage versus white level resistance

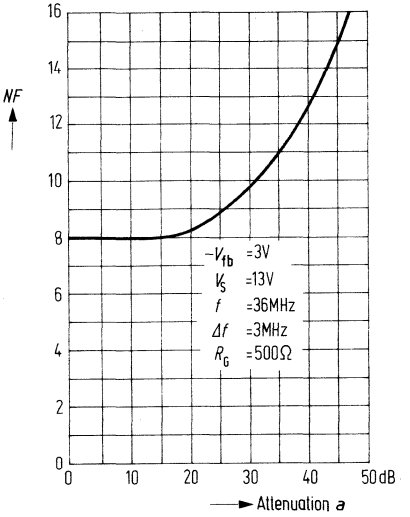
$V_S = 13$ V; $R_{10-11} = \infty$



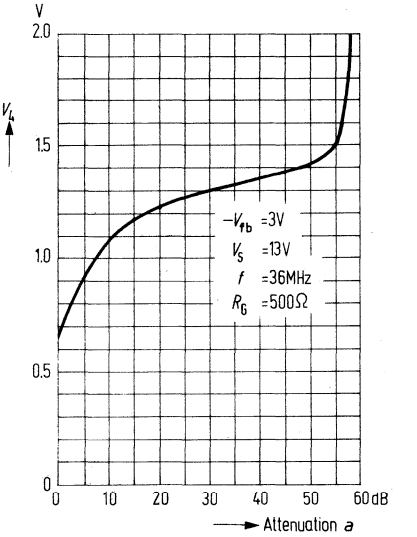
Block diagram



Noise figure versus attenuation
(measured at video frequency)
$V_S = 13$ V, $f = 36$ MHz, $\Delta f = 3$ MHz,
$R_G = 500\ \Omega$, $-V_{fb} = 3$ V

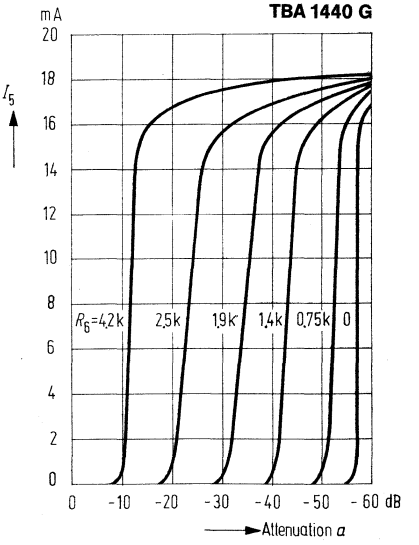


Control voltage versus attenuation
$-V_{fb} = 3$ V, $V_S = 13$ V, $f = 36$ MHz,
$R_G = 500\ \Omega$



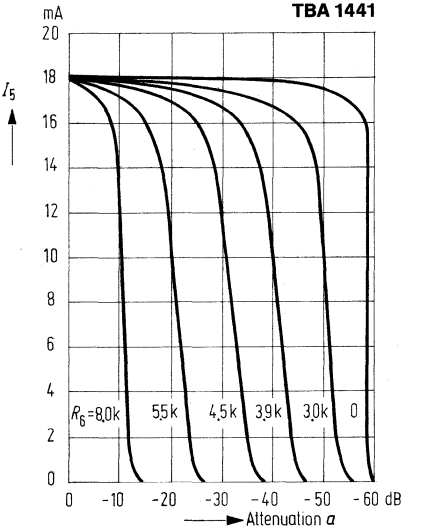
Tuner control current versus attenuation
R_6 = parameter

TBA 1440 G



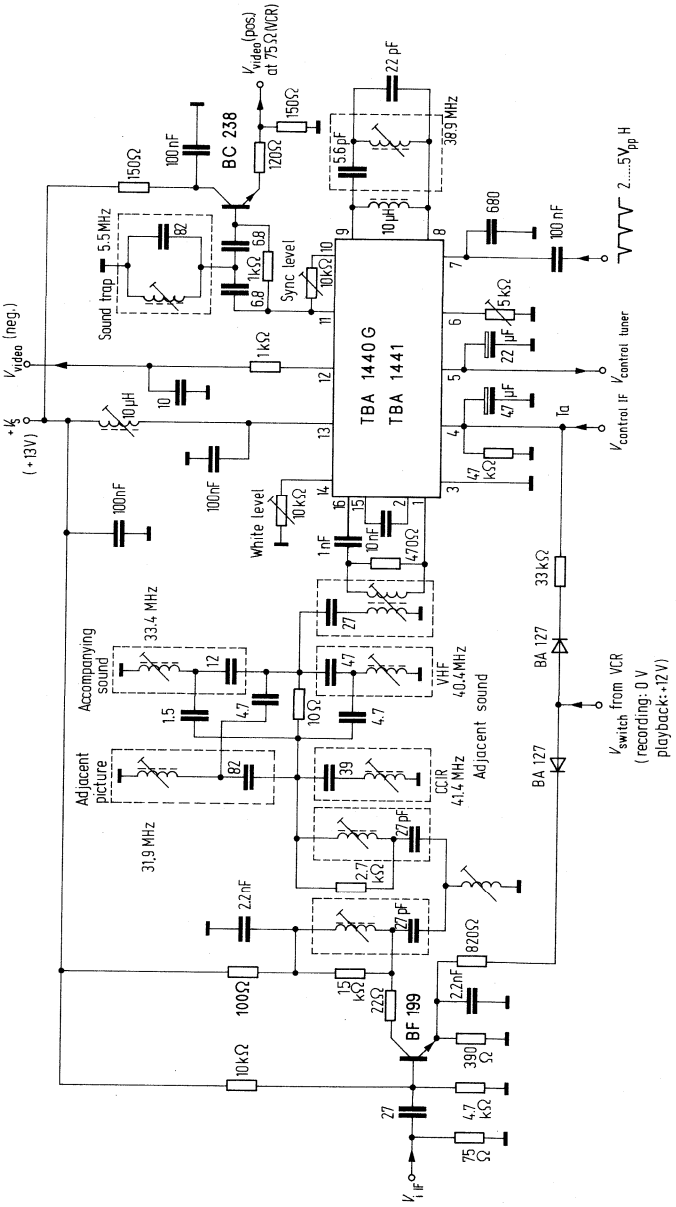
Tuner control current versus attenuation
R_6 = parameter

TBA 1441



Application circuit

suitable for connection of video recorders (75 Ω)



Bipolar circuit

Type	Ordering code	Package outline
TCA 440	Q67000-A669	DIP 16
TCA 440 I	Q67000-A669-S2	
TCA 440 II	Q67000-A669-S3	

AM receiver circuit for LW, MW, and SW in battery and line operated radio receivers. It includes an RF prestage with AGC, a balanced mixer, separate oscillator, and an IF amplifier with AGC. Because of its internal stabilization, all characteristics are largely independent of the supply voltage. For use in high quality radio sets the TDA 1046 should be preferred to the TCA 440.

Features

- Separately controlled prestage
- Multiplicative push-pull mixer with separate oscillator
- High large signal capability from 4.5 V supply voltage on
- 100 dB feedback control range in 5 stages
- Direct connection for tuning meter
- Few external components

Maximum ratings

Supply voltage	V_S	15	V
Storage temperature range	T_{stg}	−40 to 125	°C
Junction temperature	T_j	150	°C
Thermal resistance (system-air)	$R_{th\,SA}$	120	K/W

Operating range

Supply voltage range	V_S	4.5 to 15	V
Ambient temperature range	T_{amb}	−15 to 80	°C

Characteristics ($V_S = 9$ V; $T_{amb} = 25$ °C; $f_{iRF} = 600$ kHz; $f_{mod} = 1$ kHz)

Total current consumption		I_S	10.5	mA
RF level deviation for	$\Delta V_{AF} = 6$ dB	ΔG_{RF}	65	dB
($m = 80\%$)	$\Delta V_{AF} = 10$ dB	ΔG_{RF}	80	dB
AF output voltage for V_{iRF} (symm. measured at 1–2)				
for $m = 80\%$	$V_{iRF} = 20$ µV	V_{AFrms}	140	mV
	$V_{iRF} = 1$ mV	V_{AFrms}	260	mV
	$V_{iRF} = 500$ mV	V_{AFrms}	350	mV
for $m = 30\%$	$V_{iRF} = 20$ µV	V_{AFrms}	50	mV
	$V_{iRF} = 1$ mV	V_{AFrms}	100	mV
	$V_{iRF} = 500$ mV	V_{AFrms}	130	mV
Input sensitivity (measured at 60 Ω, $f_{iRF} = 1$ MHz, $m = 30\%/0\%$, $R_G = 540$ Ω)				
at signal-to-noise ratio (in acc. with DIN 45405)	$\frac{S+N}{N} = 6$ dB	V_{iRF}	1	µV
	$\frac{S+N}{N} = 26$ dB	V_{iRF}	7	µV
	$\frac{S+N}{N} = 58$ dB	V_{iHF}	1	mV

RF stage

Input frequency range	f_{iRF}	0 to 50	MHz
Output frequency $f_{IF} = f_{OSC} - f_{iRF}$	f_{IF}	460	kHz
Control range	ΔG_V	38	dB
Input voltage (for 600 kHz, $m = 80\%$) for overdrive ($THD_{AF} = 10\%$), symmetrically measured at pins 1 and 2	V_{iRFpp}	2.6	V
(mean carrier .value)	V_{iRFrms}	0.5	V
IF suppression between 1–2 and 15	a_{IF}	20	dB
RF input impedance			
a) unsymmetrical coupling			
at G_{RFmax}	Z_i	2/5	kΩ/pF
at G_{RFmin}	Z_i	2.2/1.5	kΩ/pF
b) symmetrical coupling			
at G_{RFmax}	Z_i	4.5	kΩ/pF
at G_{RFmin}	Z_i	4.5/1.5	kΩ/pF
Mixer output impedance (pins 15 or 16)	Z_q	250/4.5	kΩ/pF

IF stage		typ	
Input frequency range	f_{iIF}	0 to 2	MHz
Control range at 460 kHz	ΔG_V	62	dB
Input voltage (mean carrier value) at G_{min} for overdrive ($THD_{AF} = 10\%$), measured at pin 12 (60 Ω to ground, $f_{iIF} = 460$ kHz, $m = 80\%$; $f_{mod} = 1$ kHz)	$V_{IF\,rms}$	200	mV
AF output voltage for V_{iIF} at 60 Ω (pin 12)			
$V_{IF} = 30$ µV, $m = 80\%$; $f_{mod} = 1$ kHz	$V_{AF\,rms}$	50	mV
$V_{IF} = 3$ mV, $m = 80\%$; $f_{mod} = 1$ kHz	$V_{AF\,rms}$	200	mV
$V_{IF} = 3$ mV, $m = 30\%$; $f_{mod} = 1$ kHz	$V_{AF\,rms}$	70	mV
IF input impedance (unsymm. coupling)	Z_i	3/3	kΩ/pF
IF output impedance	Z_{q7}	200/8	kΩ/pF

Tuning meter

Recommended instruments: 500 µA ($R_i = 800$ kΩ)
or 300 µA ($R_i = 1.5$ kΩ)

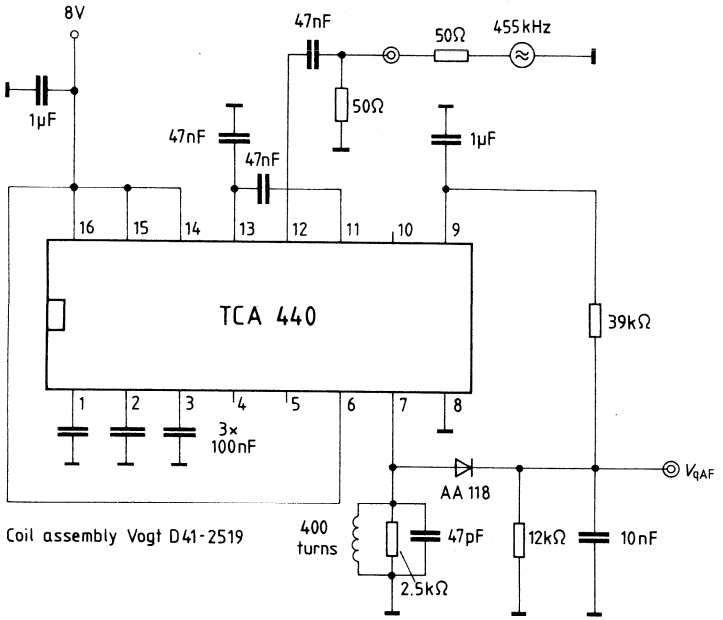
The IC offers a tuning meter voltage of 600 mV_{EMF} max. with a source impedance of approx. 400 Ω.

Selection

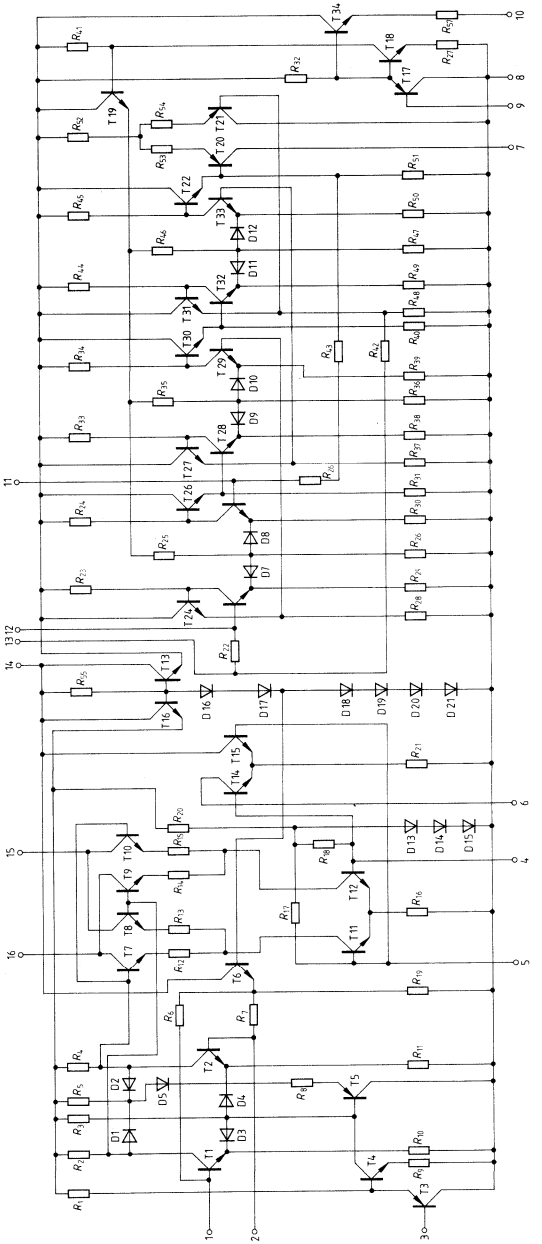
TCA 440 is selected in 2 groups as concerns the output voltage V_7:

Parameter: $V_{S\,rms} = 8$ V; V_{iIF} approx. 200 µV; $m = 30\%$; $f_{IF} = 455$ kHz; $f_{q\,AF} = 1$ kHz
TCA 440 I: $V_{7\,rms} = 40$ to 80 mV; 35 to 55 mV
TCA 440: $V_{7\,rms} = 40$ to 100 mV; 45 to 85 mV
The group number is imprinted on the IC.

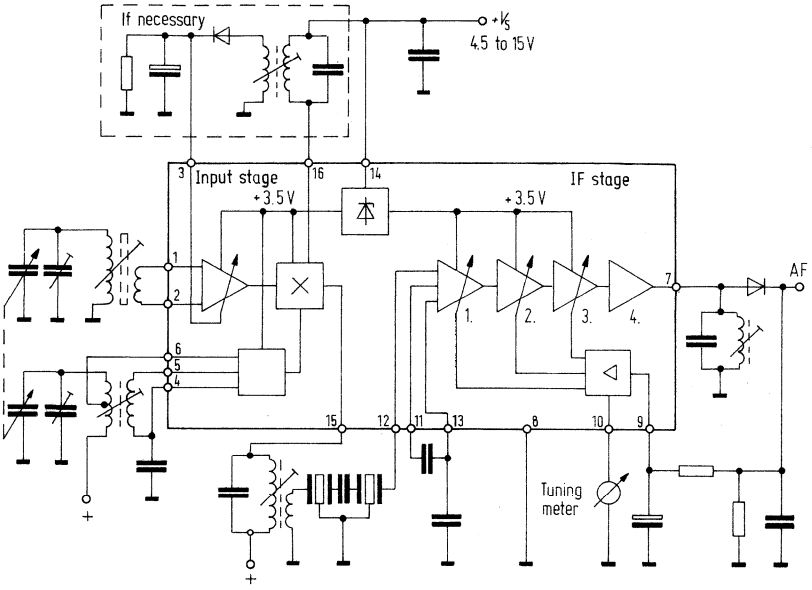
Measurement circuit to select the output voltage



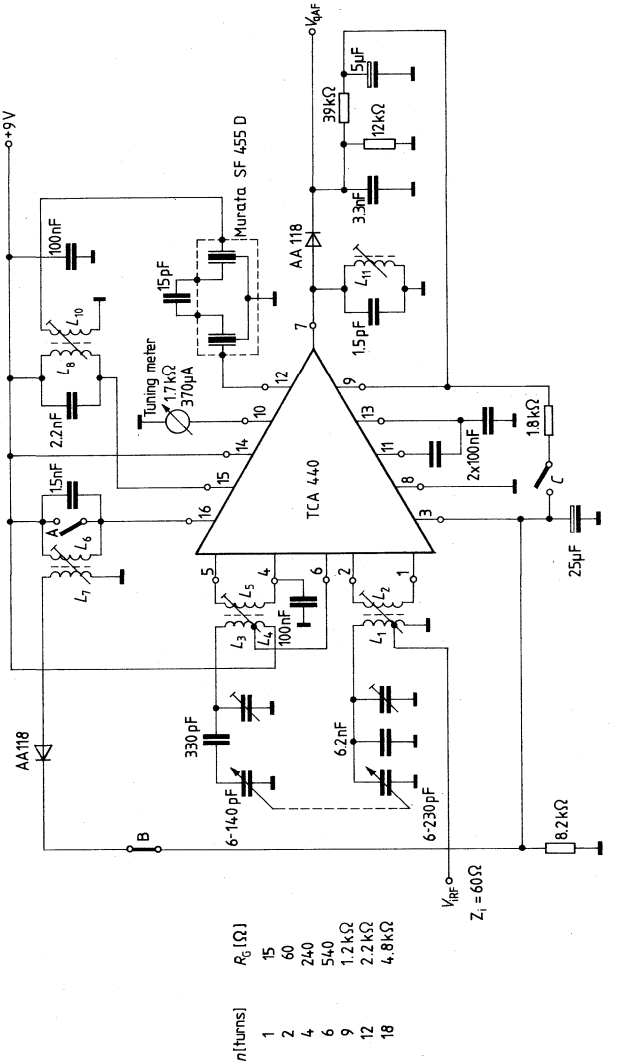
Circuit diagram



Block diagram



Measurement circuit for signal-to-noise ratio

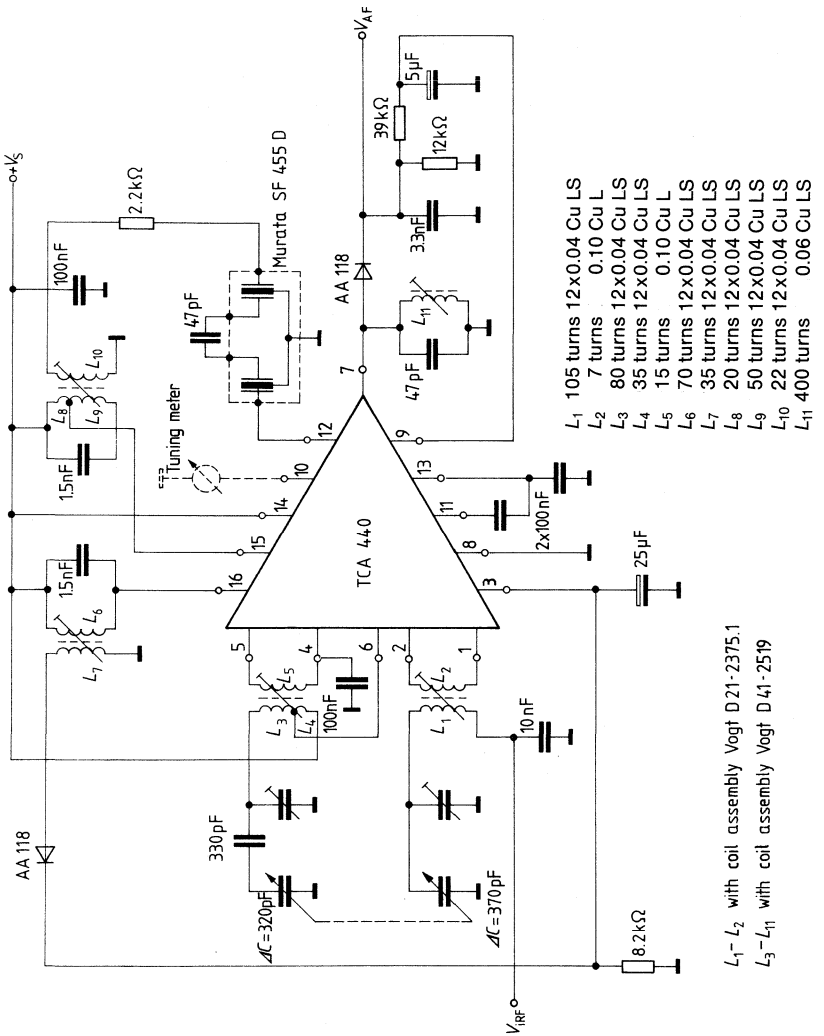


Switch

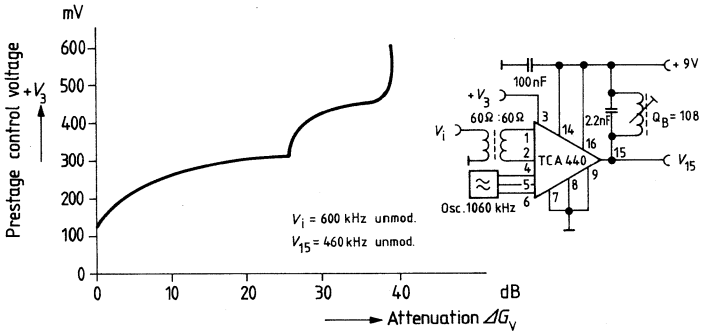
A	B	C	
off	on	off	① separate prestage control
on	off	on	② prestage control voltage derived from IF control voltage

f_i = 1 MHz; m = 30%

Application example for MW with TCA 440

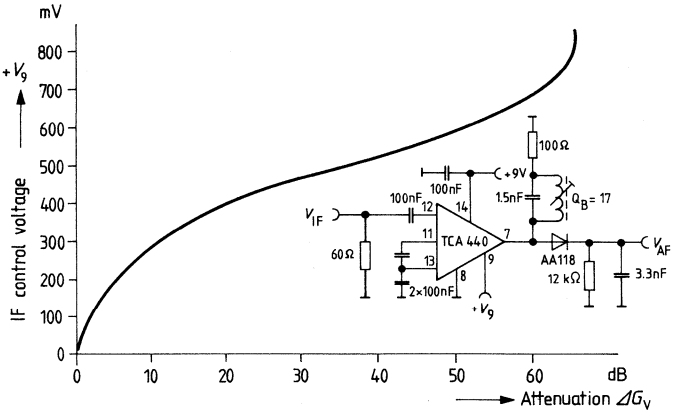


Prestage control TCA 440



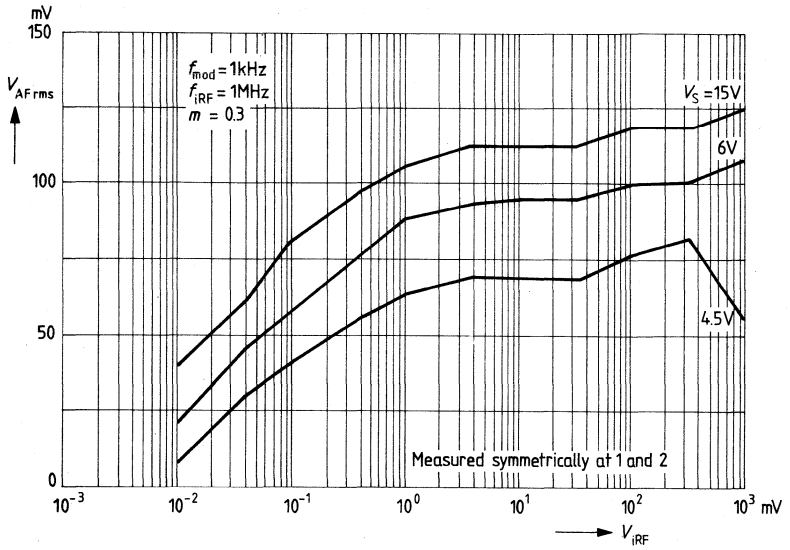
The input ist not power matched and can be driven with a higher resistance. The selected V_i ensures a constant V_{15} (50 mV peak-to-peak).

IF control



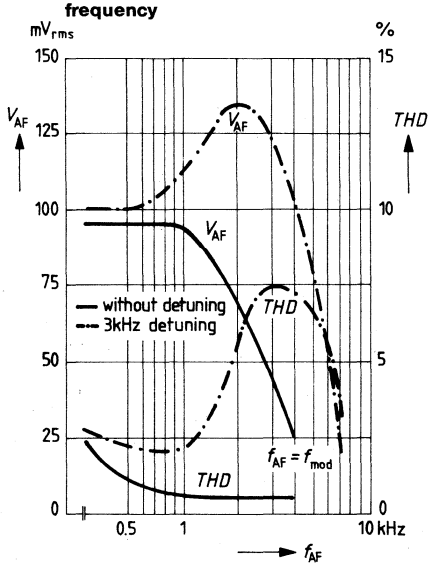
The selected V_{IF} (469 kHz; m = 80%; f_{mod} = 1 kHz) ensures a constant V_{AF} (200 mV, rms).

AF output voltage versus RF input voltage

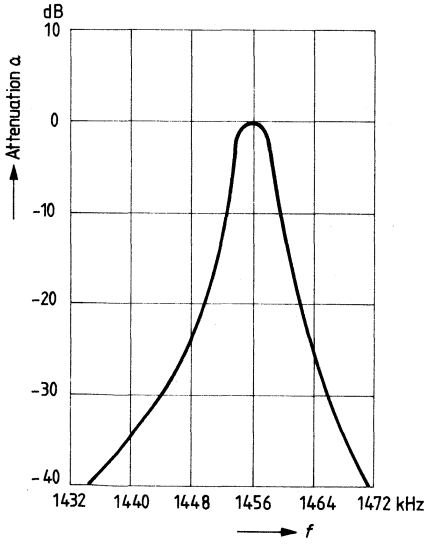


Example for medium wave applications

AF output voltage versus output frequency
Total harmonic distortion versus modulation frequency

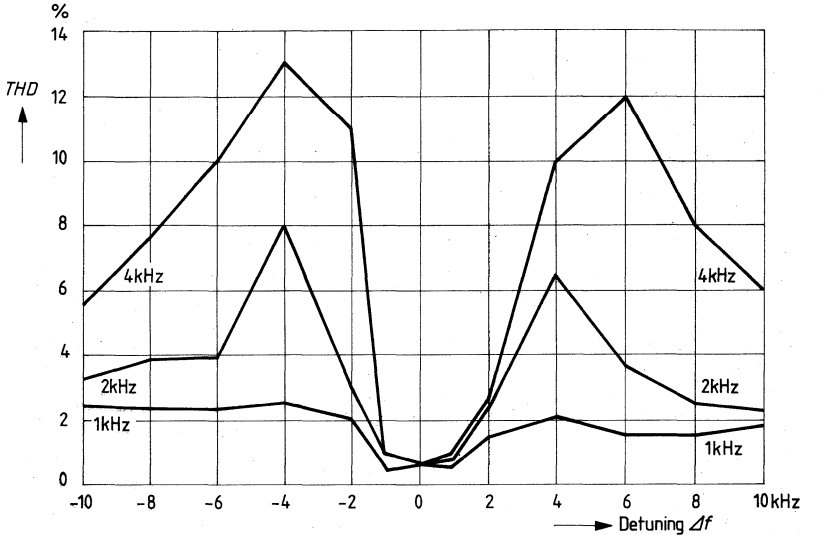


Passband characteristic versus input frequency, measured from input to output of the circuit

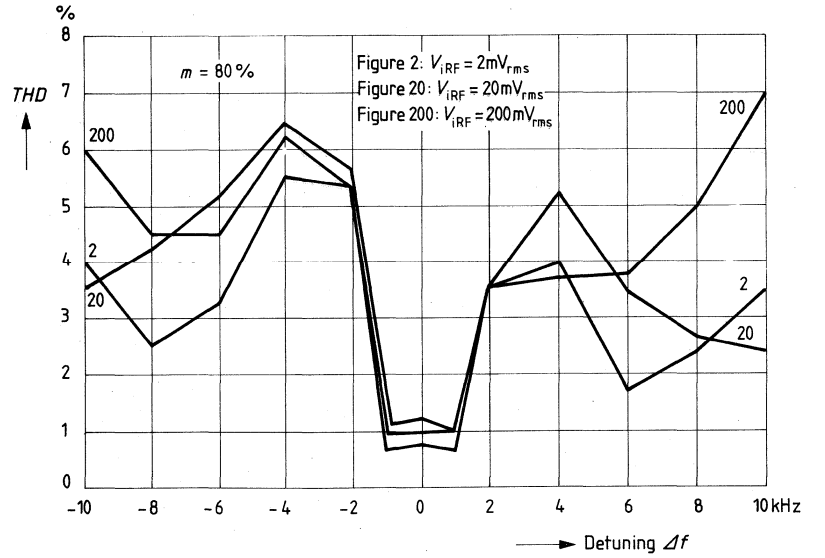


Total harmonic distortion versus detuning (parameter: modulation frequency)

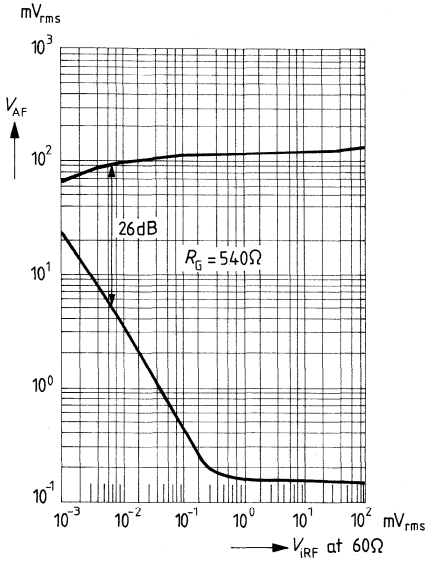
$V_S = 9$ V $f_{OSC} = 1.455$ MHz $\pm \Delta f$ $m = 30\%$
$f_{iRF} = 1$ MHz $f_{IF} = 455$ kHz $V_{iRF} = 20$ mV$_{rms}$



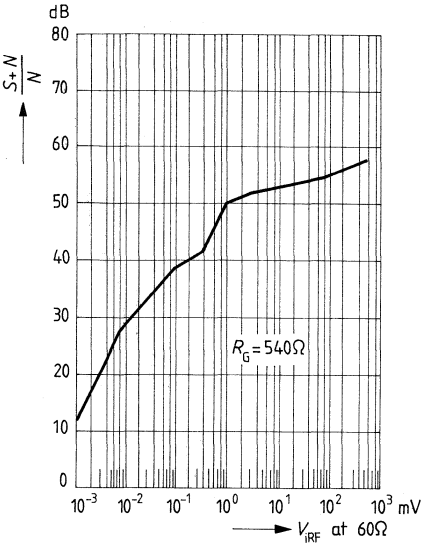
Total harmonic distortion versus detuning (parameter: RF input voltage)



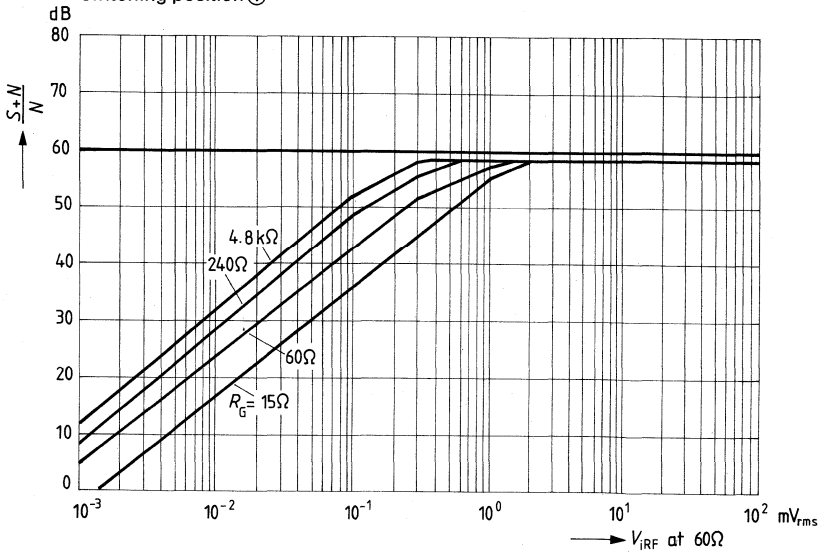
AF output voltage and noise figure versus RF input voltage
switching position ①



Signal-to-noise ratio versus RF input voltage
switching position ②

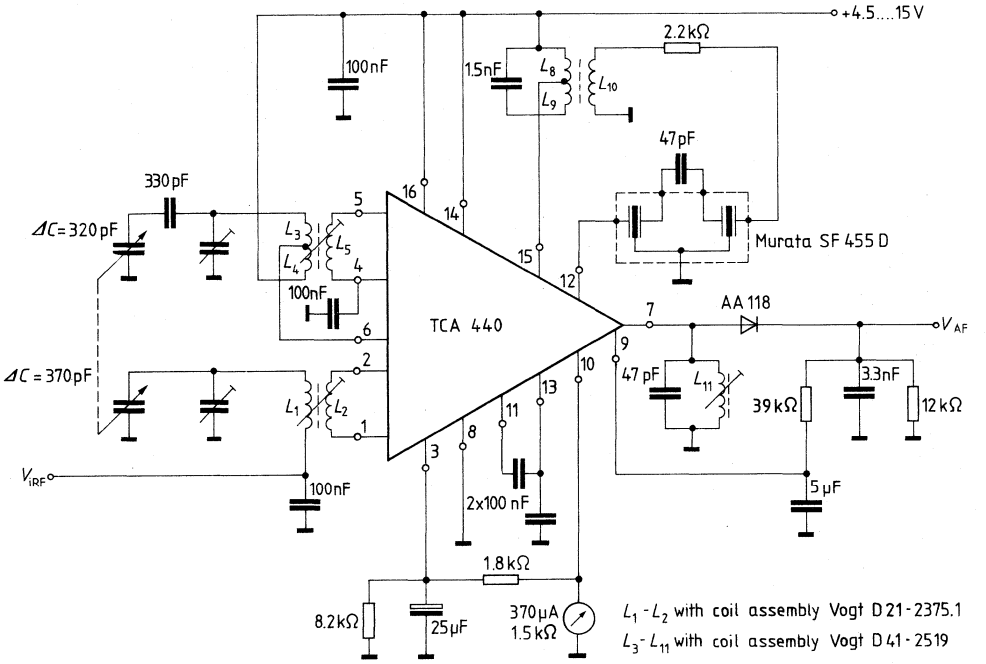


Signal-to-noise ratio versus RF input voltage
(parameter is generator impedance)
switching position ①



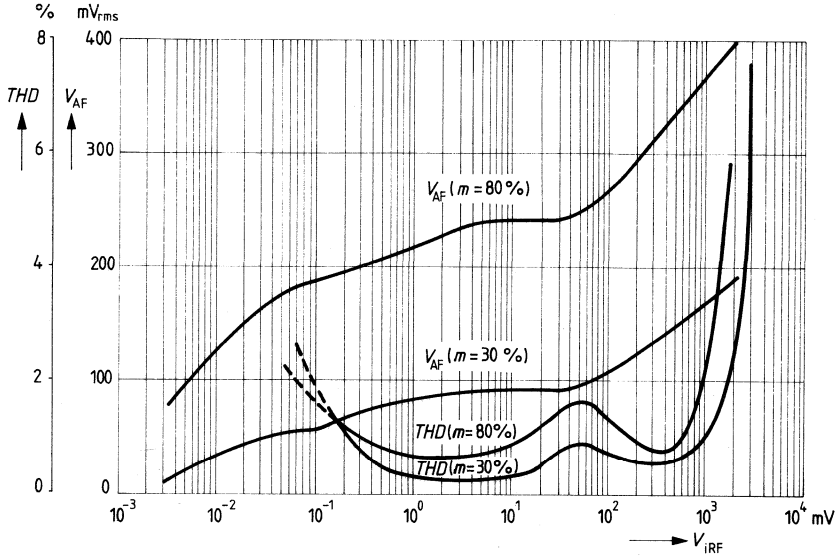
Application example for MW

Prestage control is derived from IF control

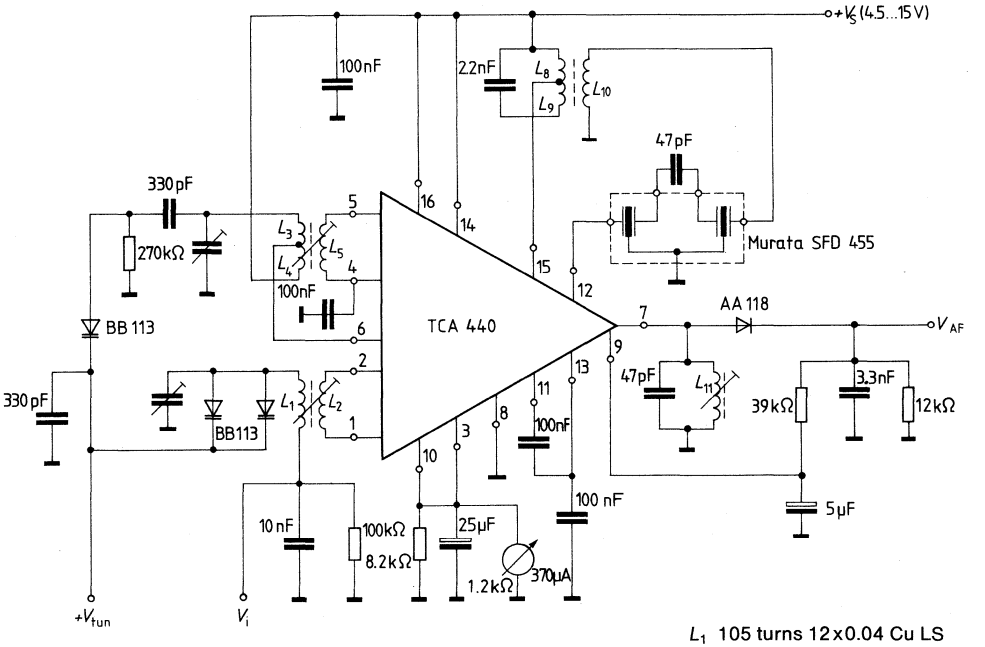


L_1 105 turns 12x0.04 Cu LS
L_2 7 turns 0.10 Cu L
L_3 80 turns 12x0.04 Cu LS
L_4 35 turns 12x0.04 Cu LS
L_5 15 turns 0.10 Cu L
L_8 20 turns 12x0.04 Cu LS
L_9 50 turns 12x0.04 Cu LS
L_{10} 22 turns 12x0.04 Cu LS
L_{11} 400 turns 0.04 Cu L

Test figures for application example for MW
Total harmonic distortion and AF output voltage
versus RF input voltage
measured symmetrically at pins 1 and 2
$f_i = 1$ MHz, $f_{mod} = 1$ kHz, $f_{IF} = 455$ kHz, $V_S = 9$ V



Application example for MW using BB 113 varicap diodes

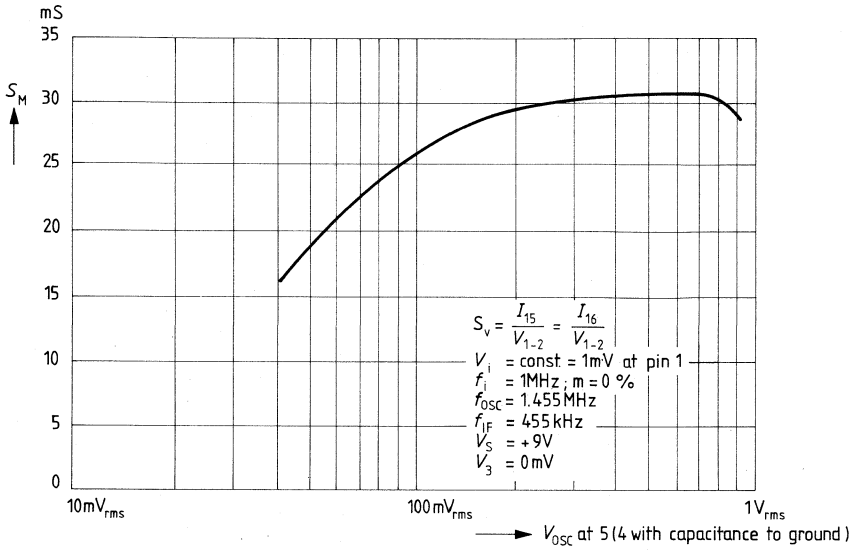


L_1-L_2 with coil assembly Vogt D21-2375.1
L_3-L_{11} with coil assembly Vogt D41-2519

V_{tun} = 8.5 V ⟶ f_i = 800 kHz
V_{tun} = 30 V ⟶ f_i = 1620 kHz

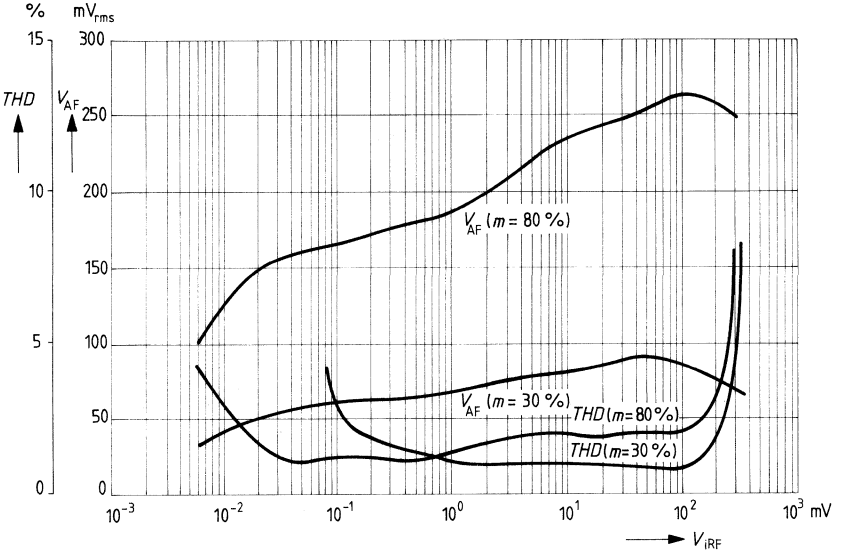
L_1	105 turns	12x0.04 Cu LS
L_2	7 turns	0.10 Cu LS
L_3	80 turns	12x0.04 Cu LS
L_4	35 turns	12x0.04 Cu LS
L_5	15 turns	0.10 Cu LS
L_8	20 turns	12x0.04 Cu LS
L_9	50 turns	12x0.04 Cu LS
L_{10}	22 turns	12x0.04 Cu LS
L_{11}	400 turns	0.06 Cu L

Conversion transconductance versus oscillator voltage

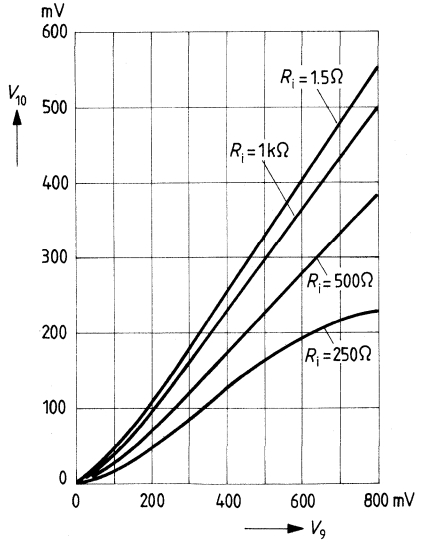


Measured values for application example for MW using diode BB 113

AF output voltage and total harmonic distortion versus RF input voltage
$f_i = 1$ MHz; $f_{mod} = 1$ kHz; $f_{IF} = 455$ kHz
$V_S = 9$ V; V_{iRF} symmetrically measured at pins 1 and 2



Tuning meter voltage versus IF control voltage
(parameter: impedance of tuning meter)



Example for moving coil instruments

R_i	Full-service deflection
1.5 kΩ	100 µA
1.5 kΩ	170 µA
2 kΩ	200 µA
350 Ω	500 µA

Bipolar circuit

Type	Ordering code	Package outline
TCA 4500 A	Q67000-A1471	DIP 16

The TCA 4500 A is a phase-locked loop stereo decoder which incorporates a variable channel separation control. In this IC, the sensitivity to the third harmonics of both the pilot and subcarrier frequencies has been eliminated due to the use of appropriate, digitally generated waveforms in the phase-locked loop and decoder sections.

Features

- Low distortion
- Excellent rejection of ARI subcarrier and pilot tone harmonics
- No need for coils

Maximum ratings

Supply voltage	V_S	16	V
Lamp drive voltage (lamp OFF)	V_7	30	V
Lamp current	I_7	100	mA
Channel separation control voltage	V_{11}	10	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	90	K/W

Operating range

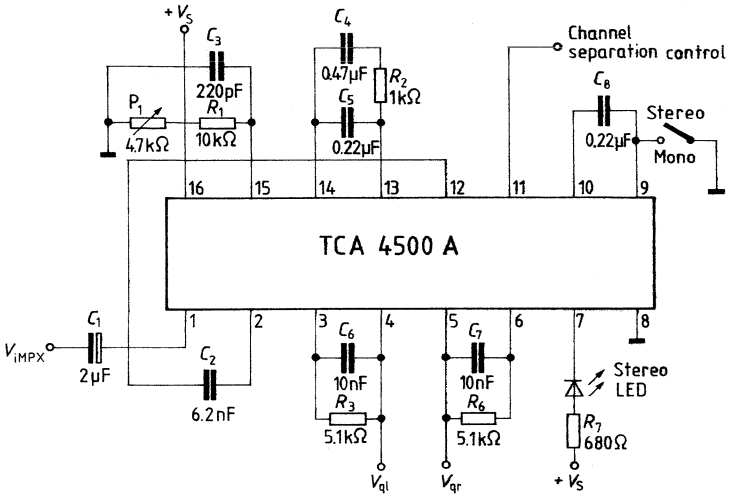
Supply voltage range	V_S	8 to 16	V
Ambient temperature range	T_{amb}	−25 to 85	°C

Characteristics

($V_S = 12$ V; $T_{amb} = 25$ °C; $V_{i(MPX)} = 2.5$ V_{pp}; $f_{mod} = 1$ kHz; $V_{pilot} = 10\%$ V_i)

		min	typ	max	
Current consumption ($I_7 = 0$)	I_{16}		35		mA
Stereo channel separation					
unadjusted	a	30			dB
optimized on other channel	a_{opt}	40			dB
Monaural voltage gain	G	0.8	1	1.2	
THD at 2.5 V_{pp}	THD			0.3	%
THD at 1.5 V_{pp}	THD		0.2		%
Signal-to-noise ratio in acc. with DIN 45405	$a_{S/N}$		85		dB
rms value 20 Hz – 15 kHz	$a_{S/N}$		90		dB
Frequency rejection 19 kHz	a		31		dB
38 kHz	a		50		dB
Pilot tone harmonic rejection 57 kHz ARI	a		60		dB
Subcarrier harmonic rejection 76 kHz	a		45		dB
114 kHz	a		50		dB
152 kHz	a		50		dB
Input voltage for stereo switching threshold (19 kHz input signal for lamp "ON"	$V_{i1\,rms}$	12	16	20	mV
Hysteresis for stereo switching threshold	H		6		dB
Quiescent output voltage change with mono/stereo switching	ΔV_{ql}, ΔV_{qr}		5	20	mV
Channel separation control voltage					
3 dB separation	V_{11}		0.7		V
30 dB separation	V_{11}		1.7		V
Minimum channel separation ($V_{11} = 0$ V)	a			1	dB
Monaural channel inbalance (pilot tone off)	$\Delta V_{ql,r}$			0.3	dB
Hum suppression	a_{hum}		55		dB
Input resistance	R_{i1}		50		kΩ
Output resistance	R_{q4}, R_{q5}		100		Ω
Channel separation control current	I_{11}			−300	μA
Capture range	$\Delta f/f_0$		±5		%

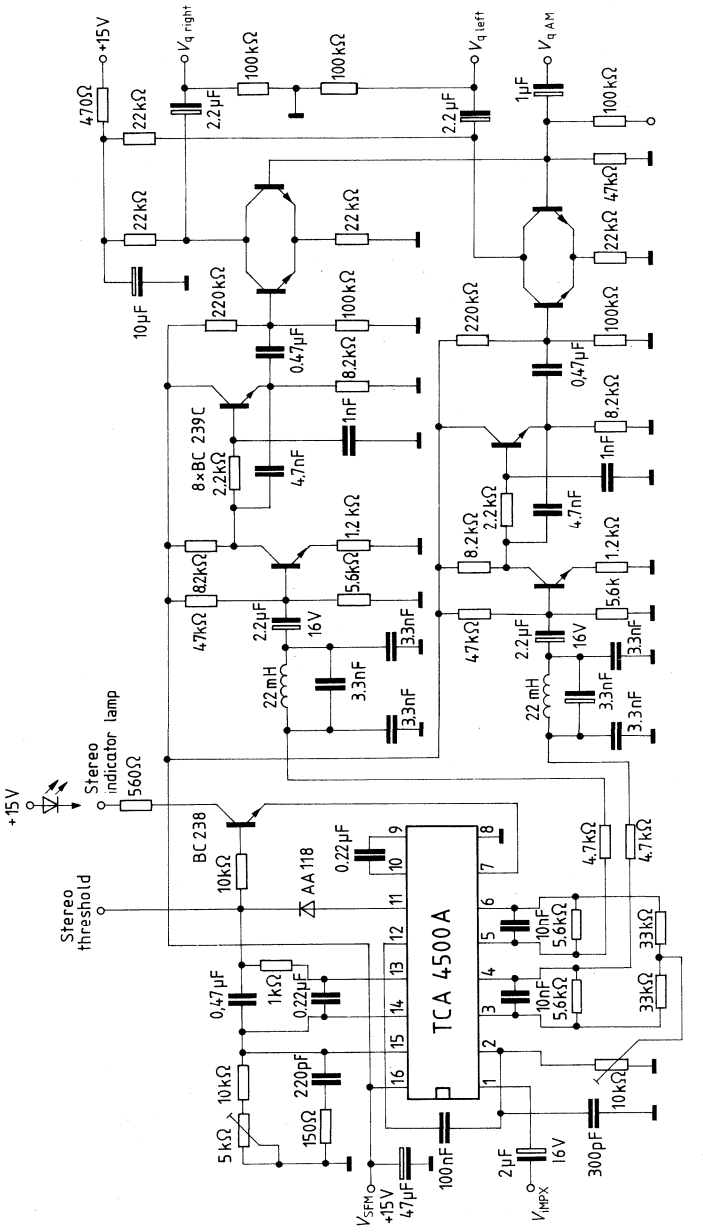
Measurement circuit



Pin configuration

Pin No.	Function
1	Input
2	Preamplifier output
3	Left amplifier input
4	Left channel output
5	Right channel output
6	Right amplifier input
7	Stereo indicator lamp
8	Ground
9	Switching threshold
10	Switching threshold
11	19 kHz output/channel separation control
12	Modulator input
13	Loop filter
14	Loop filter
15	Oscillator *RC* network
16	Supply voltage $+V_S$

Application circuit with low-pass filter



Bipolar circuit

Type	Ordering code	Package outline
TCA 4510	Q67000-A1533	DIP 18

The TCA 4510 decodes the transmitter side stereo information in both L and R channels. Stereo transmission is shown by means of an indicator lamp. A continual blending of mono and stereo signals is possible. The switching frequencies are controlled by a phase-locked loop. The stereo decoder can be used in time multiplex (switching) or in frequency multiplex (matrix) mode of operation. The TCA 4510 is particularly suitable for battery operation.

Features

- Good channel separation
- No need for coils
- Automatically adjustable bandwidth
- Good suppression of ARI subcarrier and pilot tone harmonics

Maximum ratings

Supply voltage	V_S	18	V
Lamp voltage	V_{LP}	18	V
Current for stereo indicator lamp $V_{18} \cdot I_{LP} \leqq 300$ mV	I_{LP}	50	mA
Minimum values at all pins	V	0	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	78	K/W
(junction-case)	$R_{th\,JC}$	45	K/W

Operating range

Supply voltage range	V_S	4.5 to 18	V
Ambient temperature range	T_{amb}	−25 to 85	°C

Characteristics for switch operation ($V_S = 8$ V; $T_{amb} = 25$ °C)

		min	typ	max	
Total current consumption (FM operation) S1 closed	I_S		10	15	mA
Total current consumption (AM operation) S1 open	I_S		6	8	mA
Lamp current adjustment range ($V_{18} \cdot I_{LP} \leqq 300$ mW)	I_{LP}	10		25	mA
Lamp current short circuit ($V_{18} \cdot I_{LP} \leqq 300$ mW)	I_{LP}			50	mA
Input amplifier					
Op amp input signal	V_{16pp}			0.9	V
Op amp output signal[1]	V_{14pp}		V_{16}		V
Input resistance	R_i	90	125		kΩ
Feedback resistance	R_F		10		kΩ
Reference voltage	V_{13}		1.45		V
Stereo matrix					
Output voltage (stereo) for modulated output[1,6]	V_{qAFpp}	0.7	0.8	1.2	V
Output voltage (mono) L or R modulated[2,6]	V_{qAFpp}	0.35	0.4	0.6	V
Output resistance	R_q		1.5	2	kΩ
Crosstalk attenuation[1] ($f_{AF} = 1$ kHz)	a_{CR}	32	40		dB
Reduction 19 kHz Test circuit 1	a_{19}	30	32		dB
Reduction 38 kHz Test circuit 1	a_{38}	30	40		dB
Reduction 57 kHz Test circuit 1	a_{57}	30	45		dB
Reduction 76 kHz Test circuit 1	a_{76}	30	40		dB
Hum suppression[3]	a_{hum}	34	39		dB
Noise voltage[4]	V_{qn}		30	80	μV
Total harmonic distortion[1,6] ($f_{AF} = 1$ kHz)	THD			0.5	%
Channel balance[2]	B			0.5	dB
Switching noise mono/stereo S1 closed/open	ΔV_9, ΔV_{10}			60	mV

For notes refer to page 353

Characteristics for switch operation ($V_S = 8$ V; $T_{amb} = 25$ °C) (cond't)

		min	typ	max	
Oscillator					
Output resistance for f_{OSC} measurement	R_{q8}		200		kΩ
Oscillator basic frequency	f_{OSC}		19		kHz
Capture and hold range[1])	$f_{C/H}$	±0.4	±1	±2.0	kHz
Balancing resistance ($f_{OSC} = 19$ kHz)	R_{OSC}	13		18	kΩ
Function of the oscillator S1 closed	V_{18}	0.9			V
Oscillator switch off[8]) S1 open	V_{18}			0.4	V
Phase comparisons					
Input voltage[1])	V_{5pp}	0.3	0.45	0.6	V
Input resistance	R_5		3.3		kΩ
Input voltage	V_{5pp}			0.9	V
Stereo switch					
Threshold stereo ON[5]) ($f = 19$ kHz)	V_{iPTpp}		30	55	mV
Threshold stereo OFF[5]) ($f = 19$ kHz)	V_{iPTpp}	12	15		mV
Hysteresis[5]) ($f = 19$ kHz)	H_y	3	6	9	dB
Mono/stereo blending					
Mono ($V_H = V_8 = 0.5$ V)[7])	a_{bl}	3	6	9	dB
Stereo ($V_H = V_8 = 0.9$ V[7])	a_{bl}	32			dB
Mono switchover	V_S		4.8	5	V

[1]) $V_{ipp} = 0.75$ V MPX; $V_H \geqq 1$ V; S1 closed; $f_{AF} = 1$ kHz
[2]) $V_{ipp} = 0.75$ V MPX; S1 open; $f_{AF} = 1$ kHz
[3]) $V_S = 8$ V + V_n; $V_{n\,rms} = 200$ mV; 200 Hz
[4]) CCIR DIN 45405; unweighted; S1 open
[5]) S1 closed
[6]) After TP with $f_{co} = 6.5$ kHz; reduction 36 dB/octave
[7]) $V_{16pp} = 0.75$ V MPX; S1 closed; $f_{AF} = 1$ kHz
[8]) Oscillator is disabled, with ≦ 0.4 V present at pin 18 or open S1

Circuit description (switching operation)

The MPX input signal is corrected in amplitude and phase by an operational amplifier. For this purpose an *RC* circuit is connected at pin 15.

Subsequently, the (L+R) and (L−R) signals are processed in separate stages. The (L−R) signal is demodulated and can be reduced by the factor *a* through mono/stereo blending. In the final matrix circuit the aggregate signal (L+R) is added to the demodulated signal *a* (L−R) according to the following formulae:

$$(L+R) + a\,(L-R) = L(1+a) + R(1-a)$$
$$(L+R) - a\,(L-R) = L(1-a) + R(1+a)$$

$$\underset{\text{Mono}}{0} \leq \underset{\text{Blending}}{a} \leq \underset{\text{Stereo}}{1}$$

The generated output signals are then forwarded to two external *RC* low-passes for deemphasis.

The required frequency to demodulate the L−R signal is obtained by a phase-locked loop (PLL) from the divider. By means of a pilot tone applied to pin 5, the oscillator is synchronized by phase comparison 1. An additional phase comparison 2 provides mono or stereo information. Based on this information, the indicator lamp is activated and lights up when a suffuciently strong signal is present at the input. Moreover, the (L−R) reduction is eliminated.

If switch S1 is open, the IC switches the oscillator off, whereby the stereo switch and the mono/stereo blending suppress the L−R signal. The supply current is thus reduced. Also, since the oscillator does not resonate when switch S1 is open, AM receiver signals can be forwarded without interference via the IC.

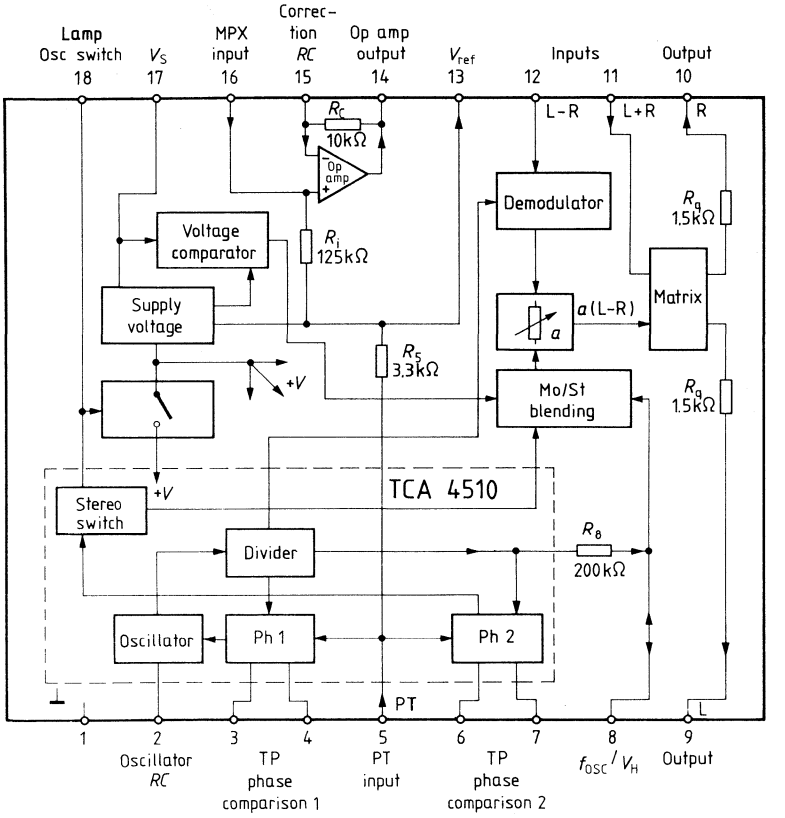
If pin 8 is not connected, the oscillator frequency can be measured. For normal operating functions, the blending voltage V_H is applied to pin 8 or pin 8 must be blocked by a capacitor. Otherwise, cross-talk is affected by the oscillator frequency.

During low operating voltages ($V_S < 5$ V) the mono/stereo blending switches over to mono ($a = 0$).

Pin configuration

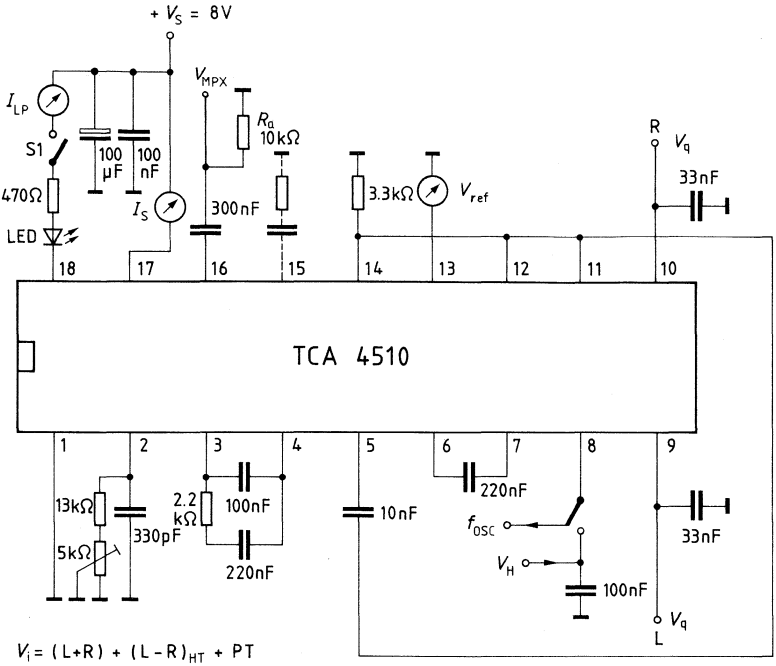
Pin No.	Function
1	Ground
2	Oscillator *RC*
3	TP phase comparison 1
4	TP phase comparison 1
5	Pilot tone (PT) input
6	TP phase comparison 2
7	TP phase comparison 2
8	f_{OSC} output/St-Mo blending V_H
9	Output L
10	Output R
11	(L+R) input
12	(L−R) input
13	Reference voltage
14	Output op amp
15	− input op amp
16	+ input op amp
17	Supply voltage
18	Lamp connection/oscillator switch

Block diagram



Test and measurement circuit

Switching operation

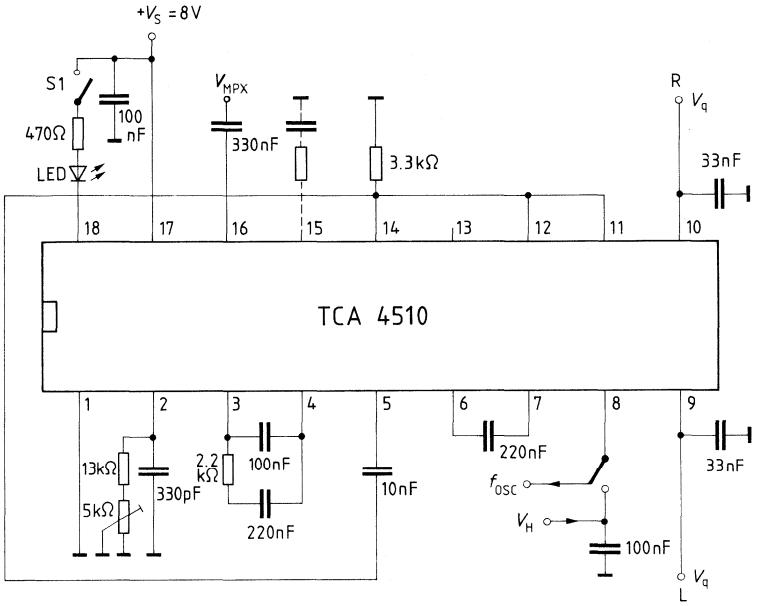


$V_i = (L+R) + (L-R)_{HT} + PT$
L = 100 % ; R = 0 % or
R = 100 % ; L = 0 %

S1 open = AM
S1 closed = FM

Application circuit

Switching operation



S1 open = AM
S1 closed = FM

Bipolar circuit

Type	Ordering code	Package outline
TCA 4511	Q67000-A1648	DIP 18

The TCA 4511 decodes the transmitter side stereo information in both L and R channels. Stereo transmission is shown by means of an indicator lamp. A continual blending of mono and stereo signals is possible. The switching frequencies are controlled by a phase-locked loop. The stereo decoder can be used in time multiplex (switching) or in frequency multiplex (matrix) mode of operation.

Features

- Good channel separation
- No need for coils
- Automatically adjustable bandwidth
- Good suppression of ARI subcarrier and pilot tone harmonics

Maximum ratings

Supply voltage	V_S	18	V
Lamp voltage	V_{LP}	18	V
Current for stereo indicator lamp ($V_{18} \cdot I_{LP} \leqq 300$ mW)	I_{LP}	50	mA
Minimum values at all pins	V	0	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	78	K/W
(junction-case)	$R_{th\,JC}$	45	K/W

Operating range

Supply voltage range	V_S	8 to 18	V
Ambient temperature range	T_{amb}	−25 to 85	°C

Characteristics for switch operation ($V_S = 12$ V; $T_{amb} = 25$ °C)

		min	typ	max	
Total current (FM operation) S1 closed	I_S		14	20	mA
Total current (AM operation) S1 open	I_S		10	15	mA
Lamp current adjustment range ($V_{18} \cdot I_{LP} \leqq 300$ mW)	I_{LP}	10		25	mA
Lamp current short circuit ($V_{18} \cdot I_{LP} \leqq 300$ mW)	I_{LP}			50	mA
Input amplifier					
Op amp input signal	$V_{16\,pp}$			1.6	V
Op amp output signal[1])	$V_{14\,pp}$		V_{16}		V
Input resistance	R_i	90	125		kΩ
Feedback resistance	R_F		10		kΩ
Reference voltage	V_{13}		1.75		V
Stereo matrix					
Output voltage (stereo)[1,6]) for modulated output	$V_{q\,AF\,pp}$	0.9	1.2	1.6	V
Output voltage (mono)[2,6]) L or R modulated	$V_{q\,AF\,pp}$	0.45	0.6	0.8	V
Output resistance	R_q		1.5	2	kΩ
Crosstalk attenuation[1]) ($f_{AF} = 1$ kHz)	a_{CR}	34	40		dB
Reduction 19 kHz Test circuit 1	a_{19}	30	32		dB
Reduction 38 kHz Test circuit 1	a_{38}	30	40		dB
Reduction 57 kHz Test circuit 1	a_{57}	30	45		dB
Reduction 76 kHz Test circuit 1	a_{76}	30	40		dB
Hum suppression[3])	a_{hum}	40	45		dB
Noise voltage[4])	V_{qn}		30	80	μV
Total harmonic distortion[1,6]) ($f_{AF} = 1$ kHz)	THD			0.5	%
Channel balance[2])	B			0.5	dB
Switching noise mono/stereo S1 closed/open	$\Delta V_9, \Delta V_{10}$			60	mV
Oscillator					
Output resistance for f_{OSC} measurement	R_8		200		kΩ
Oscillator basic frequency	f_{OSC}		19		kHz
Capture and hold range[1])	$f_{C/H}$	±0.4	±1	±2.0	kHz
Balancing resistance ($f_{OSC} = 19$ kHz)	R_{OSC}	13		18	kΩ
Function of the oscillator S1 closed	V_{18}	1.0			V
Switch off of the oscillator[8]) S1 open	V_{18}			0.4	V
Function of the oscillator ($I_{18} = 10$ mA)	V_{18}	0.9			V

1) For footnotes refer to page 361.

Characteristics for switch operation ($V_S = 12$ V; $T_{amb} = 25$ °C) (cont'd)

		min	typ	max	
Phase comparisons					
Input voltage[1])	$V_{5\,pp}$	0.5	0.7	0.9	V
Input resistance	R_5		3.3		kΩ
Input voltage	$V_{5\,pp}$			1.6	V
Stereo switch					
Threshold stereo ON[5]) ($f = 19$ kHz)	$V_{iPT\,pp}$		30	55	mV
Threshold stereo OFF[5]) ($f = 19$ kHz)	$V_{iPT\,pp}$	12	15		mV
Hysteresis	H_y	3	6	9	dB
Mono/stereo blending					
Mono ($V_H = V_8 = 0.5$ V)[7])	a_{bl}	3	6	9	dB
Stereo ($V_H = V_8 = 0.9$ V)[7])	a_{bl}	34			dB

[1]) $V_{i\,pp} = 1.2$ V MPX; $V_H \geqq 1$ V; S1 closed; $f_{AF} = 1$ kHz
[2]) $V_{i\,pp} = 1.2$ V MPX; S1 open; $f_{AF} = 1$ kHz
[3]) $V_S = 12$ V + V_n; $V_{n\,rms} = 200$ mV; 200 Hz
[4]) CCIR DIN 45405; unweighted; S1 open
[5]) S1 closed
[6]) After TP with $f_{co} = 6.5$ kHz; reduction 36 dB/octave
[7]) $V_{16\,pp} = 0.75$ V MPX; S1 closed; $f_{AF} = 1$ kHz
[8]) The oscillator is switched off, if pin 18 is connected with a voltage ≦ 0.4 V or S1 is open.

Circuit description (switching operation)

The MPX input signal is corrected in amplitude and phase by an operational amplifier. For this purpose an *RC* circuit is connected at pin 15.

Subsequently, the (L+R) and (L−R) signals are processed in separate stages. The (L−R) signal is demodulated and can be reduced by the factor *a* through mono/stereo blending. In the final matrix circuit the aggregate signal (L+R) is added to the demodulated signal *a* (L−R) according to the following formulae:

$$(L+R) + a\,(L-R) = L(1+a) + R(1-a)$$
$$(L+R) - a\,(L-R) = L(1-a) + R(1+a)$$

$$\underset{\text{Mono}}{0} \leq \underset{\text{Blending}}{a} \leq \underset{\text{Stereo}}{1}$$

The generated output signals are then forwarded to two external *RC* low-passes for deemphasis.

The required frequency to demodulate the L−R signal is obtained by a phase-locked loop (PLL) from the divider. By means of a pilot tone applied to pin 5, the oscillator is synchronized by phase comparison 1. An additional phase comparison 2 provides mono or stereo information. Based on this information, the indicator lamp is activated and lights up when a sufficiently strong signal is present at the input. Moreover, the (L−R) reduction is eliminated.

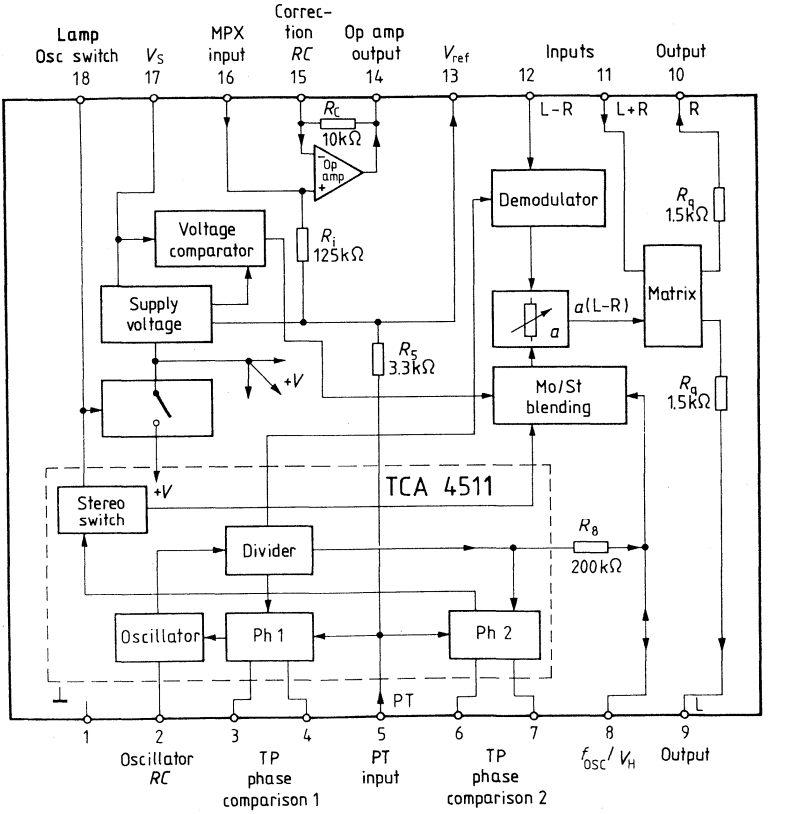
If switch S1 is open, the IC switches the oscillator off, whereby the stereo switch and the mono/stereo blending suppress the L−R signal. The supply current is thus reduced. Also, since the oscillator does not resonate when switch S1 is open, AM receiver signals can be forwarded without interference via the IC.

If pin 8 is not connected, the oscillator frequency can be measured. For normal operating functions, the blending voltage V_H is applied to pin 8 or pin 8 must be blocked by a capacitor. Otherwise, cross-talk is affected by the oscillator frequency.

Pin configuration

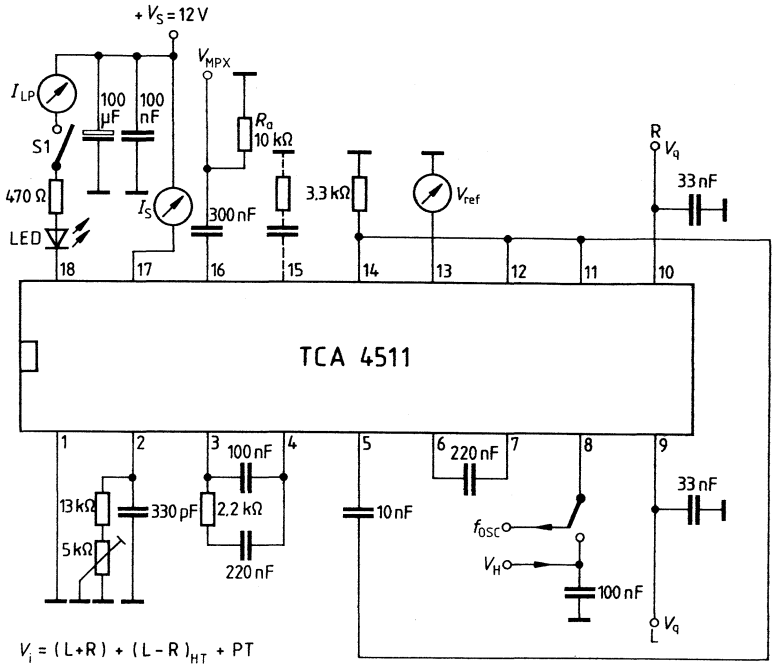
Pin No.	Function
1	Ground
2	Oscillator *RC*
3	TP phase comparison 1
4	TP phase comparison 1
5	Pilot tone (PT) input
6	TP phase comparison 2
7	TP phase comparison 2
8	f_{OSC} output/St-Mo blending V_H
9	Output L
10	Output R
11	(L+R) input
12	(L−R) input
13	Reference voltage
14	Output op amp
15	− input op amp
16	+ input op amp
17	Supply voltage
18	Lamp connection/oscillator switch

Block diagram



Test circuit

Switching operation

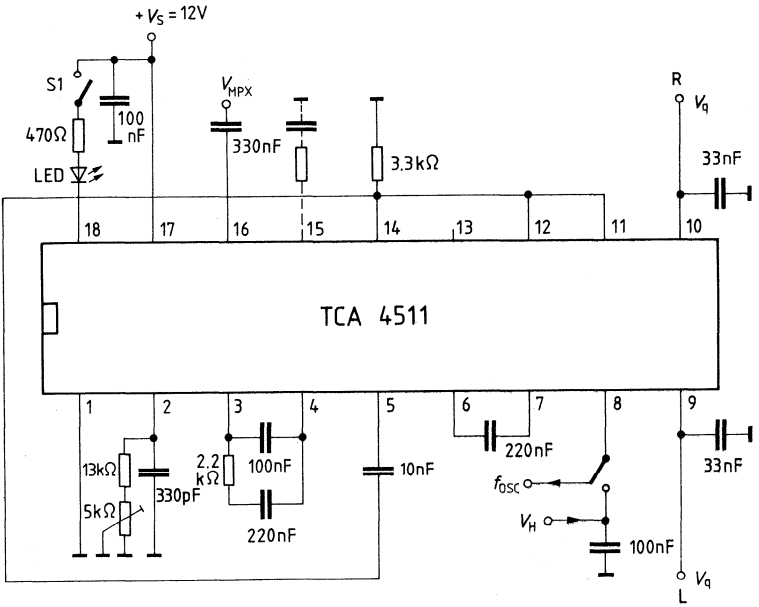


$V_i = (L+R) + (L-R)_{HT} + PT$
L = 100 % ; R = 0 % or
R = 100 % ; L = 0 %

S1 open = AM
S1 closed = FM

Application circuit

Switching operation



S1 open = AM
S1 closed = FM

AF Power Amplifier IC with Thermal Shutdown

TDA 1037
TDA 1037 D

Bipolar circuit

Type	Ordering code	Package outline
TDA 1037	Q67000-A1229	SIP 9
TDA 1037 D	Q67000-A1387	DIP 18

An AF power amplifier designed for a wide range of supply voltages to enable a plurality of application modes with entertainment electronics. The amplifier operates in the push-pull B mode and is available in the SIP 9 package as well as in the DIP 18 package. The integrated shutdown protects the IC from overheating.

Features

- Wide supply voltage range: 4 V to 28 V
- High output power up to 8 W
- Large output current up to 2.5 A
- Simple mounting

Maximum ratings

Supply voltage $R_L \geqq 16\ \Omega$	V_S	30	V
$R_L \geqq 8\ \Omega$	V_S	24	V
$R_L \geqq 4\ \Omega$	V_S	20	V
Output peak current (not repetitive)	I_q	3.5	A
Output current (repetitive)	I_q	2.5	A
Junction temperature[1])	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
SIP 9 package			
Thermal resistance (junction-case)	$R_{th\,JC}$	12	K/W
(system-air)	$R_{th\,SA}$	70	K/W
DIP 18 package			
Thermal resistance (junction-case)	$R_{th\,JC}$	35	K/W
(system-air)	$R_{th\,SA}$	70	K/W

Operating range

Supply voltage range	V_S	4 to 28	V
Ambient temperature range	T_{amb}	−25 to 85	°C

*) May not be exceeded even as instantaneous value.

Characteristics

with reference to test circuit

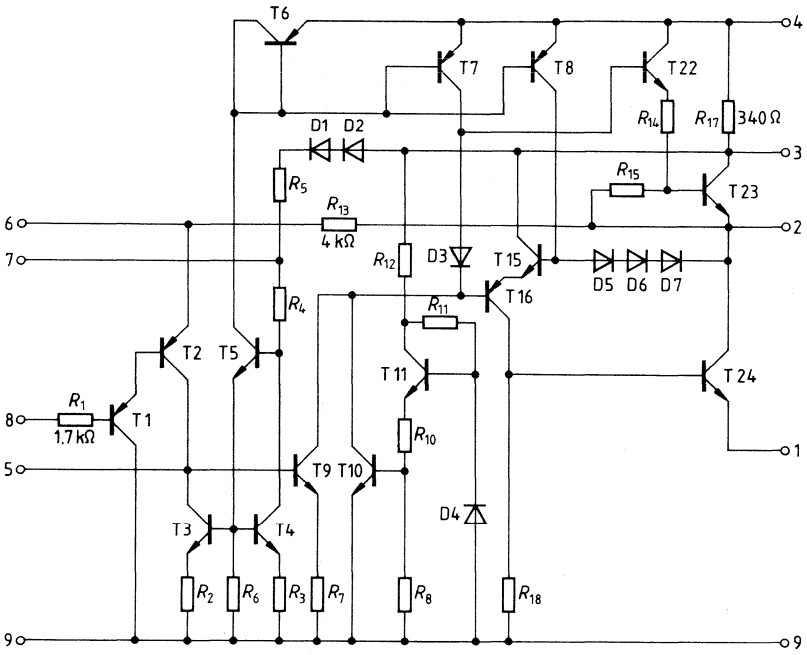
1. $V_S = 12$ V; $R_L = 4\ \Omega$; $C_1 = 1000\ \mu$F; $f_i = 1$ kHz; $T_{amb} = 25\,^\circ$C

		min	typ	max	
Quiescent output voltage	V_{q2}	5.4	6.0	6.6	V
Quiescent drain current	I_3+I_4		12	20	mA
Input DC current	I_{i8}		0.4	4	μA
Output power $THD = 1\%$	P_q	2.5	3.5		W
$THD = 10\%$	P_q	3.5	4.5		W
Voltage gain (closed loop)	G_V	37	40	43	dB
Voltage gain (open loop)	G_{V0}		80		dB
Total harmonic distortion ($P_q = 0.05$ to 2.5 W)	THD		0.2		%
Noise voltage referred to input ($f_i = 3$ Hz to 20 kHz)	V_n		3.8	10	μV_S
Disturbance voltage in acc. with DIN 45405 referred to input	V_d		2.5		μV
Hum suppression ($f_{hum} = 100$ Hz)	a_{hum}		48		dB
Frequency range (–3 dB)					
$C_4 = 560$ pF	f	40		20,000	Hz
$C_4 = 1000$ pF	f	40		10,000	Hz
Input resistance	R_{i8}	1	5		MΩ

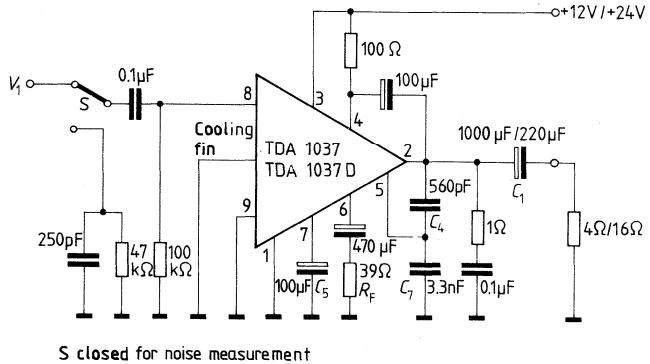
2. $V_S = 24$ V; $R_L = 16\ \Omega$; $C_1 = 220\ \mu$F; $f_i = 1$ kHz; $T_{amb} = 25\,^\circ$C

Quiescent output voltage	V_{q2}	11	12	13	V
Quiescent drain current	I_3+I_4		18	30	mA
Input DC current	I_{i8}		0.8	8	μA
Output power $THD = 1\%$	P_q		3.5		W
$THD = 10\%$	P_q	4.5	5.0		W
Voltage gain (closed loop)	G_V	37	40	43	dB
Voltage gain (open loop)	G_{V0}		80		dB
Total harmonic distortion ($P_q = 0.05$ to 3 W)	THD		0.2	0.5	%
Noise voltage with reference to input ($f_i = 3$ Hz to 20 kHz)	V_n		5	15	μV_S
Disturbance voltage in acc. with DIN 45405 referred to input	V_d		3.8		μV
Hum suppression ($f_{hum} = 100$ Hz)	a_{hum}		40		dB
Frequency range (–3 dB)					
($C_4 = 560$ pF)	f	40		20,000	Hz
($C_4 = 1000$ pF)	f	40		10,000	Hz
Input resistance	R_{i8}	1	5		MΩ

Circuit diagram

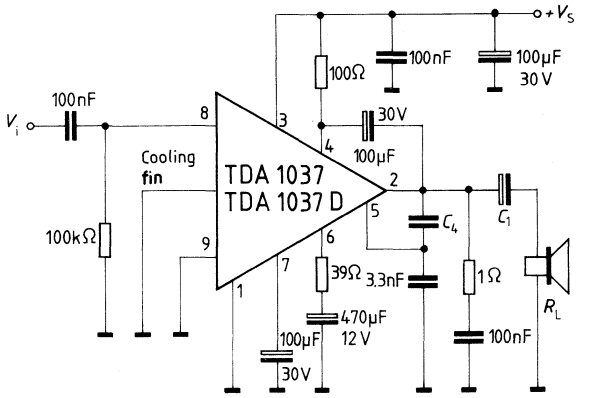


Measurement circuit



S closed for noise measurement

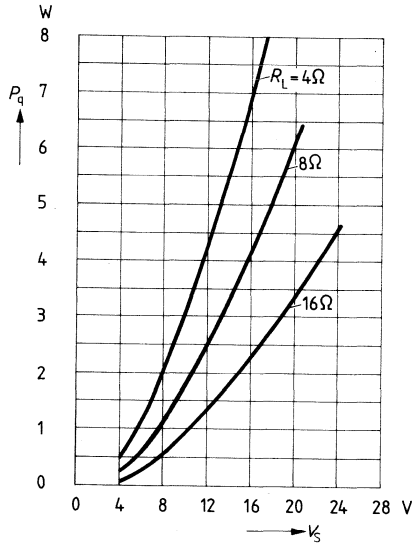
Application circuit



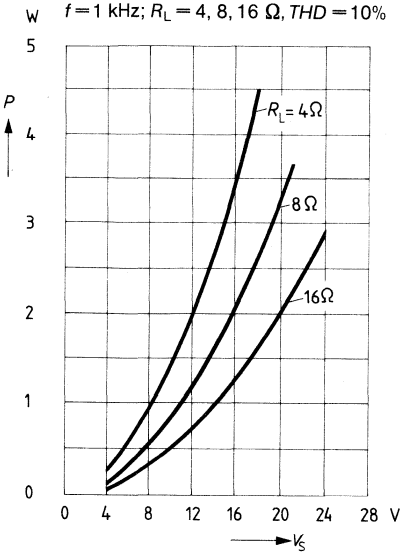
V_S	12 V	18 V	24 V
R_L	4 Ω	8 Ω	16 Ω
C_1	1000 µF	470 µF	220 µF

f_{max}	10 kHz	20 kHz
C_4	1000 pF	560 pF

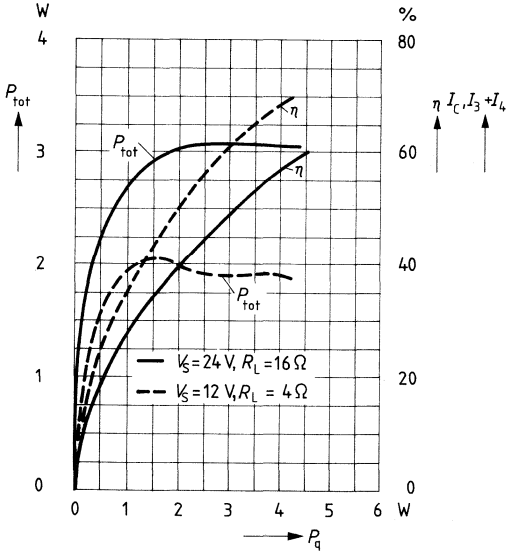
Output power versus supply voltage
THD = 10%; R_L = 4, 8, 16 Ω; *f* = 1 kHz



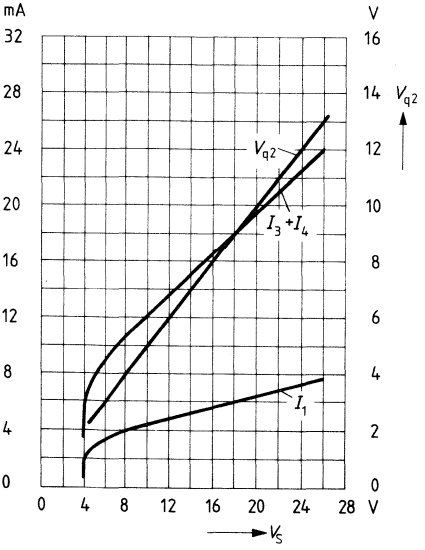
Max. power dissipation versus supply voltage at sine-shaped driving
f = 1 kHz; R_L = 4, 8, 16 Ω, *THD* = 10%



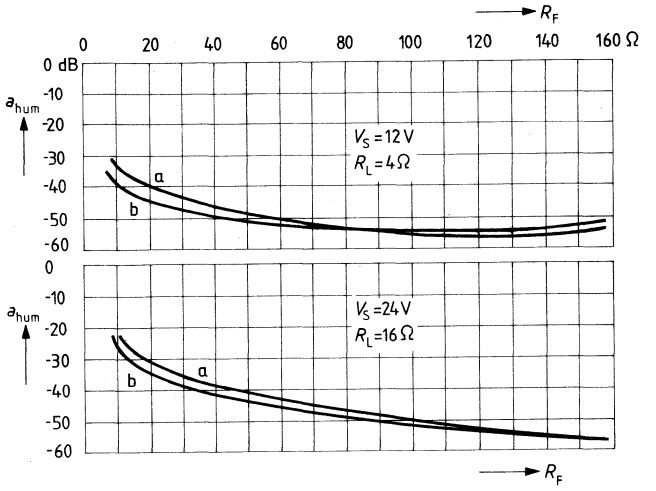
Total power dissipation and efficiency versus output power
THD = 10%; *f* = 1 kHz



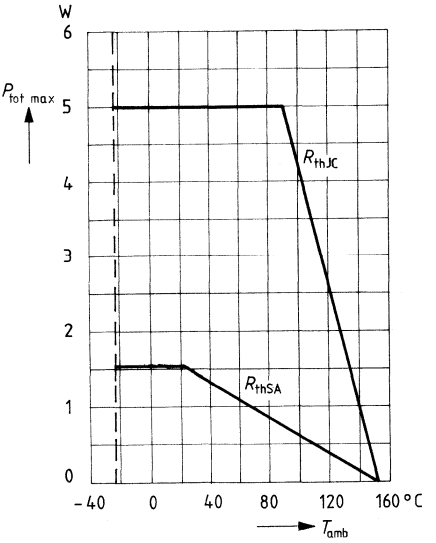
Quiescent drain current, quiescent current of output transistors, quiescent output voltage versus supply voltage



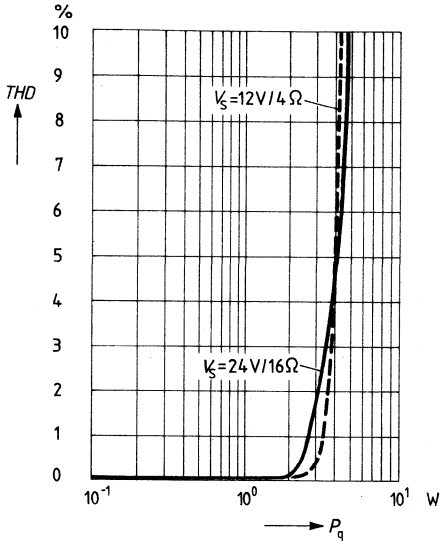
Hum suppression versus feedback resistance
$f_{hum} = 100$ Hz; $C_5 = 100$ µF
a: input short-circuited
b: input open



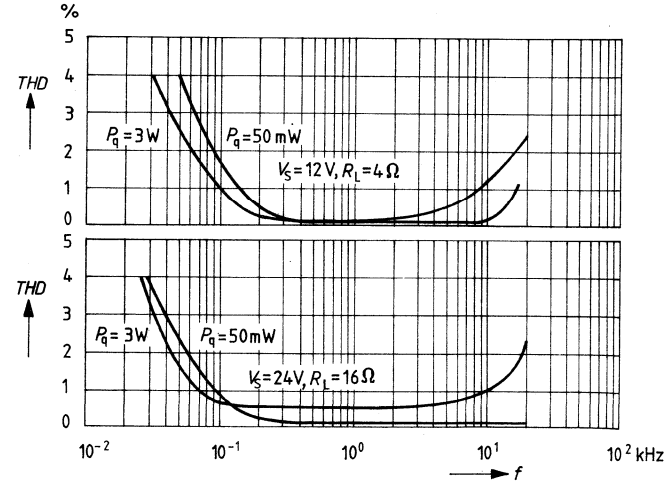
Max. total power dissipation versus ambient temperature



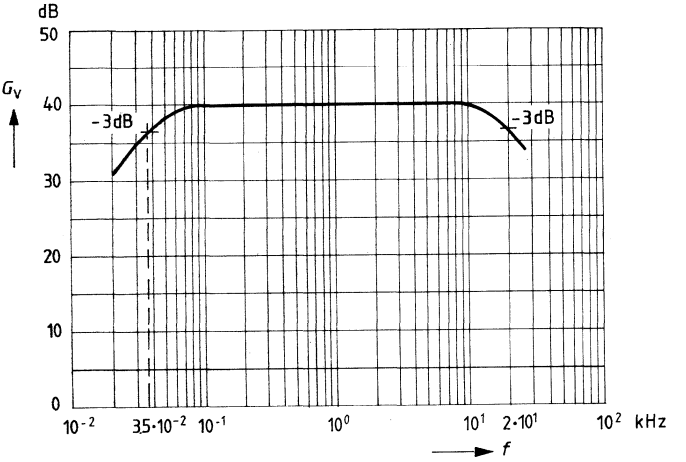
Total harmonic distortion versus output power
$f = 1$ kHz



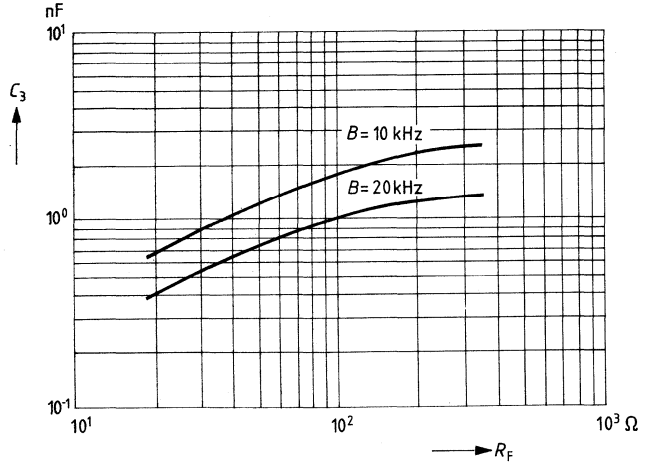
Total harmonic distortion versus frequency



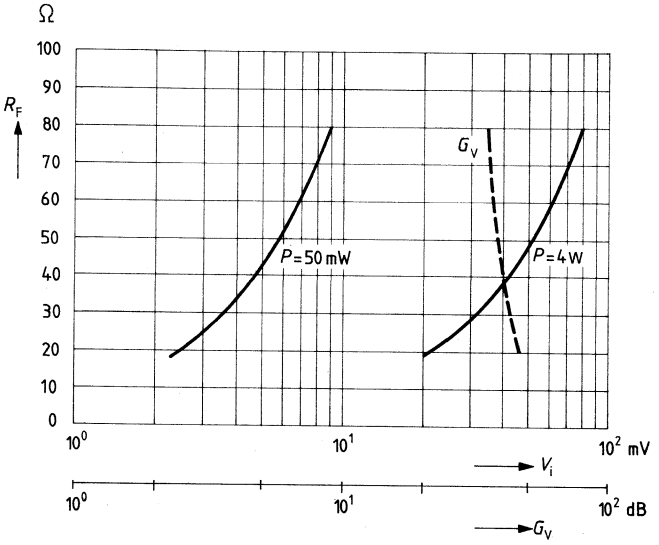
Voltage gain versus frequency
$V_S = 12$ V; $R_L = 4\ \Omega$



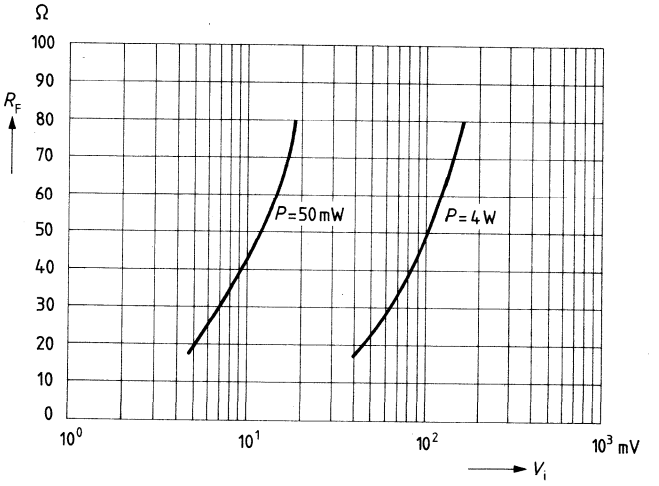
Bandwidth C_3 versus feedback resistance
$V_S = 12$ V; $R_L = 4\ \Omega$, $G_V = 40$ dB
$C_1 = 5 \cdot C_4$



Output power and voltage gain versus feedback resistance and input voltage
$V_S = 12$ V; $R_L = 4\ \Omega$; $f = 1$ kHz



Output power versus feedback resistance and input voltage
$V_S = 24$ V; $R_L = 16\ \Omega$; $f = 1$ kHz



Bipolar circuit

Type	Ordering code	Package outline
TDA 1046	Q67000-A1092	DIP 16

AM receiver circuit for LW, MW, and SW in car radios and mains operated radio receivers. The TDA 1046 includes controlled RF pre- and intermediate stages, a multiplicative push-pull mixer with separate oscillator, a controlled IF amplifier, a full-wave demodulator, an active low pass, as well as an amplifier to directly feed a field-strength indicator instrument. By means of its amplitude-controlled oscillator, the TDA 1046 is particularly suited for applications with varicap diodes. The circuit is balanced.

Features

- Internal AGC
- Superior large signal stability
- Internal demodulator
- Internal AF filtering
- Direct feed of a logarithmical field strength indicator (range 90 dB)
- High AF output voltage with low distortion factor
- Minimization of external components
- Provisions for additional RF intermediate circuitry

Maximum ratings

Supply voltage	V_S	18	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	90	K/W

Operating range

Supply voltage range	V_S	8 to 18	V
Oscillator frequency range	f_{OSC}	0.5 to 31	MHz
Input frequency range RF unit	f_{IRF}	0 to 30	MHz
IF unit	f_{IIF}	0.2 to 1	MHz
Ambient temperature range	T_{amb}	−15 to 85	°C

Characteristics ($V_7 = 10$ V, $T_{amb} = 25$ °C, $f_{mod} = 1$ kHz, $f_{iRF} = 1000$ kHz) see test circuit

		min	typ	max	
Current consumption	I_S	15	20	25	mA
AF output voltage and total harmonic distortion factor					
$m = 80\%$; $V_{iRF\,rms} = 1$ mV	$V_{AF\,rms}$	600	800	1000	mV
	THD		0.8	1	%
$m = 80\%$; $V_{iRF\,rms} = 25$ mV	$V_{AF\,rms}$	600	800	1000	mV
	THD		1.5	2	%
$m = 30\%$; $V_{iRF\,rms} = 1$ mV	$V_{AF\,rms}$	200	300	400	mV
	THD			0.6	%
$m = 30\%$; $V_{iRF\,rms} = 45$ mV	$V_{AF\,rms}$	200	300	400	mV
	THD			0.9	%
Total AGC range (variation of AF voltage $\Delta V_6 \leqq 6$ dB)	ΔG	85			dB
Input voltage for AGC triggering					
with tuned LC circuit	$V_{i9\text{-}10}$		19		µV
with wideband circuit	$V_{i9\text{-}10}$		28		µV
Signal-to-noise ratio[1] (measured at 50 Ω, $m = 30\%/0\%$)					
at $V_{iRF} = 2.5$ µV	$\frac{S+N}{N}$		6		dB
$= 14$ µV	$\frac{S+N}{N}$		26		dB
$= 1$ mV	$\frac{S+N}{N}$	50	53		dB
Instrument current ($V_S = 15$ V; at G_{min}; $V_{11} \leqq V_7 - 3$ V)	I_{11}	1		1.5	mA
AF output resistance	R_{q6}	2.25	3	3.75	kΩ
Noise voltage in accordance with DIN 45405	V_n		500		µV

1) Disturbance voltage spacing unweighted (DIN 45405)

Additional characteristics RF stage

($V_S = 10$ V, $T_{amb} = 25$ °C; $f_{iRF} = 1000$ kHz, $f_{mod} = 1$ kHz, $m = 95\%$, $f_{IF} = 450$ kHz)

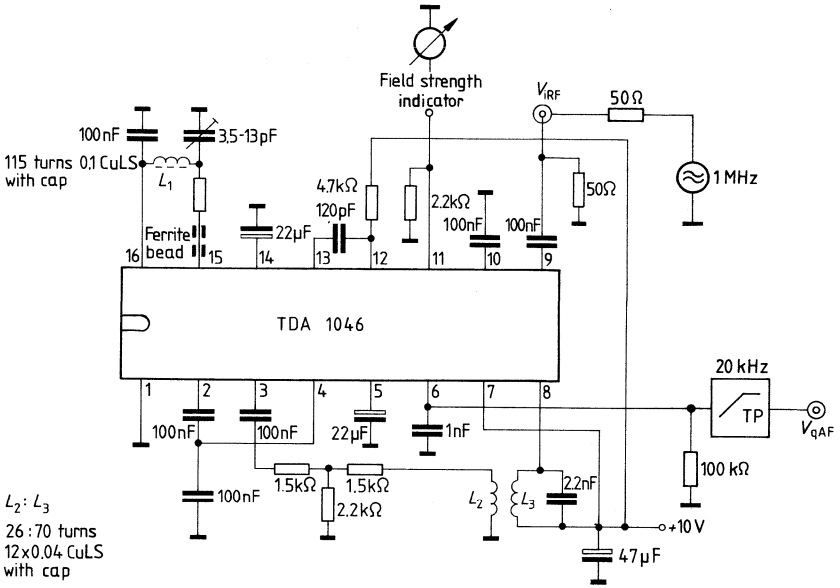
		min	typ	max	
Oscillator voltage ($f_{OSC} = 1.45$ MHz)	$V_{15\,rms}$			350	mV
AGC range of RF prestage	ΔG	40			dB
Voltage gain	$G_{V/8\text{-}9/10}$		40		dB
Voltage gain of RF stage	$G_{V13\text{-}9/10}$		20		dB
Input impedance $Z_{i9\text{-}1} =$	$Z_{i10\text{-}1}$		2/5		kΩ/pF
	$Z_{i9\text{-}10}$		4/5		kΩ/pF
Input voltage for overload ($THD_{mod} = 10\%$)	$V_{i9\text{-}10\,pp}$		2		V
Reference voltage ($I_{16} \leqq 3$ mA)	V_{16}	3	3.3	3.8	V

Additional characteristics IF stage

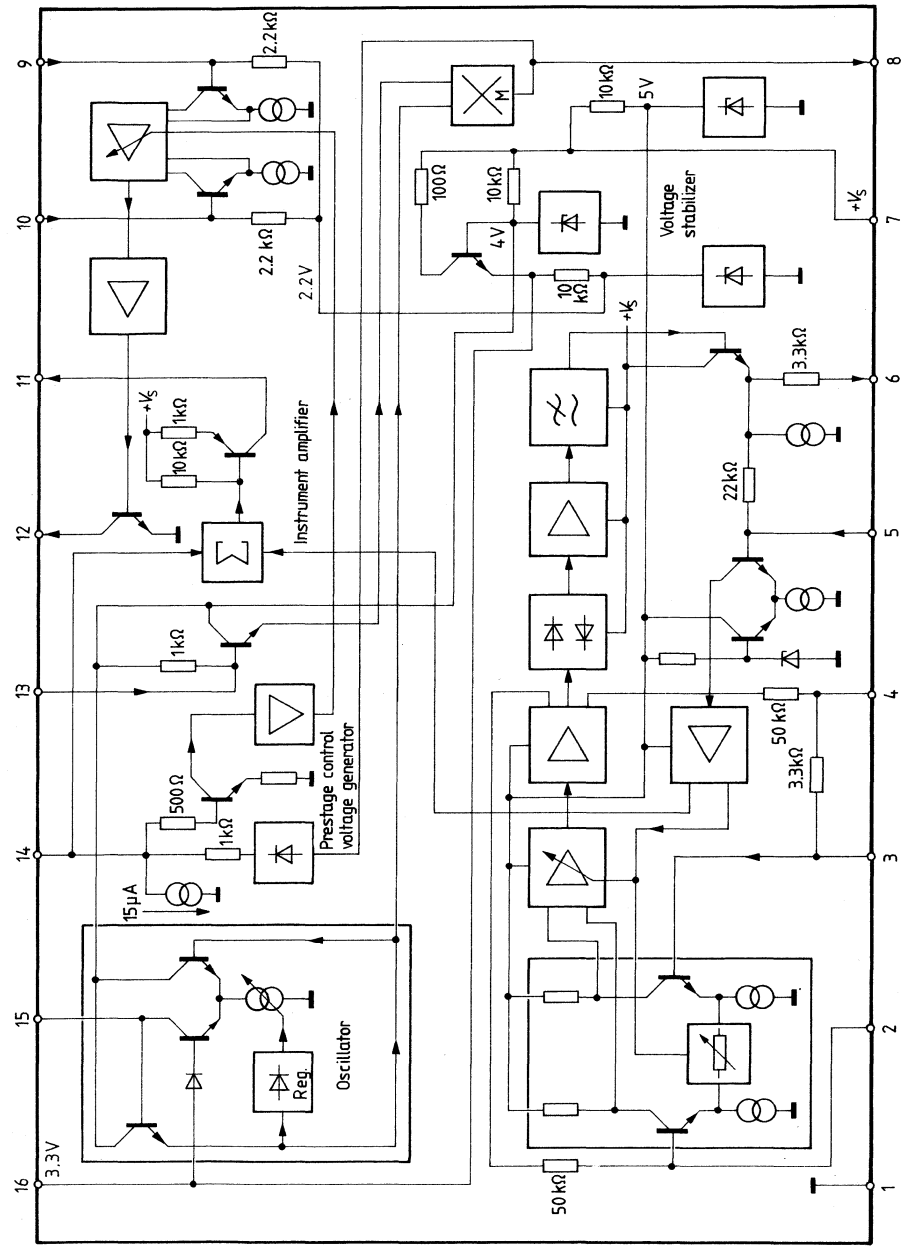
($V_S = 10$ V, $T_{amb} = 25$ °C, $f_{IF} = 450$ kHz, $f_{mod} = 1$ kHz, $m = 95\%$)

AGC range at 450 kHz	ΔG	45			dB
Input voltage for overload ($THD = 10\%$)	$V_{3\,rms}$		120		mV
Output impedance	Z_{q8}		100		kΩ
Input impedance	Z_{i3}		3.3/3		kΩ/pF
AF output voltage ($V_{3\,rms} = 10$ mV; $m = 30\%$)	$V_{AF\,rms}$	245			mV

Measurement circuit

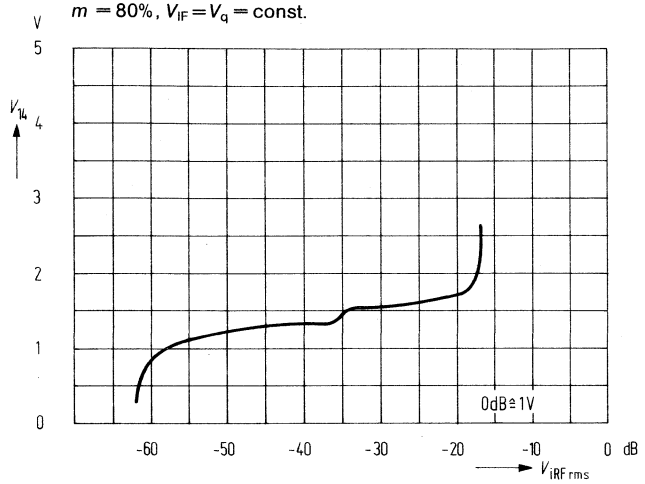


Block diagram



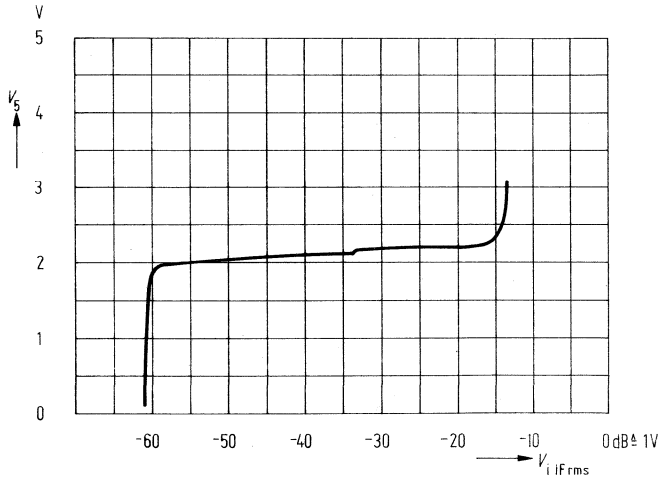
Prestage control

$V_S = 10$ V; $T_{amb} = 25$ °C; $f_{iRF} = 1000$ kHz; $f_{mod} = 1$ kHz, $m = 80\%$, $V_{IF} = V_q = \text{const.}$

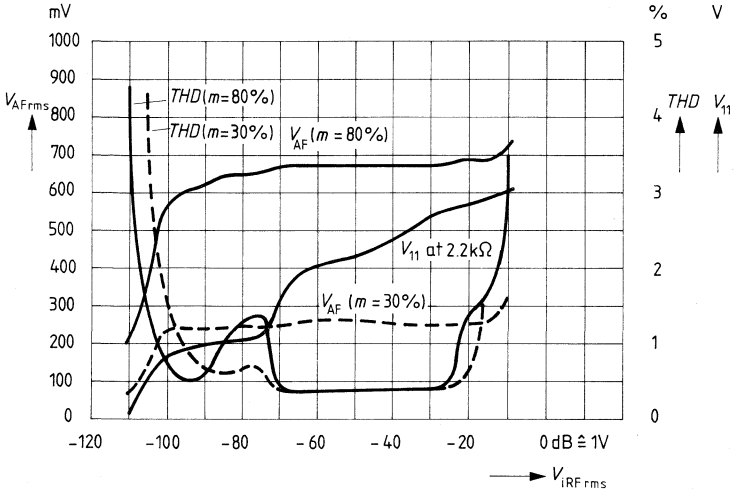


IF stage control

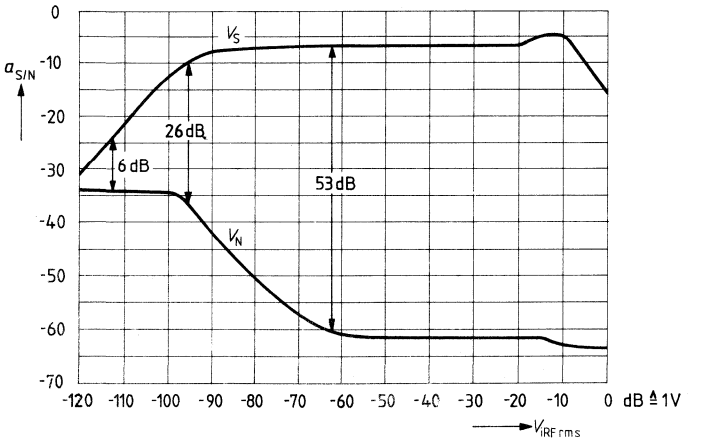
$V_S = 10$ V; $T_{amb} = 25$ °C; $f_{iIF} = 455$ kHz; $f_{mod} = 1$ kHz; $m = 80\%$; $V_{AF} = V_6 = \text{const.}$



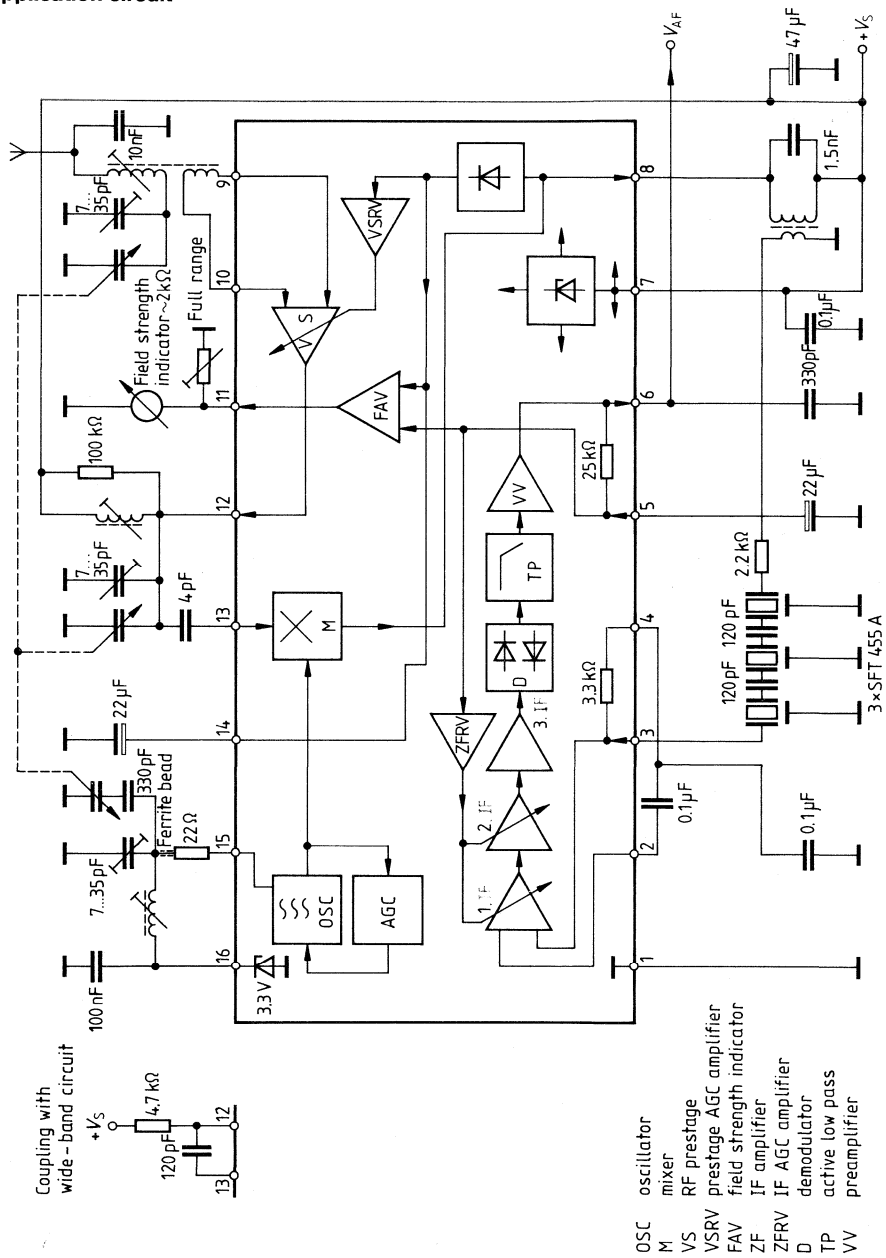
AF output voltage, total harmonic distortion, instrument voltage versus RF input voltage
$V_S = 15$ V, $f_{IRF} = 1000$ kHz, $f_{mod} = 1$ kHz Coupling with wideband circuit



Signal-to-noise ratio versus input voltage
$V_S = 15$ V; $m = 30\%$; $f_{IRF} = 1000$ kHz; $f_{mod} = 1$ kHz



Application circuit



Coil data

1. RF prestage		
primary	105 turns	15x0.04 CuLS
sec. (pin 9–10)	7 turns	15x0.04 CuLS
wound on Vogt D 21-2375.1		
2. RF intermediate circuit		
	105 turns	15x0.04 CuLS
wound on Vogt D 21-2375.1		
3. Oscillator circuit		
	115 turns	0.10 CuLS
wound on Vogt D 41-2519 with cap		
4. IF circuit (pin 8)		
primary (*LC* circuit)	70 turns	12x0.04 CuLS
secondary	26 turns	12x0.04 CuLS
wound on Vogt D 41-2519 with cap		

Variable capacitor

HOPT triple rotary capacitor set MG 06-05 A

FM IF Amplifier with Demodulator for Radio Receivers

TDA 1047

Bipolar circuit

Type	Ordering code	Package outline
TDA 1047	Q67000-A1091	DIP 18

FM-IF amplifier for radio sets with 8-stage amplifier and symmetrical coincidence demodulator. The TDA 1047 additionally offers provisions for feeding an amplitude indicator and either positive or negative mono-stereo voltage as well as an AFT output (push-pull current output) with automatic switch-off. The included squelch can be adjusted within an input signal range of more than 40 dB and depends on detuning.

Features

- Excellent limiting qualities
- Excellent frequency stability of demodulator characteristic
- Large range of operating voltage between 4 and 18 V
- Low current consumption
- Externally adjustable squelch
- Few external components

Maximum ratings

Supply voltage	V_S	18	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	90	K/W

Operating range

Supply voltage range	V_S	4 to 18	V
Frequency range	f	0 to 15	MHz
Ambient temperature range	T_{amb}	−25 to 85	°C

Characteristics ($V_S = 12$ V; $T_{amb} = 25$ °C; $f_i = 10.7$ MHz; $f_{mod} = 1$ kHz; $\Delta f = \pm 75$ kHz; Q_B approx. 20) see test circuit

		min	typ	max	
Current consumption ($I_{14} = 0$)	I_{12}	9	12	15	mA
Voltage for field strength indicator ($R_{14} = 3.3$ kΩ)					
$V_{irms} = 160$ mV	V_{14}	1.6	2		V
$V_{irms} = 16$ μV	V_{14}		10	20	mV
Current	I_{14}			3.6	mA
Voltage for squelch adjustment (approx. log.)					
$V_{irms} = 8$ mV	V_{15}		0		V
$V_{irms} = 16$ μV	V_{15}	2.2	2.5		V
Current	I_{15}			3.6	mA
AF output DC voltage	V_7		2.1		V
AF output voltage ($V_i = 10$ mV; $THD = 0.4\%$)	$V_{7\,rms}$	270	300		mV
Internal DC voltage of output emitter follower	I_7	180	200		μA
Total harmonic distortion ($V_i = 10$ mV)[1]	THD		0.4	0.8	%
Input voltage for limiting[2]	V_i		30	50	μV
Input resistance	$R_{i\,18}$	10			kΩ
AF output resistance[3] (emitter follower output)	$R_{q\,7}$		0.3	1	kΩ
Threshold of detuning-depending squelch (referred to $f = 10.7$ MHz)	Δf		± 100	± 150	kHz
Switching threshold for AFT OFF	V_2			20	mV
Input resistance	$R_{i\,2}$	40	100		kΩ
Voltage for AFT OFF	V_3	0.8			V
Current deviation of the AFT output	ΔI_5		± 150		A
IF output voltage for limiting	$V_{8\text{-}11\,pp}$		500		mV
Input resistance for demodulator circuit	$R_{9\text{-}10}$		5.4		kΩ
Recommended voltage for demodulator circuit[4]	$V_{9\text{-}10\,pp}$		500		mV
Threshold for AF OFF	V_{13}		0.85	0.95	V
AF ON	V_{13}	0.5	0.6		V
Hysteresis for switching threshold	ΔV_{13}		120	200	mV
Internal resistance for AF switch-off time constant	$R_{q\,6}$		500		Ω
AM suppression ($V_i = 10$ mV; $m = 30\%$)	a_{AM}	60			dB
Signal-to-noise-ratio ($V_i = 10$ mV)	$a_{S/N}$	70			dB
AF suppression at muting circuit ($V_i = 10$ mV)	a_{AF}		60		dB

For footnotes refer to page 387.

[1] In the case of using a band filter: $THD_{max} = 0.3\%$

[2] Limiting application for $V_{AF} = -3$ dB

[3] The output resistance R_{q7} can be reduced by connecting a resistor of at least 2.7 kΩ between pin 7 and ground.

[4] The recommended voltage at the demodulator circuit V_{9-10} can be adjusted by the capacitors C_{8-9} and C_{10-11}, which are also influencing the voltage V_{14} and V_{15}.

If the slider of potentiometer *P* is grounded, the field-strength-dependent squelch is switched off.

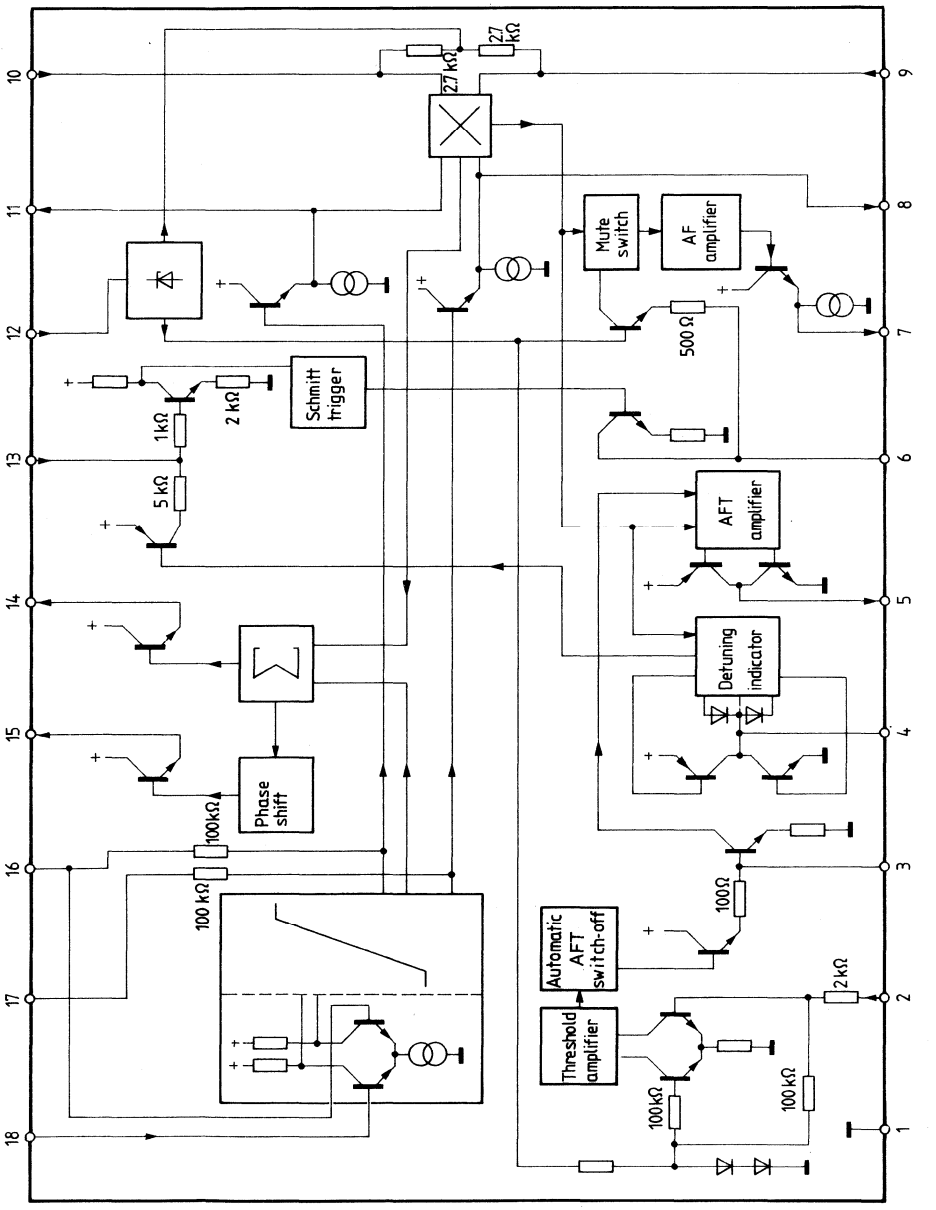
If pin 13 is grounded, both the field-strength- and the detuning-dependent squelch are switched off.

The noise level between the transmitters becomes more or less audible, when pin 6 is loaded with a resistance to +12 V in case of "squelch on". Noise attenuation increases with the size of the resistance ($R \geqq 10$ kΩ).

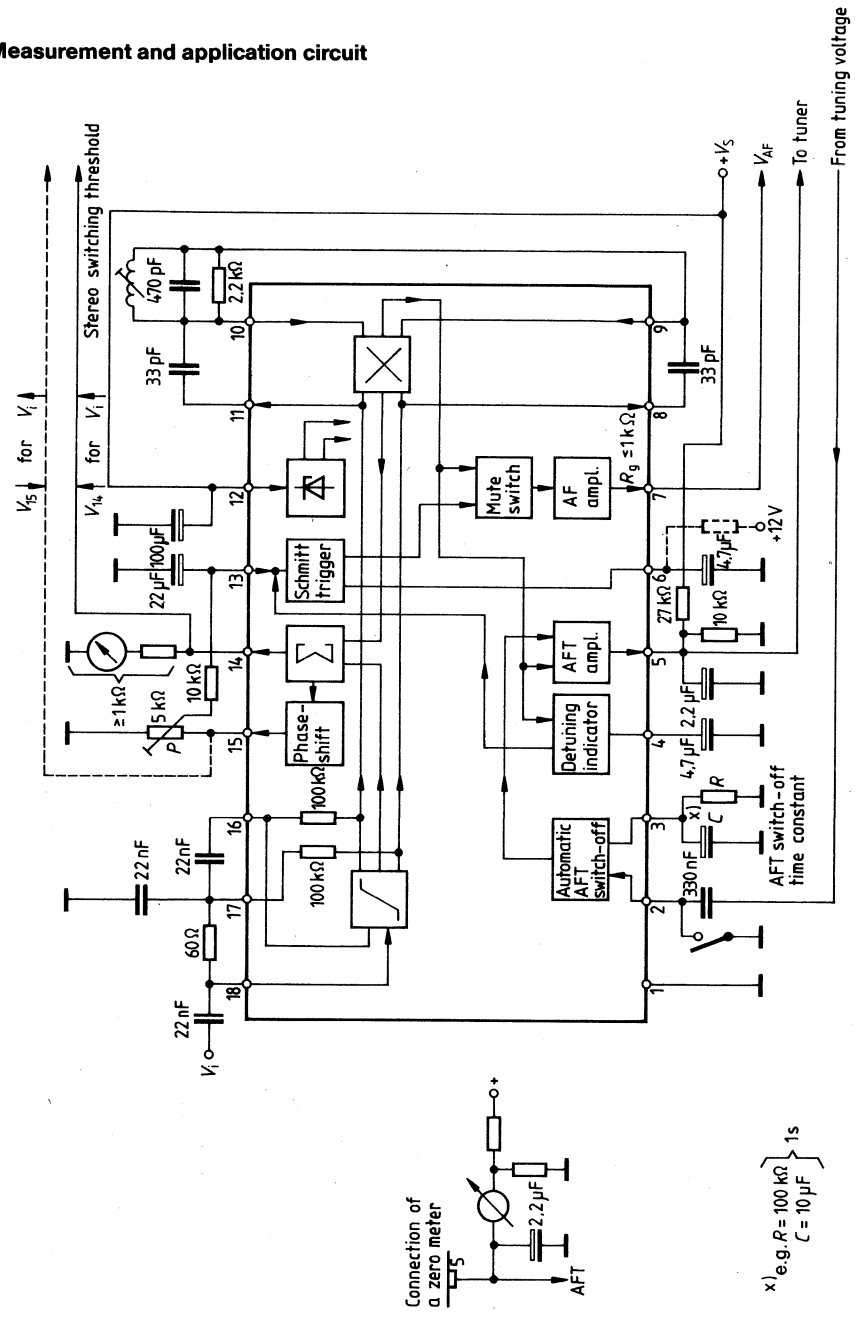
Pin configuration

Pin No.	Function
1	Ground
2	Sensor input for AFT switch off
3	AFT switch-off time constant
4	Low-pass capacitor for detuning-dependent AF switch off
5	AFT output (push-pull output)
6	Low-pass capacitor for suppression of switch off clicks in case of detuning and insufficient field strength
7	AF output (emitter follower with constant-current source)
8	Output of limiter amplifier
9 } 10	Phase shifting circuit
11	Output of limiter amplifier
12	Positive operating voltage
13	Input for amplitude-dependent switch off
14	Instrument connection and stereo switching voltage (positive going)
15	Squelch and stereo switching voltage (negative going)
16 } 17	Feedbacks for IF amplifier
18	IF input

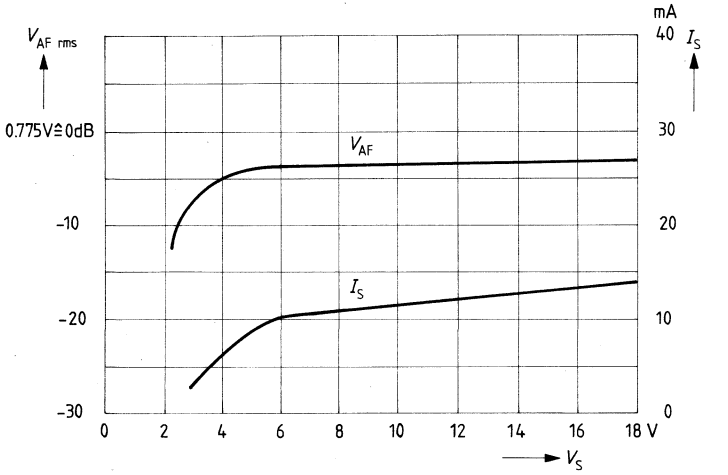
Block diagram



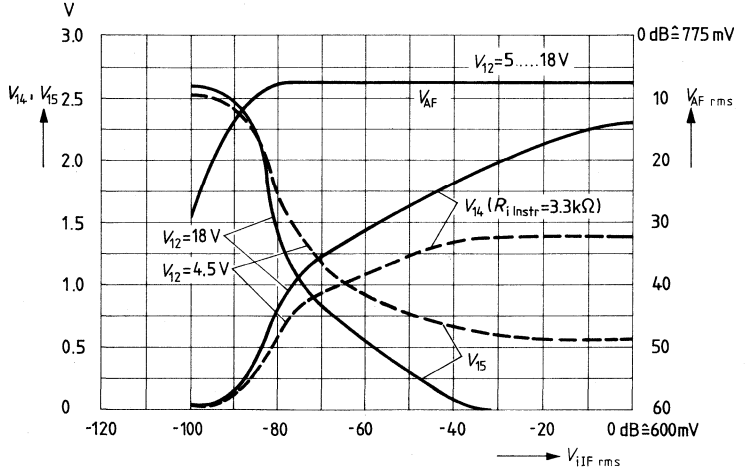
Measurement and application circuit



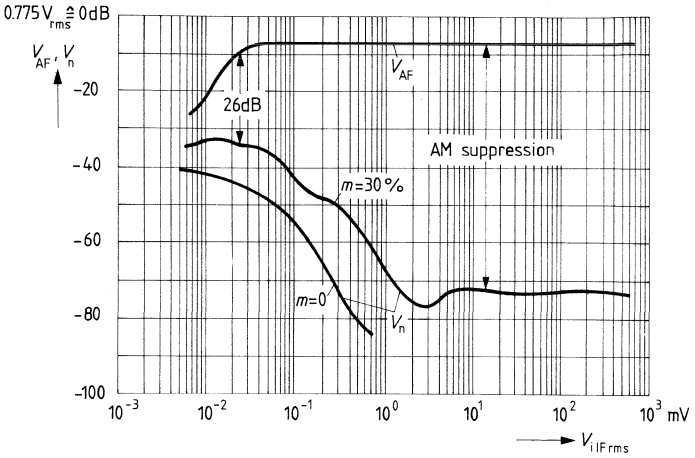
AF output voltage, total current consumption versus supply voltage
$V_{IIF} = 60\ mV_{rms}$ wideband, pin 13 to ground, $V_{9\text{-}10} = 500\ mV_{pp}$



AF output voltage, indicator voltage, squelch voltage versus input voltage
$V_{12} = 15\ V$; $f = 10.7\ MHz$, $\Delta f = \pm 75\ kHz$, $f_{mod} = 1\ kHz$
$V_{9\text{-}10} = 500\ mV_{pp}$, wideband-measured at 100 nF, $THD = 0.4\%$



AF output voltage, noise voltage versus input voltage
$f = 10.7$ MHz, $\Delta f = \pm 75$ kHz, $V_{12} = 15$ V



Controlled AM Amplifier with Demodulator and AF Volume Control

TDA 1048 G

Bipolar circuit

Type	Ordering code	Package outline
TDA 1048 G	Q67000-A1090	DIP 16

The integrated circuit TDA 1048 G contains a gain-controlled push-pull amplifier, a demodulator, and a DC volume control. The AF outputs are referred to ground and stabilized against the hum of the supply voltage.

The IC TDA 1048 G is particularly suited for use in the sound section of TV sets of French Standard (amplitude modulation).

Features

- High input sensitivity
- Low-distortion control
- Low-distortion demodulation
- Volume control by means of DC voltage
- Internally stabilized supply voltage

Maximum ratings

Supply voltage	V_S	16.5	V
Output current	I_{11}	5	mA
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	90	K/W

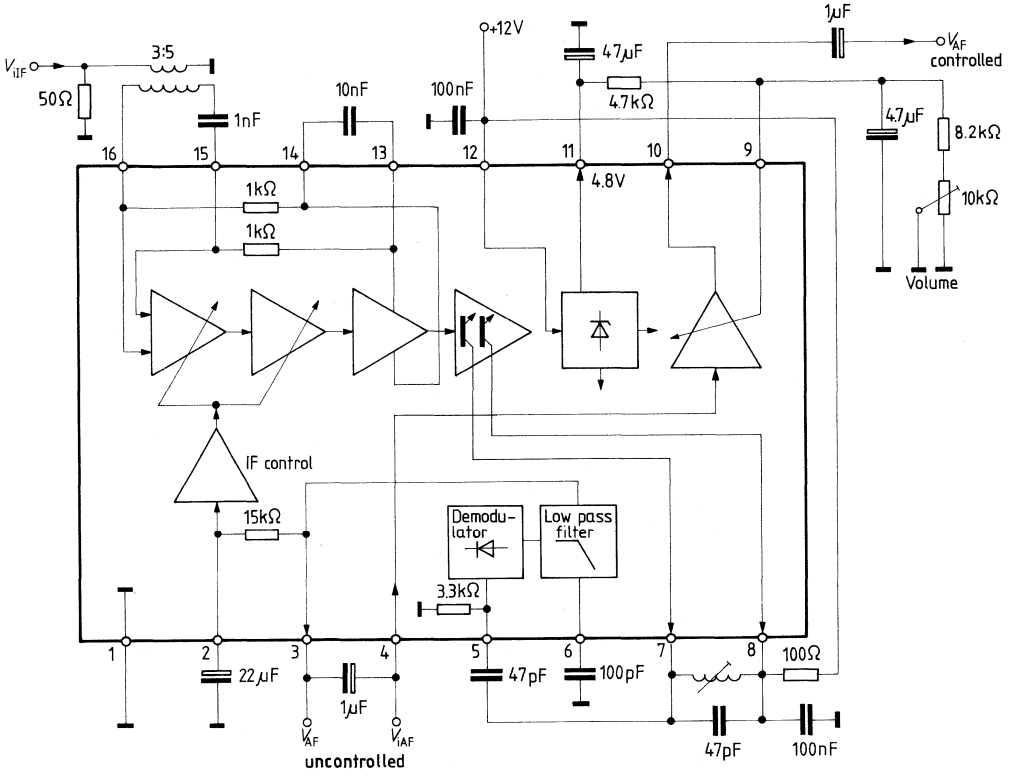
Operating range

Supply voltage range	V_S	10 to 15	V
Ambient temperature range	T_{amb}	0 to 60	°C

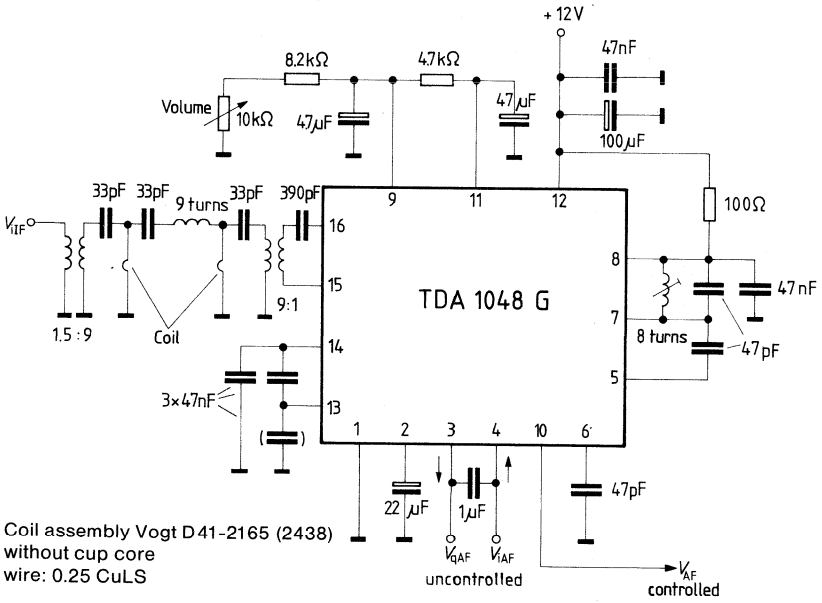
Characteristics ($V_S = 12$ V; $f_i = 40$ MHz; $f_{mod} = 1$ kHz; $T_{amb} = 25$ °C)

		min	typ	max	
Total current consumption	$I_{12}+I_7+I_8$	29	37	45	mA
Output DC currents of amplifier (difference max. 100 mV at 100 Ω)	$I_7 = I_8$		4		mA
Input voltage for AGC threshold	V_i	100			µV
AGC range	ΔG	50	60		dB
AF output voltage ($m = 80\%$)	$V_{q10\,rms}$	0.9	1.2	1.5	V
AF output dc voltage	V_{10}	3.7	4.4	5.1	V
Total harmonic distortion ($m = 80\%$)	THD		1.3	2.0	%
Output resistance	R_{q3}		200	300	Ω
	R_{q10}		50	100	Ω
Load resistance	R_{L3}	3.3			kΩ
	R_{L10}	3.3			kΩ
Stabilized voltage	V_{11}	4.4		5.8	V
Range of volume control	$\Delta G_{10\text{-}4}$	70	80		dB
Gain of the AF section (slight spread)	$\Delta G_{10\text{-}4}$	6	7		dB
Input resistance	R_{i4}	6.5			kΩ
Potentiometer resistance for −30 dB attenuation	R_{pot}	4.5	5	5.3	kΩ

Test circuit and block diagram

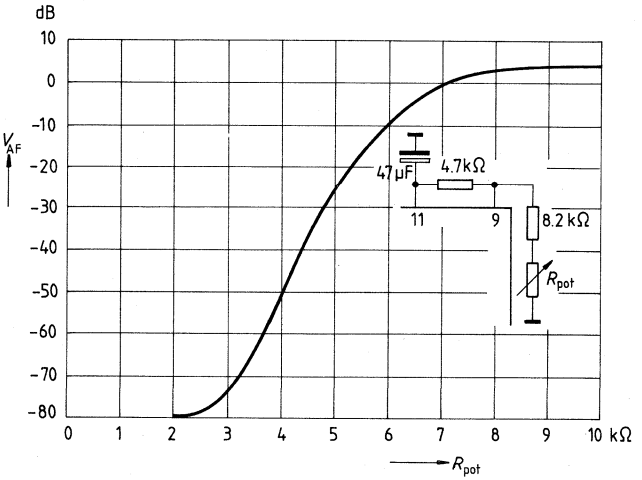


Application circuit for $f_{IIF} = 39.2$ MHz



Coil assembly Vogt D41-2165 (2438)
without cup core
wire: 0.25 CuLS

AF output voltage versus potentiometer resistance
$V_S = 15$ V



Controlled AM Amplifier for French Sound IF Standard

TDA 2048

Bipolar circuit
MOS handling

Type	Ordering code	Package outline
TDA 2048	Q67000-A1773	DIP 18

The TDA 2048 contains a 4 stage AM broadband amplifier, a limiter, and a mixer for the synchronous demodulation of AM signals. The AF section contains standard VCR connections for CCIR and French standards, a CCIR input which can be switched into the circuit, and a volume control.

Features

- High input sensitivity
- Low-distortion regulation
- Low-distortion demodulation
- DC volume control
- Internally stabilized supply voltage

Maximum ratings

Supply voltage	V_S	16.5	V
Switching voltage	V_2	16.5	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	70	K/W

Operating voltage

Supply voltage range	V_S	10 to 15	V
Frequency range	f	10 to 60	MHz
Control voltage range	$V_{control}$	0 to 5	V
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics ($V_S = 12$ V; $T_{amb} = 25$ °C; $f_{IF} = 39.2$ MHz; $f_{mod} = 1$ kHz)

		min	typ	max	
Total current consumption	I_7		40	60	mA
Stabilized voltage	V_3	5.4	6	6.6	V
AGC range	ΔG	60			dB
IF control voltage (V_{max})	V_2	0		0.9	V
(V_{min})	V_2	3		5	V
Input voltage for AGC threshold	$V_{17,18}$		50		µV
Max. IF input voltage ($THD \leqq 5\%$; $m = 80\%$)	$V_{17,18}$			150	mV
AF output voltage ($V_{IIF\,rms} = 10$ mV, $m = 30\%$)					
(record CCIR)	$V_{6\,rms}$	400	600	800	mV
(record French)	$V_{11\,rms}$	66	100	133	mV
($V_5 = 0.8 \times V_3$)	$V_{4\,rms}$		300		mV
Total harmonic distortion					
($V_{IIF} = 10$ mV, $m = 30\%$)	THD_{11}			1	%
($V_{IIF} = 10$ mV, $m = 80\%$)	THD_{11}			4	%
Total harmonic distortion volume control and op amp 1 ($V_{12} = 150$ mV, $V_5 = 0.8\ V_3$)	THD_4			1	%
Input voltage (playback CCIR)	$V_{6\,rms}$		600		mV
(playback French)	$V_{14\,rms}$		100		mV
(CCIR operation)	$V_{10\,rms}$		100		mV
Range of volume control	ΔG_{LR}	80			dB
Voltage at volume control pin					
for max. volume	V_5			$0.8 \times V_3$	V
for min. volume	V_5	0			V
Switching thresholds					
VCR playback (CCIR, French)	$V_{2,13}$	8		15	V
Switching current					
VCR playback (CCIR, French)	$I_{2,13}$	0		0.3	mA
Switching threshold (CCIR operation)	V_{16}	0		1	V
Switching current (CCIR operation)	I_{16}	0		0.5	mA
Switching threshold (VCR record, French)	V_{13}	0		5	V
Cross-talk attenuation at switched-off AF inputs	a_{CR}	60			dB
Gain pin 12, 14 to pin 6	G_{AF}		6		dB
pin 12, 14 to pin 4	G_{AF}		3		dB

Additional characteristics ($V_S = 12$ V; $T_{amb} = 25$ °C)
(Data is not guaranteed by series measurement)

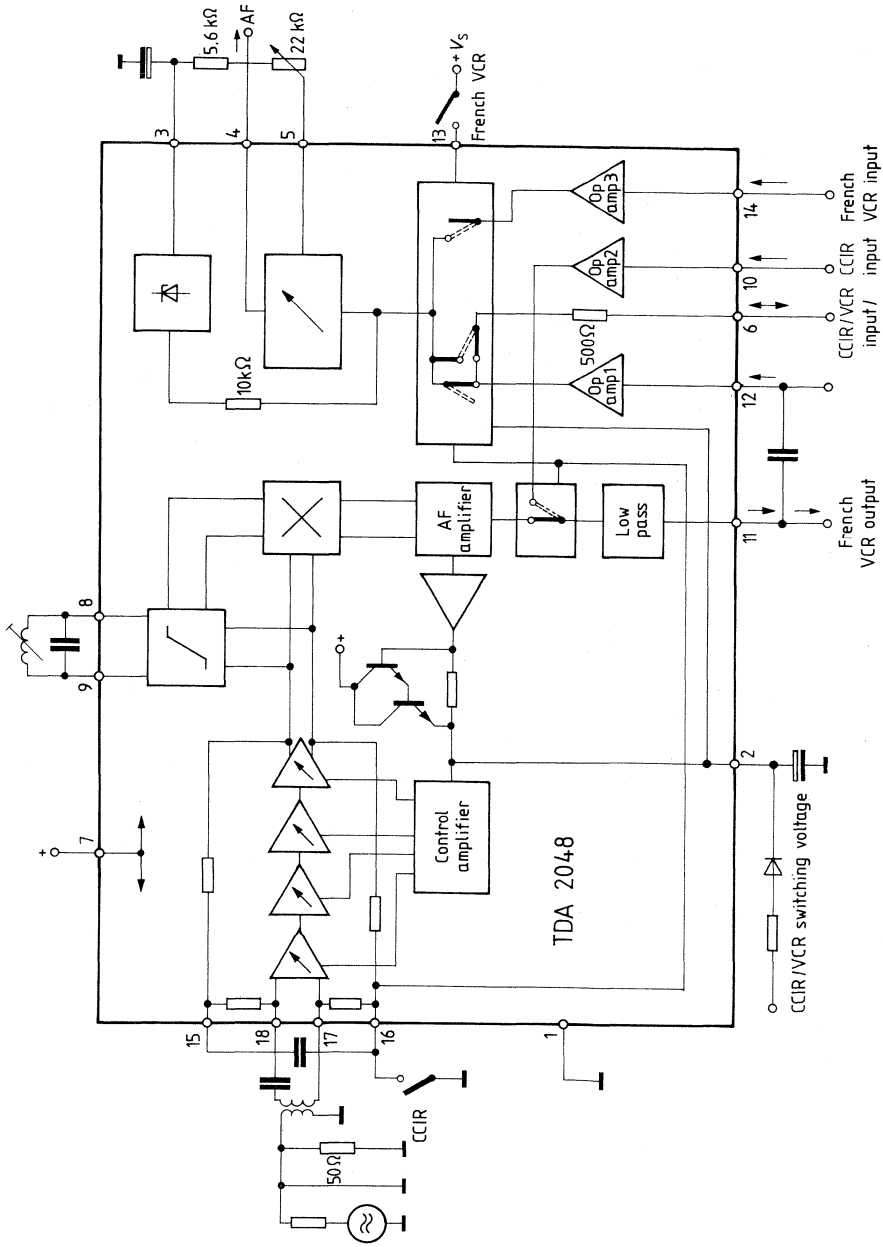
Input resistance	R_{i12}	10			kΩ
Input resistance (CCIR playback)	R_{i10}	10			kΩ
Input resistance (VCR playback)	$R_{i6,14}$	10			kΩ
Output resistance (VCR record)	$R_{q6,11}$			200	Ω
AF output resistance	R_{q11}			200	Ω
AF output resistance	R_{q4}			200	Ω

Truth table

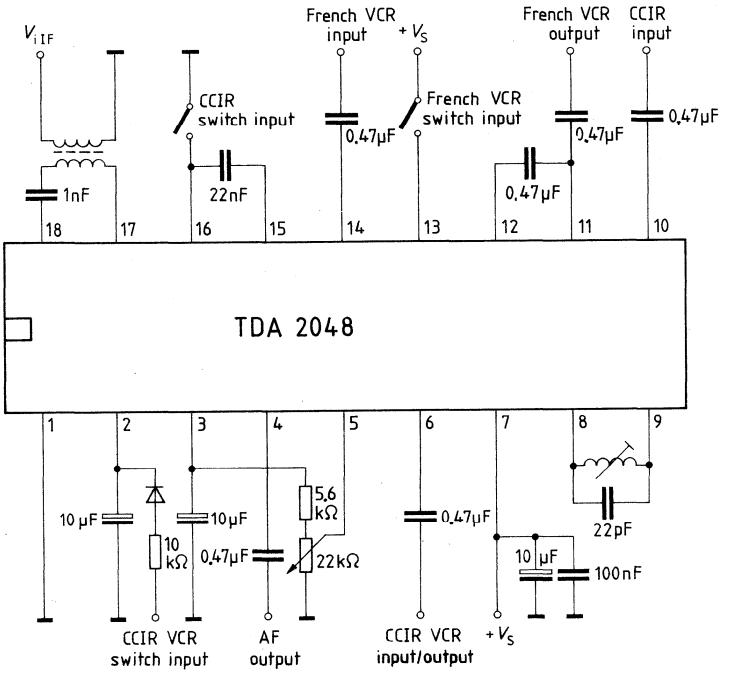
	Switch inputs			Functions					Operating mode
	CCIR Pin 16	CCIR VCR Pin 2	French VCR Pin 13	AF amplifier Pin 17/18	French VCR Pin 11	Op amp 1 Pin 12	Op amp 2 Pin 10	Op amp 3 Pin 14	CCIR VCR in-output Pin 6	
desired operation										
I	0	0	0	ON	ON	ON	OFF	OFF	Record IF	IF reception
II	L	0	0	OFF	ON	ON	ON	OFF	Record CCIR	CCIR playback
III	0	H	0	OFF	OFF	OFF	OFF	OFF	Playback VCR	Playback CCIR-VCR
IV	0	0	H	ON	ON	OFF	OFF	ON	Record French VCR	Playback French VCR + Teletext (Antiope)
V	L	0	H	OFF	ON	OFF	ON	ON	Record CCIR	Teletext (CCIR)
	0	0	L	corresponds to operating mode			I			
	0	L	0				I			
	0	L	L				I			
	0	L	H				IV			
	0	H	L				III			
	0	H	H				III			
	L	0	L				II			
	L	L	0				II			
	L	L	L				II			
	L	L	H				V			
	L	H	0				III			
	L	H	L				III			
	L	H	H				III			
	H	X	X	not permissible						

0 ≙ open
L ≙ to ground
H ≙ to $+V_S$
X ≙ any

Block diagram and measurement circuit



Application circuit



Video IF IC for Black/White and Color TV Sets

TDA 2440
TDA 2441

Preliminary data

Bipolar circuit

Type	Ordering code	Package outline
TDA 2440	Q67000-A2164	DIP 16
TDA 2441	Q67000-A2174	

The high gain, controlled video IF amplifier with controlled demodulator includes low-impedance outputs for the positive and negative video signal as well as a gated control and delayed tuner control.

TDA 2440: for PNP tuners
TDA 2441: for NPN tuners

Features

- High degree of integration
- Extensive control range
- High input sensitivity
- Minimal 1.07 MHz interference (920 kHz for US standards)
- Positive and negative video signal
- Adjustable white level
- Superior tuning properties

Maximum ratings

Supply voltage	V_S	16.5	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	70	K/W

Operating range

Supply voltage range	V_S	10.5 to 15.8	V
IF frequency	f_{IF}	up to 60	MHz
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics ($V_S = 12$ V; $T_{amb} = 25$ °C)

Current consumption	I_{11}	55	mA
Stab. reference voltage	V_{12}	6.0	Vdc
Controlled current for tuner ($V_{14} = 0.5\ V_{11}$)	I_{14}	4.0	mA
Tuner AGC threshold	$V_{13/1}$	0 to 4.0	V
Gating pulse voltage			
pos. gating pulse	V_1	3.0	V
neg. gating pulse	V_1	−3.0	V
Input voltage at V_{max} ($V_3 = 3\ V_{pp}$)	$V_{15/16}$	max 100	μV
AGC range	ΔG	60	dB
Video output voltage (pos.) ($R_L = \infty$)	V_{q3pp}	3.0	V
Sync pulse level	V_3	2.0	Vdc
DC voltage ($V_2 = 4$ V; $V_{15/16} = 0$)	$V_{3/10}$	5.3	Vdc
Output current			
(to ground through R)	I_{q3}	−5.0	mA
(to plus $V_3 = 7$ V)	I_{q3}	2.0	mA
Video output voltage (neg.) ($R_L = \infty$)	V_{4pp}	3.0	V
Sync pulse level	$V_{4/10}$	$V_{11} - 2.0$	Vdc
DC voltage ($V_2 = 4$ V; $V_{15/16} = 0$)	$V_{4/10}$	$V_{11} - 5.3$	Vdc
Output current			
(to ground through R)	I_{q4}	−5.0	mA
(to plus $V_4 = V_{11}$)	I_{q4}	1.0	mA
IF control voltage			
V_{max}	$V_{2/10}$	min 0	Vdc
V_{min}	$V_{2/10}$	max 4	Vdc

Additional application data[1)]

Input impedance	$Z_{i15/16}$	1.8/2	kΩ/pF
Output impedance	$Z_{q8/9}$	6.6/2	kΩ/pF
Output resistance	R_{q3}	150	Ω
Output resistance	R_{q4}	150	Ω
Residual IF (basic frequency)	$V_3; V_4$	10	mV
Video bandwidth (−3 dB)	B_{video}	6.0	MHz
Intermodulation ratio with reference to f_{FT} (1.07 MHz)	a	45	dB

1) not measured

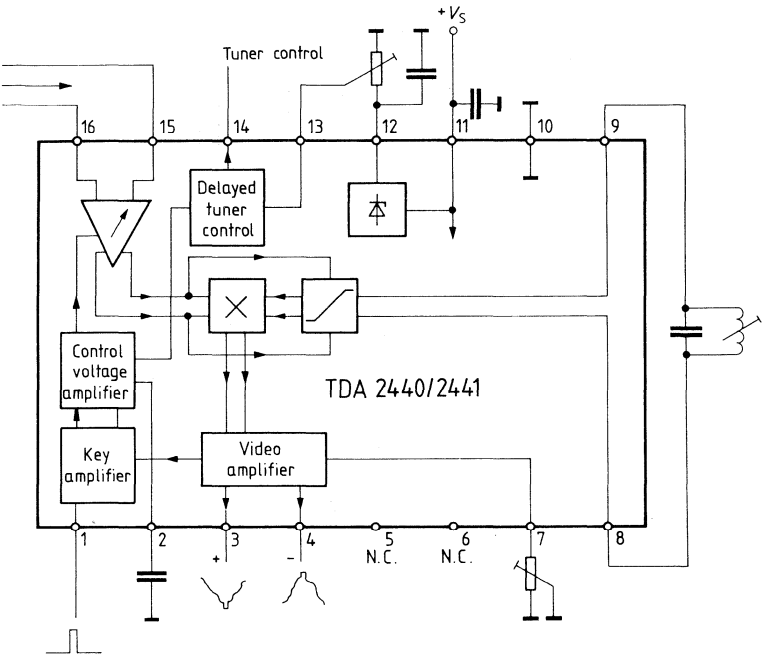
Circuit description

The integrated circuit is comprised of a 4-stage controlled AM amplifier, a limiter and mixer for synchronous demodulation of the video signals as well as an amplifier for both the positive and negative video output signal. The positive video signal as well as the positive flyback pulse are used for gated control. The delayed tuner AGC is generated by a threshold amplifier driven by the control voltage.

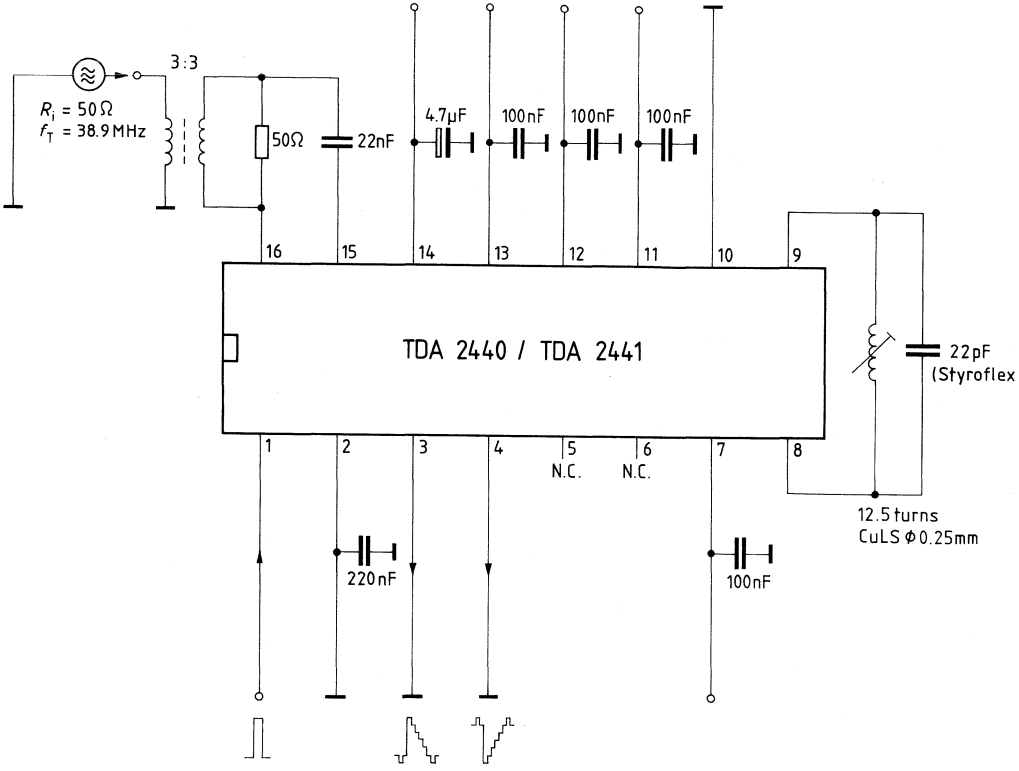
Pin configuration

Pin No.	Function
1	Gating pulse
2	Time constant AGC
3	Positive video output
4	Negative video output
5	N.C.
6	N.C.
7	White level adjustment
8	Tank circuit
9	Tank circuit
10	Ground
11	Supply voltage
12	Reference voltage
13	AGC threshold
14	Tuner control
15	Video IF input
16	Video IF input

Block diagram



Measurement circuit



Preliminary data **Bipolar circuit**

Type	Ordering code	Package outline
TDA 2842	Q67000-A2385	DIP 14

Controlled AM broadband amplifier with quadrature demodulator, sound carrier output, internal control voltage generation.

Features

- High input sensitivity
- Large control range
- Very high signal-to-noise ratio

Maximum ratings

Supply voltage range	$V_4 = V_S$	0 to 16	V
	V_2	0 to V_S	V
	I_3	−2 to 2	mA
	V_7	V_{13} to V_S	V
	V_8	V_{13} to V_S	V
	V_{11}	0 to V_S	V
	V_{12}	0 to V_S	V
	I_{13}	−2 to 2	mA
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	80	K/W

Operating range

Supply voltage range	V_S	10.5 to 15	V
IF frequency range	f_{IF}	20 to 60	MHz
Control voltage range	V_2	0 to 4	V
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics ($V_S = 12$ V; $T_{amb} = 0$ to 70 °C)

		min	typ	max	
Current consumption	I_4		55		mA
Input voltage at V_{max}	$V_{11\text{-}12}$			100	µA
V_3 ($V_{11/12} = 1$ mV) −3 dB					
Sound carrier output voltage	V_3	100			mV
($V_{iVC} = 1$ mV)					
($V_{iSC} = 300$ µV)					
AGC range	a		60		dB
V_3 ($V_{11/12} = 1$ mV) ±3 dB					
Reference voltage	V_{13}		6		V
Signal-to-noise voltage*)					
White/staircase signal	a_{white}		61		dB
DIN 45405					
Peak weighting					
Black picture	a_{black}		66		dB
DIN 45405					
Peak weighting					

***) Test conditions**

Video carrier/sound carrier	$a_{VC\text{-}SC}$		10		dB
Modulation frequency	f_{mod}		1		kHz
Frequency deviation	Δf		50		kHz
IF input voltage	V_{iIF}		20		mV

Recommended operating conditions

Input impedance	$Z_{11\text{-}12}$		1.8/2		kΩ/pF
Output impedance	$Z_{3\text{-}4}$		6.6/2		kΩ/pF
Output resistance	R_3		400		Ω
IF control voltage					
V_{max}	$V_{1/2}$	0			V
V_{min}	$V_{1/2}$			4	V

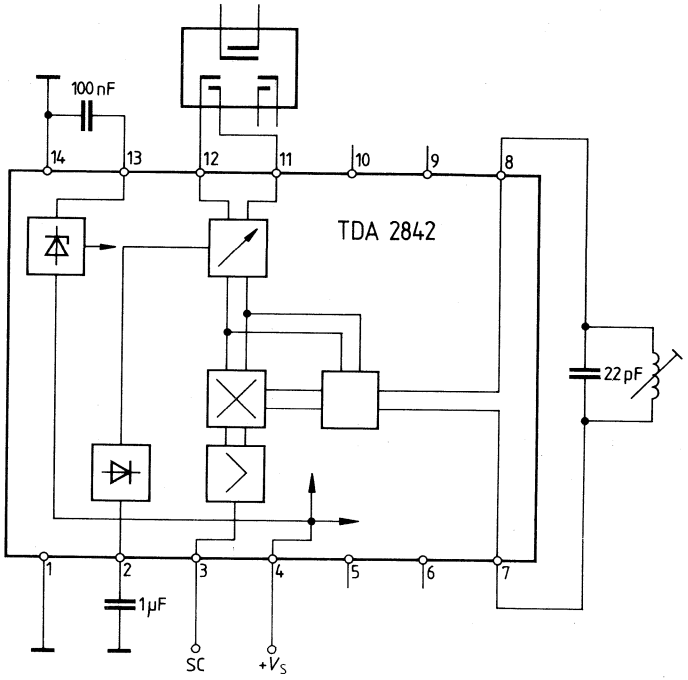
Circuit description

The TDA 2842 contains a 4-stage AM amplifier with peak rectifier with quadratic characteristic for control voltage generation. The AM amplifier drives a coincidence demodulator at the output of which the differential sound carrier (5.5 MHz; 5.74 MHz) is available. The carrier-near double sideband parts are thereby suppressed.

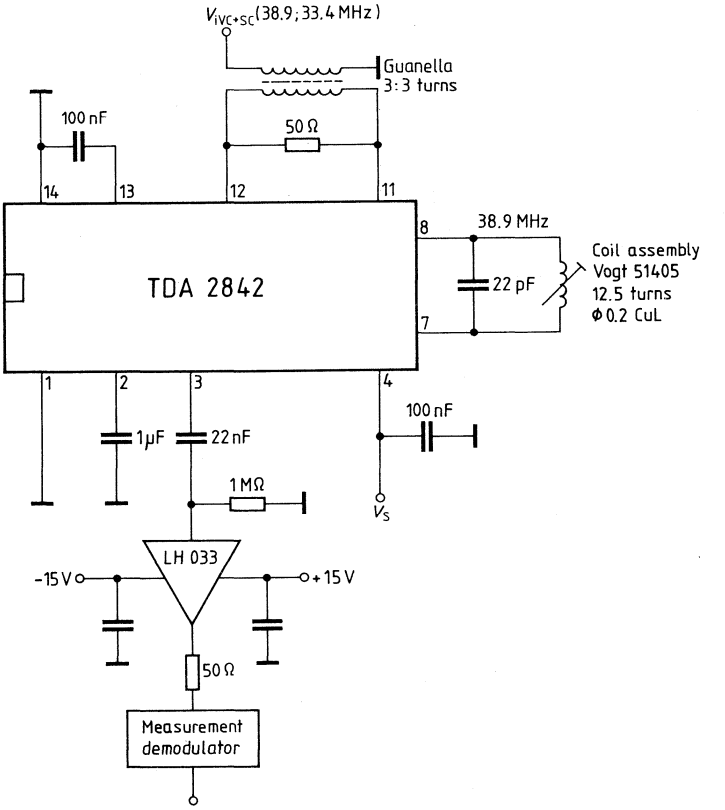
Pin configuration

Pin No.	Function
1	Ground
2	Time constant AGC
3	Sound carrier output
4	Supply voltage
5	N.C.
6	N.C.
7	Tank circuit
8	Tank circuit
9	N.C.
10	N.C.
11	IF input
12	IF input
13	Reference voltage
14	Ground

Block diagram



Test and mesurement circuit



Bipolar circuit

Type	Ordering code	Package outline
TDA 4001	Q67000-A1779	DIP 18

The TDA 4001 has been designed to convert, amplify, and demodulate AM signals. In addition, the component provides a search tuning stop pulse.

Features

- Internal demodulation
- Search tuning stop signal
- Low total harmonic distortion
- Minimal IF leakage at the AF output
- 2-stage integrated low pass filter

Maximum ratings

Supply voltage	V_S	15	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resitance (system-air)	$R_{th\,SA}$	70	K/W

Operating range

Supply voltage range	V_S	7 to 15	V
Ambient temperature range	T_{amb}	−25 to 85	°C

Characteristics ($V_S = 12$ V; $T_{amb} = 25$ °C; $V_{iRF} = 1$ MV_{rms}; $R_g = 50$ Ω; $f_{iRF} = 1$ MHz; referred to measurement circuit)

		min	typ	max	
Current consumption	I_S		15		mA
AF output voltage $m = 0.8$	$V_{qAF\,rms}$		800		mV
$m = 0.3$	$V_{qAF\,rms}$		300		mV
$V_{iRF\,rms} = 15$ μV; $m = 0.8$	$V_{qAF\,rms}$	150		320	mV
20 log ($V_{qAF\,rms}$/30 mV : $V_{qAF\,rms}$/1 mV)				3	dB
Total harmonic distortion $m = 0.8$	THD			2	%
$m = 0.3$	THD			1	%
$V_{iRF\,rms} = 30$ mV; $m = 0.8$	THD			5	%
Signal-to-noise ratio					
($m = 0.3$; $V_{iRF\,rms} = 10$ μV)	$\frac{S+N}{N}$		6		dB
($m = 0.3$; $V_{iRF\,rms} = 1$ mV)	$\frac{S+N}{N}$		46		dB
Reference voltage	V_{stab}		4.8		V
Oscillator voltage	$V_{OSC\,pp}$		100		mV
Counter output voltage	$V_{qC\,pp}$		100		mV
Input impedance RF input	Z_{iRF}		10/1.5		kΩ/pF
IF amplifier	Z_{iIF}		3.3/1.5		kΩ/pF
AFC offset current without signal	I_{AFC}			±10	μA
AFC offset current in the whole control range	ΔI_{AFC}			±10	μA
AFC output current	I_{AFC}		±80		μA
($f_{iRF} = 1$ MHz ±3 kHz)					
Search tuning stop output current	I_{q13}		2		mA
Search tuning stop output voltage	V_{q13}			0.4	V
Search tuning stop output voltage					
($V_{iRF} = 0$ V)	V_{q13}	11			V
($f_{iRF} > 1$ MHz + 3 kHz)	V_{q13}	11			V
($f_{iRF} < 1$ MHz − 3 kHz)	V_{q13}	11			V

Additional data with respect to application[1])

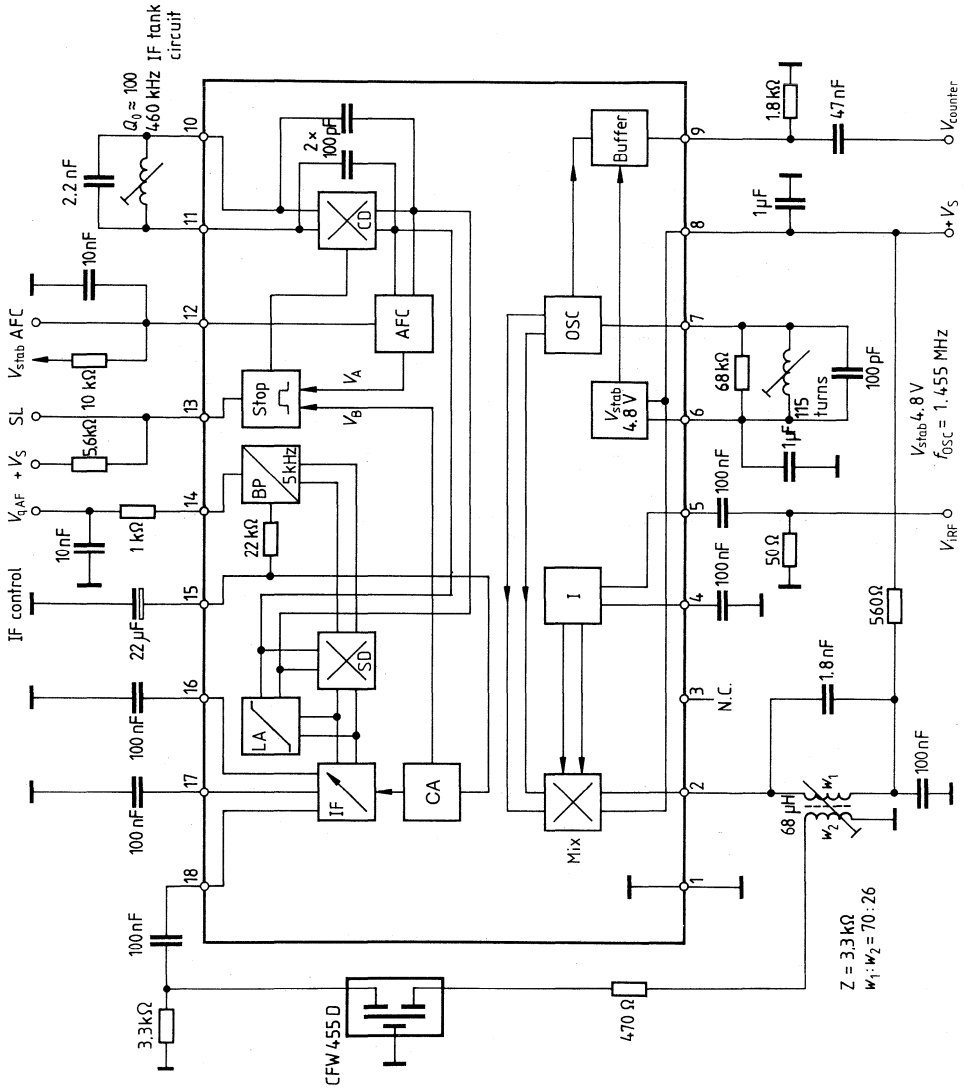
IF suppression	a_{IF}		40		dB
3 dB limit frequency of the integrated TP	f_G		5		kHz
Conversion gain	G_C		30		dB
AGC IF amplifier	$V_{iIF\,rms}$		100		μV
Control range ($\Delta V_{qAF} = 6$ dB)	a		60		dB
Input sensitivity ($V_{qAF}/V_{iRF\,rms} = 1$ mV −3 dB)	$V_{iRF\,rms}$		30		μV

Circuit description

The impedance converter forwards the input signal V_{iRF} to the symmetrical double balanced mixer. Subsequently the signal is converted to IF with the amplitude-controlled oscillator. An external filter forwards the IF signal to the controlled IF amplifier. The amplifier IF signal and the carrier signal will be converted to AF in the subsequent synchrnous demodulator (SD). The 2-stage low pass filter forwards the available AF to the AF output. Via an additional limiter amplifier (LA), the AF uses the carrier signal to control the coincidence demodulator (CD). The output signal of the coincidence demodulator provides the stop pulse during exact tuning and sufficient field strength. The stop pulse interrupts the automatic search tuning.

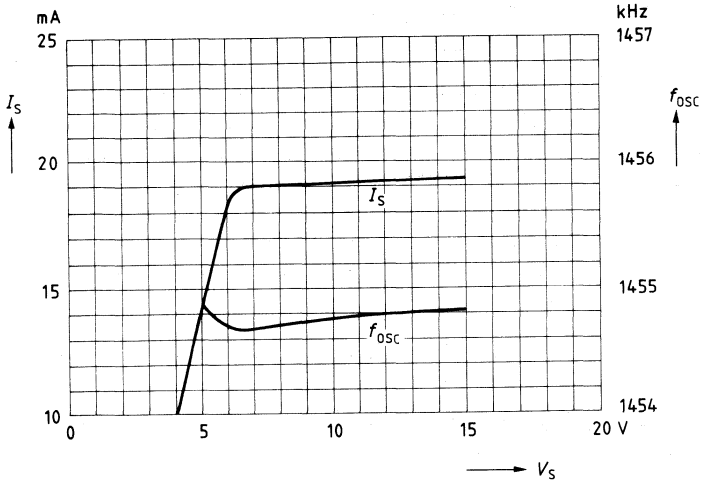
1) Data does not apply to series measurement processes.

Block diagram and measurement circuit



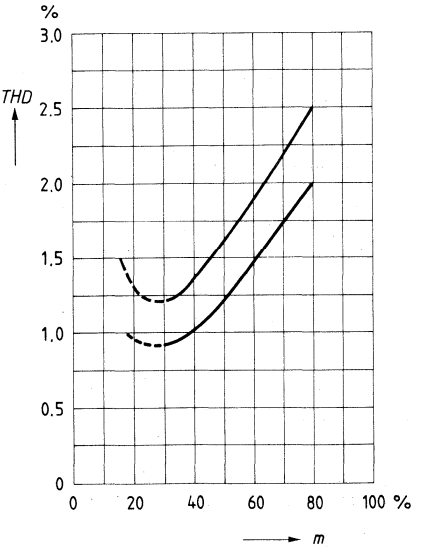
CA = Control amplifier
LA = Limiting amplifier
BP = Band pass
CD = Coincidence demodulator
I = Impedance converter

Oscillator frequency versus current consumption

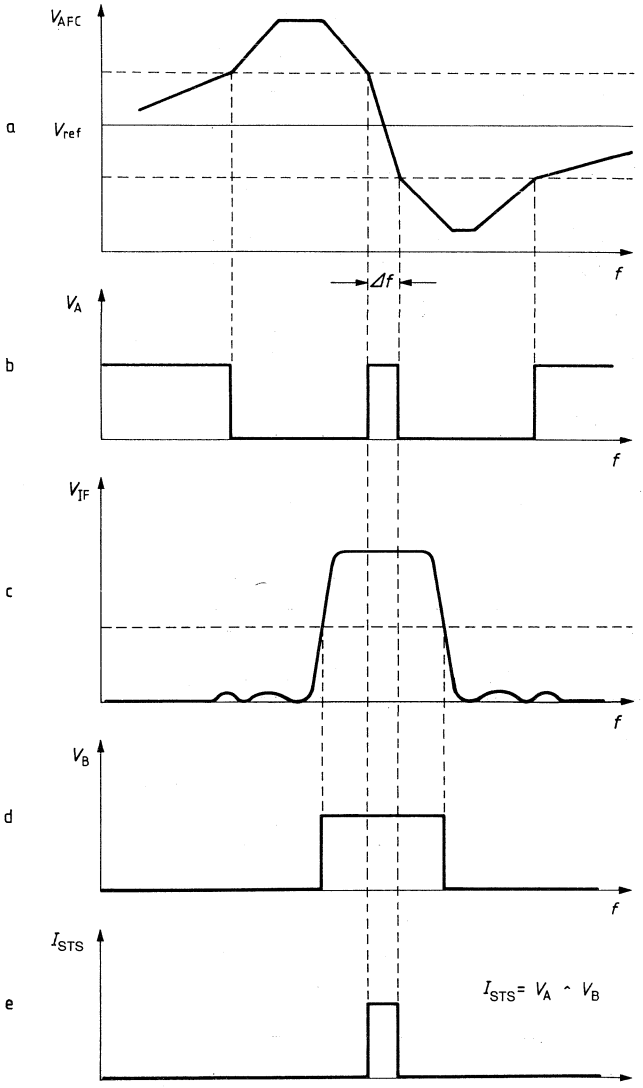


Total harmonic distortion versus modulation factor

$V_S = 15$ V; $f_{mod} = 1$ kHz; $V_i = 1$ mV



Derivation of the AM-SL stop criterion



S curve simulation (pin 12)

--- Comparator threshold A

Δf = Stop bandwidth

V_A = Output voltage, window discriminator A

IF selection (e. g. CFW 455)

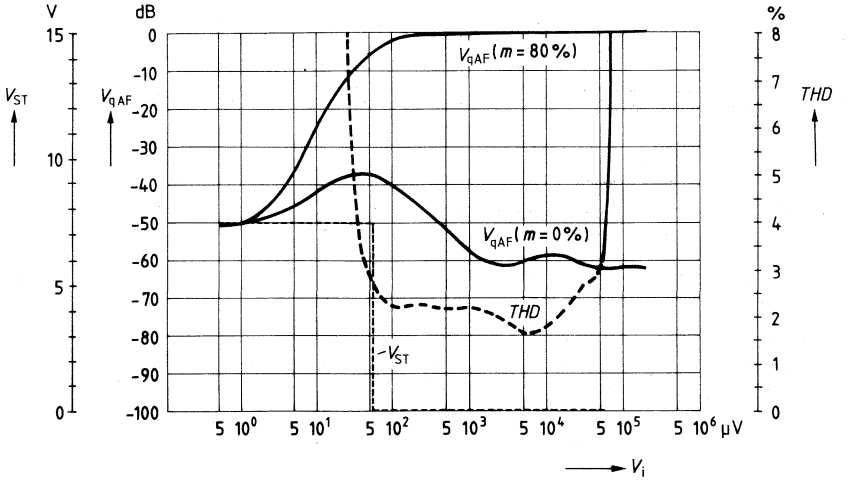
--- Comparator threshold B

V_B = Output voltage, window discriminator B

Search tuning stop pulse (pin 13)

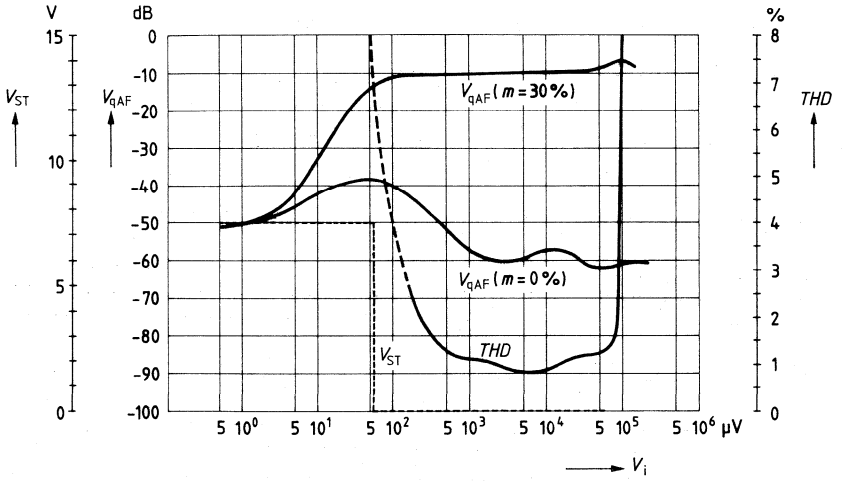
AF output voltage, total harmonic distortion, search tuning stop versus input voltage
$V_S = 15$ V, $f_{mod} = 1$ kHz, $f_i = 1$ MHz

0dB ≙ 775 mV (rms)

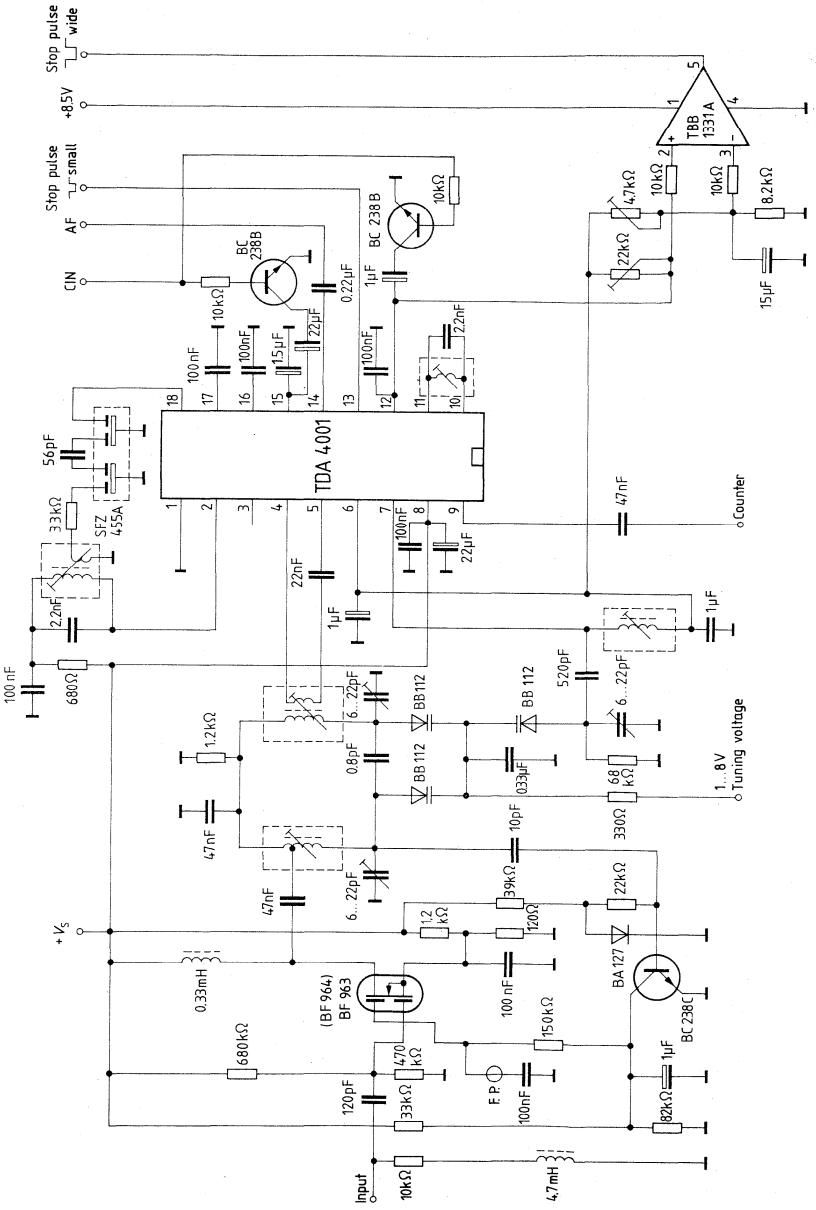


AF output voltage, total harmonic distortion, search tuning stop versus input voltage
$V_S = 15$ V; $f_{mod} = 1$ kHz, $f = 1$ MHz

0dB ≙ 775 mV (rms)



Application circuit



Bipolar circuit

Type	Ordering code	Package outline
TDA 4050 B	Q67000-A1373	DIP 8

The IC TDA 4050 B is suitable for use as infrared preamplifier in remote control facilities for radio and TV sets.

The IC includes a controlled driver stage with subsequent amplifier stage as well as an amplifier for the threshold value. The circuit is largely balanced.

Features

- Internal AGC
- Superior large signal stability
- Short-circuit proof signal output
- Simple connection for an active band filter
- Few external components

Maximum ratings

Supply voltage	V_S	16[1])	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	140	K/W

Operating range

Supply voltage range	V_S	9 to 16	V
Ambient temperature range	T_{amb}	0 to 70	°C
Input frequency range	f_i	0 to 100	kHz

1) intermittently 17.5 V

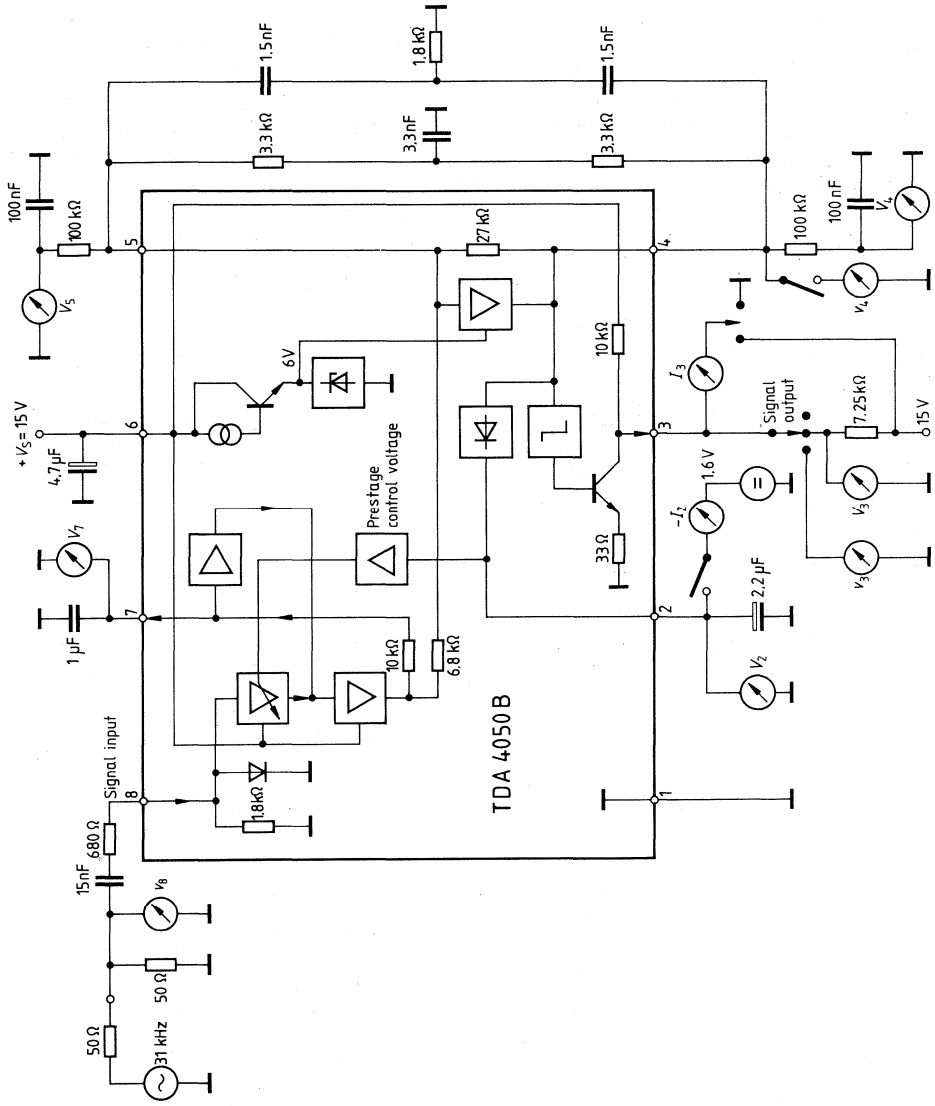
Characteristics ($V_S = 15$ V; $T_{amb} = 25$ °C; $f_{IR} = 31$ kHz) referred to measurement circuit

		min	typ	max	
Current consumption ($R_L \geqq 10$ kΩ)	I_6	6	9	12	mA
Input voltage for control start	$v_{8\,rms}$		50		μV
Input voltage for output signal	$v_{8\,rms}$			85	μV
Filter output voltage (in control range)	$v_{4\,rms}$	350	450	550	mV
Gain	$G_{4/8}$	74	77	85	dB
Gain	$G_{3/4}$		21		dB
Total control range	ΔG	74	77	85	dB
Control voltage without input signal	V_2	1325	1425	1525	mV
Control voltage ($v_{8\,rms} = 100$ μV)	V_2	1.5		2.1	mV
Control voltage ($v_{8\,rms} = 10$ mV)	V_2	1.9		2.45	V
Control voltage ($v_{8\,rms} = 1$ V)	V_2	2.1		2.6	V
Operating points	$V_{4/5/7}$	2.2		2.8	V
Output current ($V_3 = V_S$)	I_3		20		mA
Output dc voltage for L level	V_{3L}		150	500	mV
Output dc voltage for H level	V_{3H}	14.6			V
Charge current ($v_{8\,rms} = 100$ mV; $V_2 = 1.6$ V)	$-I_2$	0.4		1.0	mA
Discharge current ($v_{8\,rms}$ from 1 mV to 0) ($T = 50$ ms)	I_2	0.4		3.0	μA
Input resistance	R_{i8}		1.8		kΩ
Output resistance	R_{q3}		10		kΩ
Rated resistance of the double-T network at pin 4 (unbalanced to ground)	R_4	2			kΩ

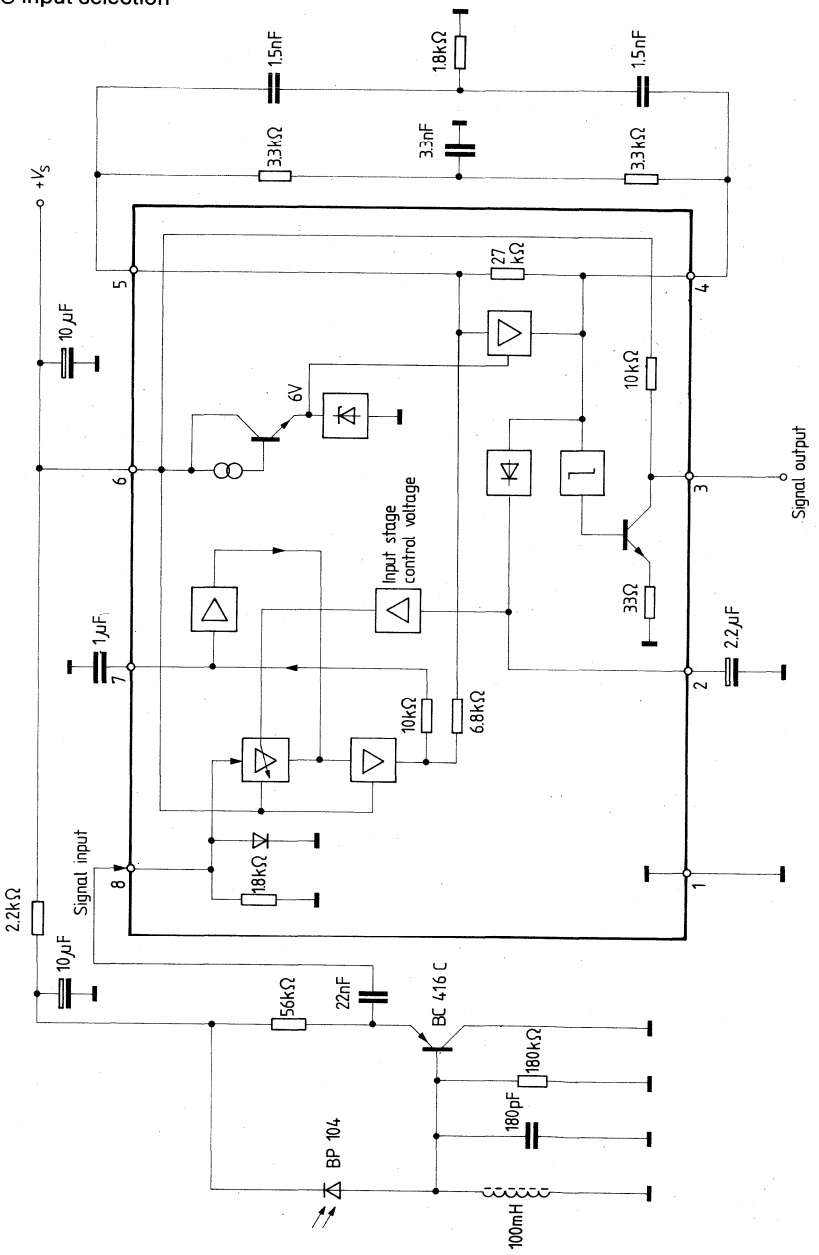
Pin configuration

Pin No.	Function
1	Ground
2	Connection for capacitance for prestage control
3	Output threshold amplifier
4	Output active filter
5	Input active filter
6	Supply voltage, positive
7	Unlocking of operating point control
8	Signal input

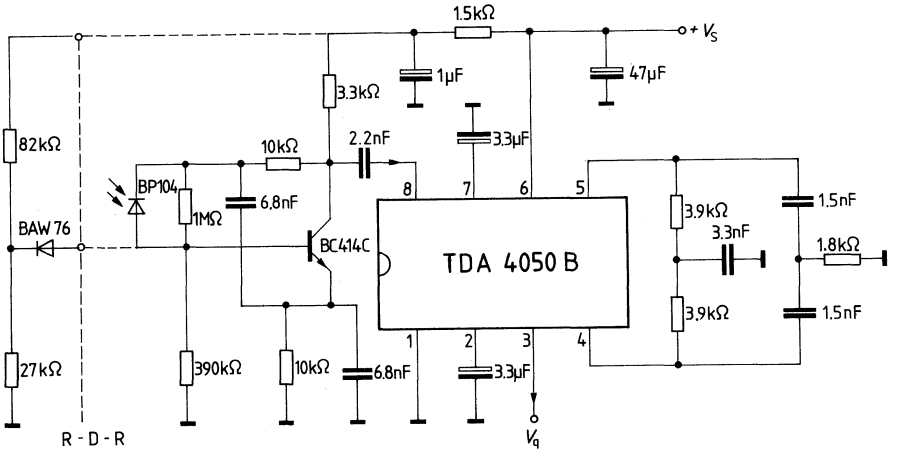
Measurement circuit and block diagram



Application circuit I
incl. *LC* input selection



Application circuit II
without coil



Notes

Circuit I uses an LC resonant circuit and is of superior quality due to its high selectivity feature (approx. 3 kHz bandwidth at −3 dB).

Circuit 2 offers the lower cost solution without coil incl. broadband input selection. Higher requirements as to steady radiation and large signal stability can be met by means of resistor-diode-resistor connection (RDR).

Bipolar circuit

Type	Ordering code	Package outline
TDA 4100	Q67000-A1443	DIP 22

As an AM-FM combination, the integrated circuit TDA 4100 has been primarily designed for the use in portable radio sets.

Features

- Low current consumption
- Optional low voltage supply (> 4 V)
- Few external components
- Optimal AF processing with AM

Maximum ratings

Supply voltage AM section	V_{SAM}	16.5	V
Supply voltage FM section	V_{SFM}	16.5	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	R_{thSA}	70	K/W

Operating range

Supply voltage range AM section	V_{SAM}	4.5 to 15	V
Supply voltage range FM section	V_{SFM}	4.5 to 15	V
Oscillator frequency range	f_{OSC}	0.5 to 30	MHz
Input frequency range AM RF section	f_{iAM}	0.1 to 30	MHz
Input frequency range AM IF section	f_{IFAM}	0.2 to 0.7	MHz
Input frequency range FM IF section	f_{IFFM}	0 to 15	MHz
Ambient temperature range	T_{amb}	−20 to 80	°C

Characteristics ($V_S = 10$ V; $T_{amb} = 25$ °C)

		min	typ	max	
AM section ($f_{iRF} = 1$ MHz; $f_{mod} = 1$ kHz)					
Current consumption	I_{AM}		12		mA
AF output voltage $m = 0.8\%$	V_{qAFrms}	110	160	210	mV
($V_{RFrms} = 3$ mV)	THD		1.8		%
AF output voltage $m = 0.3\%$	V_{qAFrms}		60		mV
($V_{RFrms} = 3$ mV)			1		%
AF output voltage $m = 0.12\%$	V_{qAFrms}		25		mV
($V_{RFrms} = 3$ mV)	THD		0.4		%
AGC range ($\Delta AF = 6$ dB)	ΔG	64	70		dB
Signal-to-noise ratio $m = 0.3\%$					
at 1 μV_{rms}	$\frac{S+N}{N}$		6		dB
at 15 μV_{rms}	$\frac{S+N}{N}$		26		dB
at 1 mV_{rms}	$\frac{S+N}{N}$	38	40		dB
Instrument voltage ($V_{iRFrms} = 150$ mV)	$V_{instr.}$		2.5		V
Reference voltage	V_{ref}		2.7		V
Oscillator voltage ($f_{OSC} = 1$ MHz)	V_{OSCpp}		300		mV
Counter output voltage	V_{qcpp}		300		mV
Quiescent current/counter output	I_3		100		µA
IF suppression	a_{IF}		30		dB
Input impedance prestage	Z_{iAM}	1.6/1	2.2/1.5	2.8/3	kΩ/pF
Input impedance IF	Z_{iIF}	2.4	3.3	4.2	kΩ
AGC threshold	V_{irms}		20		µV
FM section ($f_{iIF} = 10.7$ MHz; $f_{mod} = 1$ kHz)					
Current consumption	I_{FM}		10	19	mA
AF output voltage	V_{qAFrms}	20	30	50	mV
($\Delta f = \pm 5$ kHz; $V_{iIFrms} = 1$ mV)					
DC portion					
(AFC = 0; $V_{iIFrms} = 1$ mV)	V_{qdc}	1.0	1.5	2.2	V
Instrument voltage	V_i		0	0.1	V
($V_{iIF} = 0$ mV)					
Instrument voltage	V_i	1.5	2.5	2.8	V
($V_{iIF} = 100$ mV)					
Total harmonic distortion					
($V_{iIFrms} = 1$ mV; $\Delta f = \pm 12$ kHz)	THD		0.3	0.6	%
Total harmonic distortion					
($V_{iIFrms} = 1$ mV; $\Delta f = \pm 75$ kHz)	THD		1.0		%
Input limiting voltage	V_{iIFrms}		30	50	µV
Input impedance	Z_{iIF}	5/5			kΩ/pF
Reference voltage	V_{stab}	1.8	2.4		V
AFC current deviation	I_{AFC}		±150	±200	µA

Additional data with respect to application[1])

		min	type	max	
General					
Current carrying capability of V_{REF}	I_{22}			2.0	mA
Min. ext. load resistance at the tuning meter output	$R_{15\,ext.}$	3			kΩ
Temperature variation of the reference voltage	TC_{22}		+0.3		mV/K
AM section					
Matching noise			500		Ω
Control range IF			40		dB
Control range prestage			30		dB
AGC prestage (rms)			1		mV
AGC IF (rms)			100		µV
Large signal stability ($V_{iRF\,rms} = 150$ mV); $m = 0.8\%$			10		%
Max. ext. load at counter output	$I_{3\,ext.}$			2.0	mA
FM section					
Signal-to-noise ratio ($V_{iIF} = 20$ µV)	$\frac{S+N}{N}$			26	dB

1) Data does not apply to series measurement procedure

Circuit description

The AM section of the TDA 4100 includes a controlled prestage and an IF amplifier, a mixer, a two-point oscillator operable up to 30 MHz, as well as a demodulator and a 3-stage active low-pass filter (3 dB point = 5 kHz). In addition, technical provisions have been made to connect a field-strength indicator and to add additional filters in the AF path.

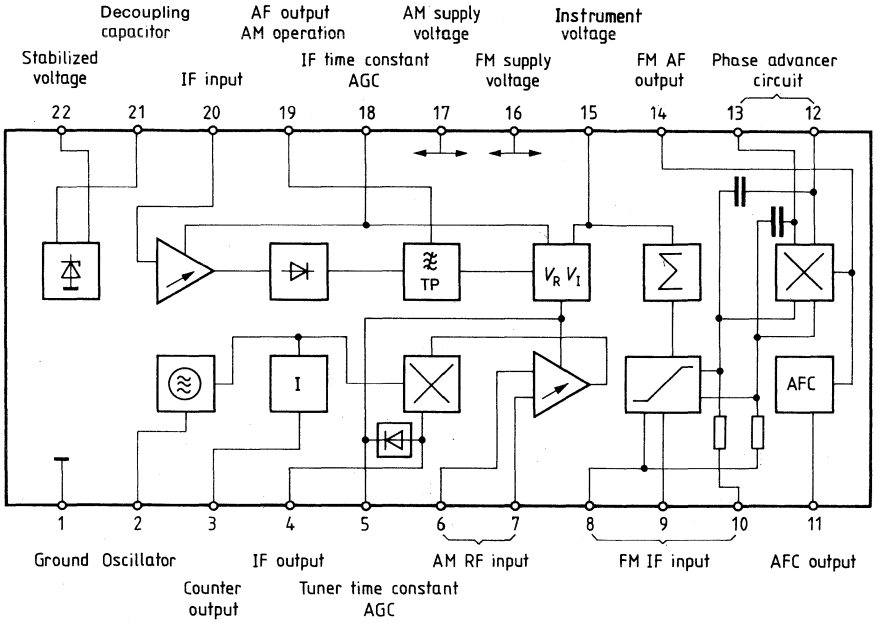
The FM section, on the other hand, includes a symmetrical 6-stage amplifier with a symmetrical quadrature detector to limit, demodulate, and amplify FM signals. In addition, the FM section has been designed to include an AFC output and to provide a connection for the field-strength indicator.

The TDA 4100 is equipped with separate AM and FM inputs as well as separate outputs for the AF voltages. However, collective outputs have been provided for the instrument and reference voltages.

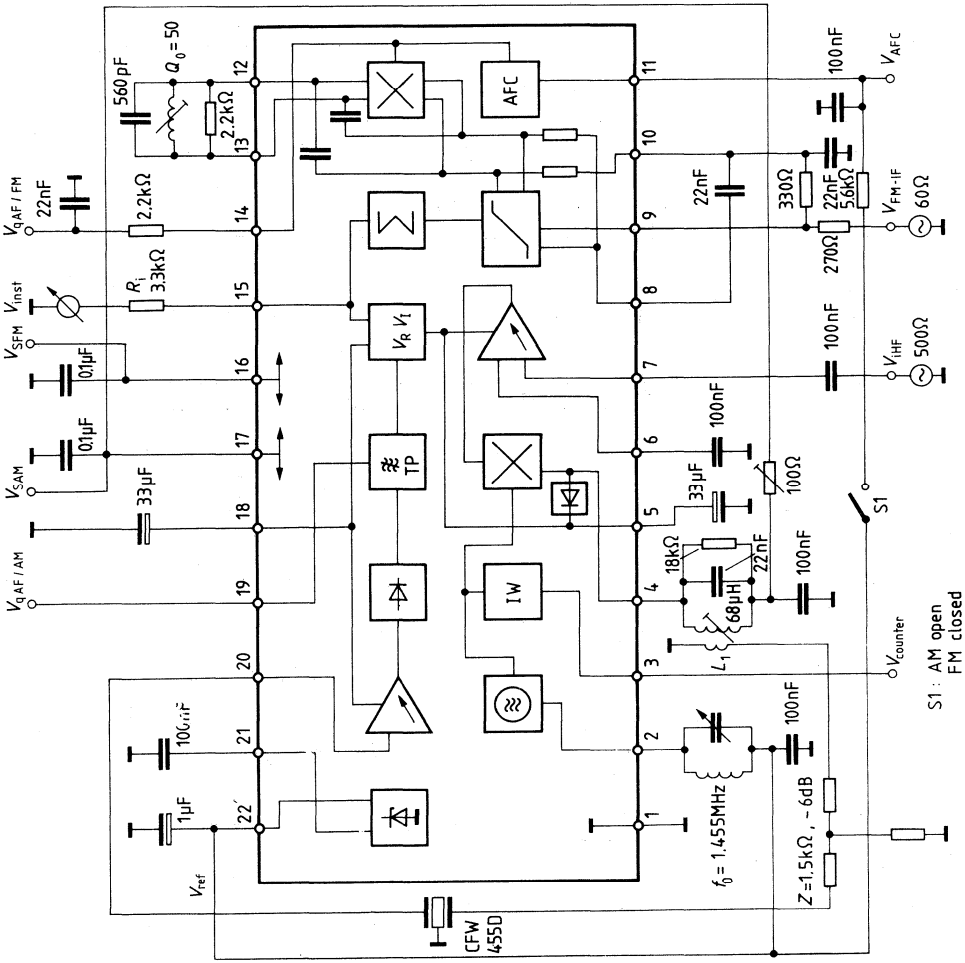
Pin configuration

Pin No.	Function
1	Ground
2	Oscillator circuitry
3	Counter output
4	IF output
5	Tuner time constant AGC
6	AM RF input I
7	AM RF input II
8	Decoupling capacitor
9	FM IF input
10	Decoupling capacitor
11	AFC output at FM operation
12	Phase advancer circuit
13	Phase advancer circuit
14	AF output at FM operation
15	Instrument output
16	FM supply voltage
17	AM supply voltage
18	IF time constant AGC
19	AF output at AM operation
20	AM IF input
21	Decoupling capacitor
22	Stabilized voltage

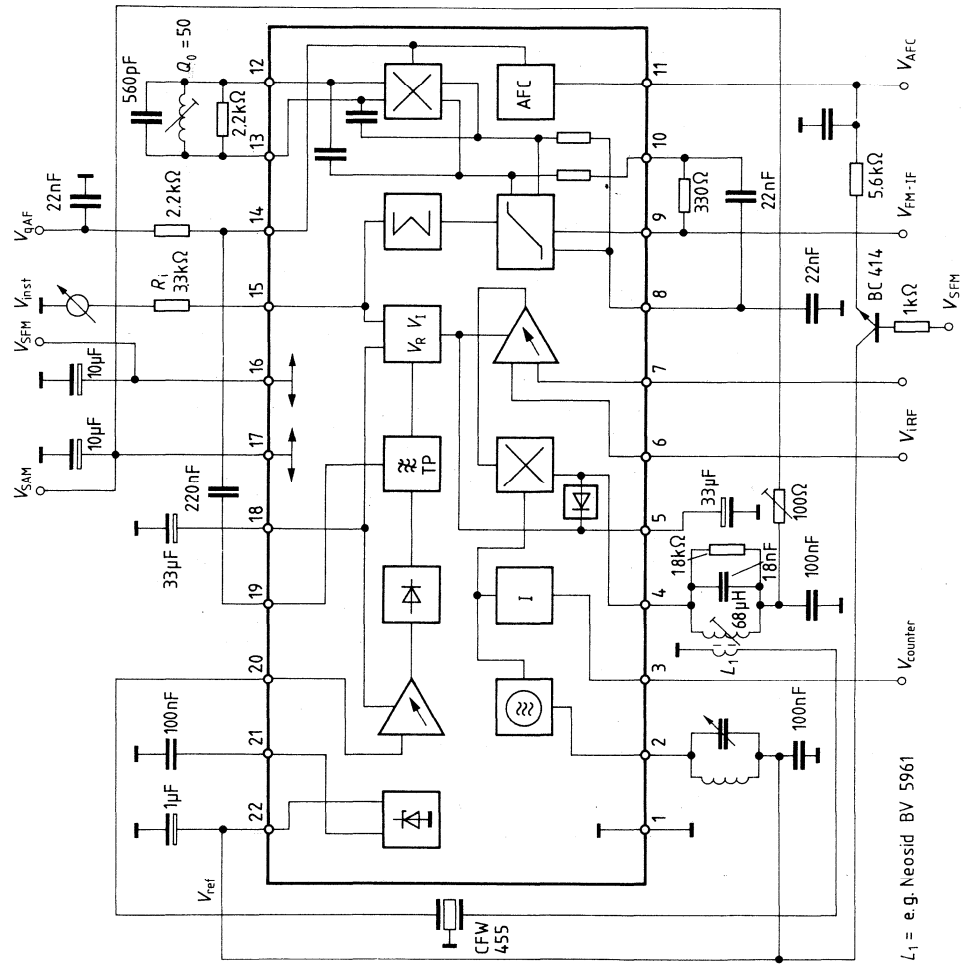
Block diagram



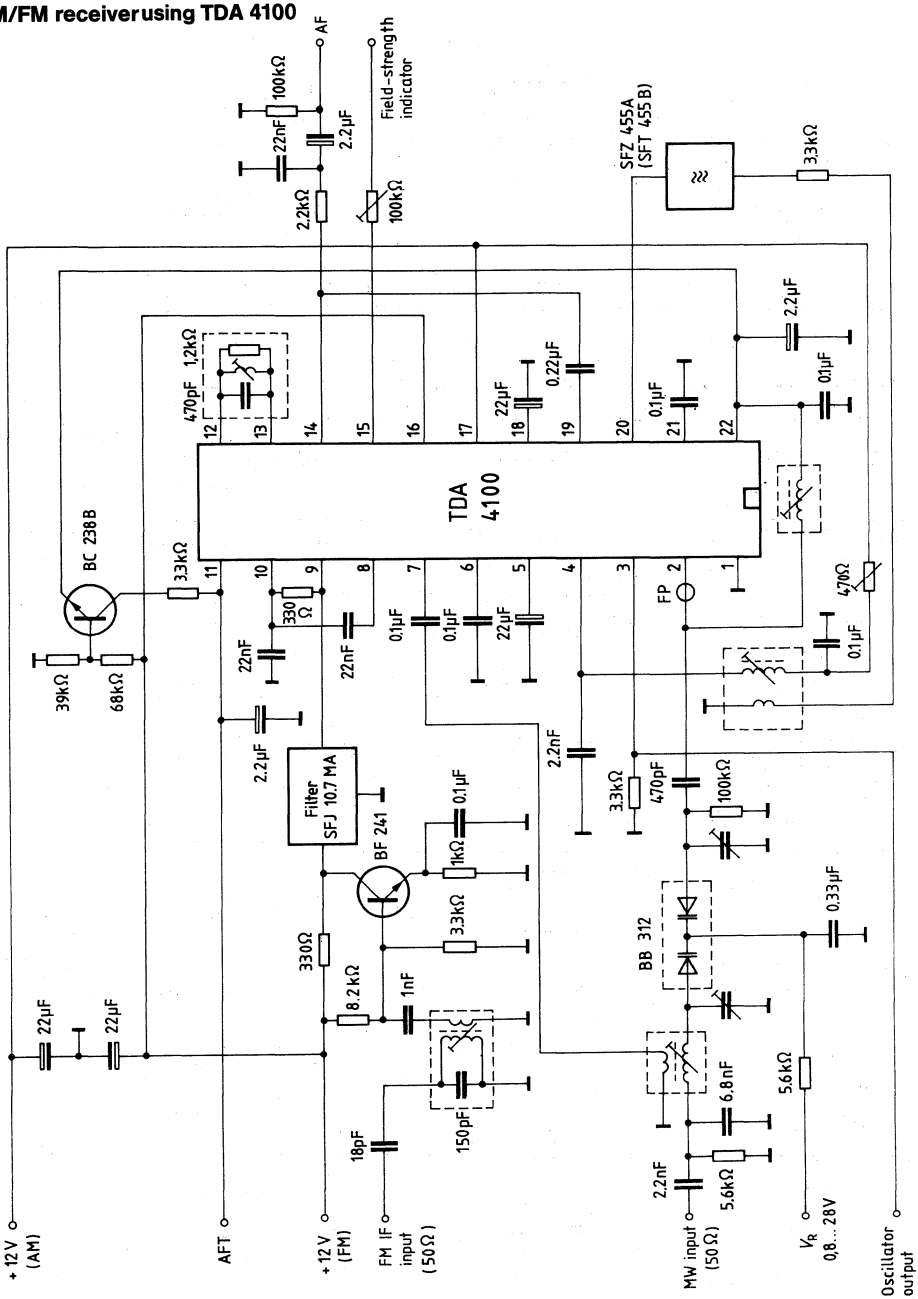
Test and measurement circuit



Application circuit



AM/FM receiver using TDA 4100



Bipolar circuit

Type	Ordering code	Package outline
TDA 4200-2	Q67000-A1469-E11	DIP 18

As an FM IF component with demodulator, the TDA 4200-2 is especially designed for application in car radios. The integrated circuit facilitates automatic search tuning, including a search tuning stop pulse. In addition, the input sensitivity of the RF preamplifier is externally adjustable.

Features

- 7-stage limiter amplifier
- Product demodulator
- AFC output
- Field-strength dependent volume control

Maximum ratings

Supply voltage	V_S	18	V
Output current	I_{q6}	0.5	mA
Invert. field strength output current	I_{q11}	5	mA
Field strength output current	I_{q12}	5	mA
	V_{q13}	V_S	
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	70	K/W

Operating range

Supply voltage range	V_S	7.5 to 15	V
Frequency			
IF section, demodulator	f_{IF}	0.4 to 15	MHz
overall frequency range	f	5 to 15	MHz
AF ($V_q = -1$ dB)	f_{AF}	0.02 to 150	kHz
Ambient temperature range	T_{amb}	−25 to 85	°C

Characteristics ($V_S = 8.5$ V; $V_{i\,rms} = 10$ mV; $f_i = 10.7$ MHz; $\Delta f = \pm 75$ kHz; $f_{mod} = 1$ kHz; Q_B approx. 20; $T_{amb} = 25$ °C)

		min	typ	max	
Current consumption	I_{14}		24	29	mA
Field strength output voltage					
($V_{i\,rms} = 50$ mV)	V_{12}	3.0	3.8		V
($V_{i\,rms} = 0$)	V_{12}		0	0.1	V
Inverse field strength output voltage					
($V_{i\,rms} = 5$ mV)	V_{11}		0.8	1.5	V
($V_{i\,rms} = 0$)	V_{11}	3.5	4	4.5	V
AF-output voltage	$V_{q\,5\,rms}$	270	350		mV
Total harmonic distortion with FM-IF operation (pin 13 open; $I_{AFC} = 0$)	THD		0.7	1.5	%
Input voltage for limiting start ($V_{q\,5}$ −3 dB)	$V_{i\,IF\,rms}$		15	25	µV
AM suppression ($m = 30\%$)	a_{AM}	60			dB
Signal-to-noise ratio	$a_{S/N}$	70			dB
Current deviation of the AFC output ($f = \pm 50$ kHz; $\Delta f = 0$)	ΔI_7		±90		µA
AFC offset ($V_i = 20$ µV...10 mV)	f_{off}			±15	kHz
Search tuning stop window ($R_{7/8} = 22$ kΩ)	f_{ST}		±18		kHz
Search tuning stop signal threshold ($V_6 < 1$ V)	$V_{i\,ST}$	10	35	70	µV
Search tuning stop signal output ($I_6 = 500$ µA) Pin 6 47 kΩ at 8.5 V	V_6			500	mV
Stabilized voltage	V_8	3.6	4.1	4.6	V
Adjustable range of limiting start through pin 15	$V_{i\,IF}$	36	44	50	dB
Limiting start at $V_{15} = V_{8/2}$	$V_{i\,IF}$		500		µV
AF mute $V_{2/1} = 0$; $R_{4/1} = \infty$	a_{AF}	4	7	10	dB
$V_{2/1} = 0$; $R_{4/1} = 0$	a_{AF}	32	39	46	dB
AF mute switch-off voltage	$V_{2/1}$	0.75	0.5		V
AF output voltage for $V_{i\,3\,rms} = 200$ mV	$V_{q\,rms}$	250	350	400	mV
Total harmonic distortion ($V_{i\,3\,rms} = 500$ mV)	THD			1	%

Additional data with respect to application[1)]

DC voltage AF output	$V_{q\,5}$	2.8	3.8	4.8	V
Internal DC current of the emitter follower output	I_5	0.75	1		mA
Input resistance for demodulator circuitry	$R_{9\text{-}19}$	22	30		kΩ
Input resistance	$R_{i\,3}$	75	100	125	kΩ

1) Data does not apply to series measurement process.

Pin configuration

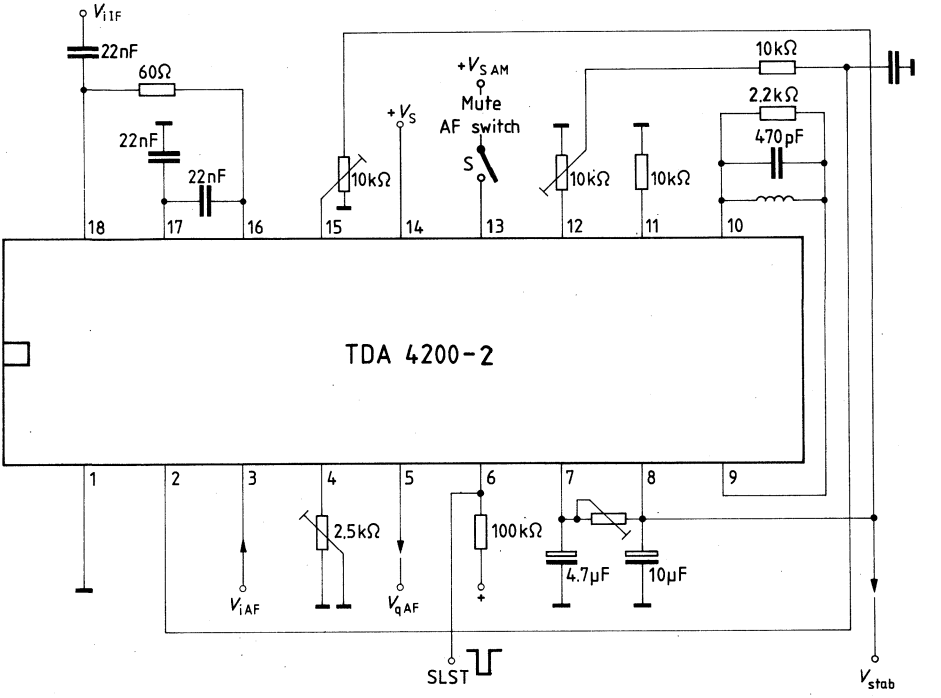
Pin No.	Function
1	Ground
2	Audio control
3	Audio input
4	Audio control range adjustment
5	Audio output
6	Search tuning stop pulse
7	AFC output
8	Stabilized voltage
9	Tank circuit
10	Tank circuit
11	Inverted field strength output
12	Field strength output
13	Mute AF switch
14	Battery voltage $+V_S$
15	Limiter threshold adjustment
16	Operating point feedback
17	Operating point feedback
18	IF input

Circuit description

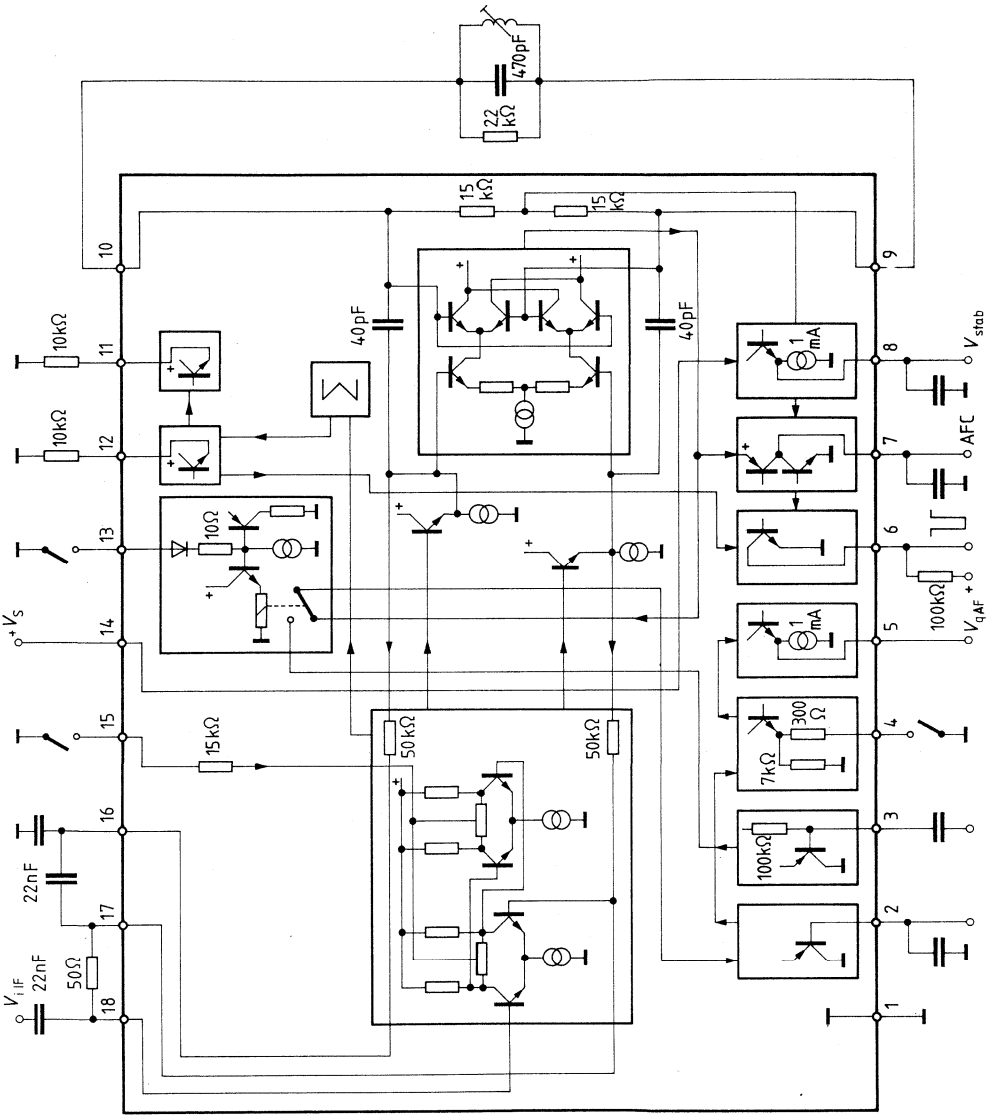
The integrated circuit includes a 7-stage limiter amplifier with demodulator and an uncontrolled AF output. By means of external circuitry the limiter threshold can be varied by 40 dB. Within this range, the AF output signal can be continuously attenuated by max. 39 dB. Therefore, increasing noise levels are avoided during strong field strength variations. Also included are a field strength output, an inverted field strength output, an AFC output as well as an open collector output. The latter will be activated at zero crossing of the detector S-curve.

When applying the integrated circuit in combined AM/FM configurations, it is possible to supply pin 3 with the AM-AF signal and forward it via the muting stage to audio output pin 5. During the process, the muting circuitry will be connected to $V_{S\,AM}$ through an external switch S, which simultaneously cancels the mute function.

Test circuit



Block diagram



Bipolar circuit

Type	Ordering code	Package outline
TDA 4260	Q67000-A1300	DIP 8

Symmetrical, single-stage limiter amplifier with symmetrical coincidence demodulator and symmetrical AFC amplifier including a push-pull current output. Particularly suitable for automatic tuning in TV sets.

Features

- Good limiting characteristics
- Excellent frequency stability of the converter characteristic
- Few external components
- Programmable current deviation

Maximum ratings

Supply voltage	V_S	15[1])	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	100	K/W

Operating range

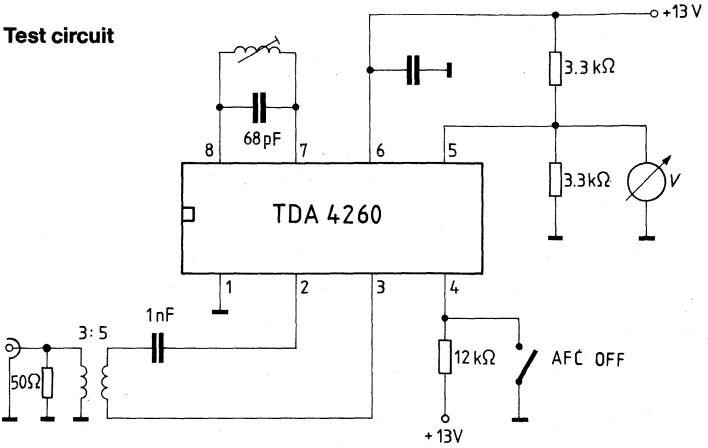
Supply voltage range	V_S	10.5 to 15	V
Ambient temperature range	T_{amb}	−25 to 60	°C

Characteristics ($V_S = 13$ V; $T_{amb} = 25$ °C)

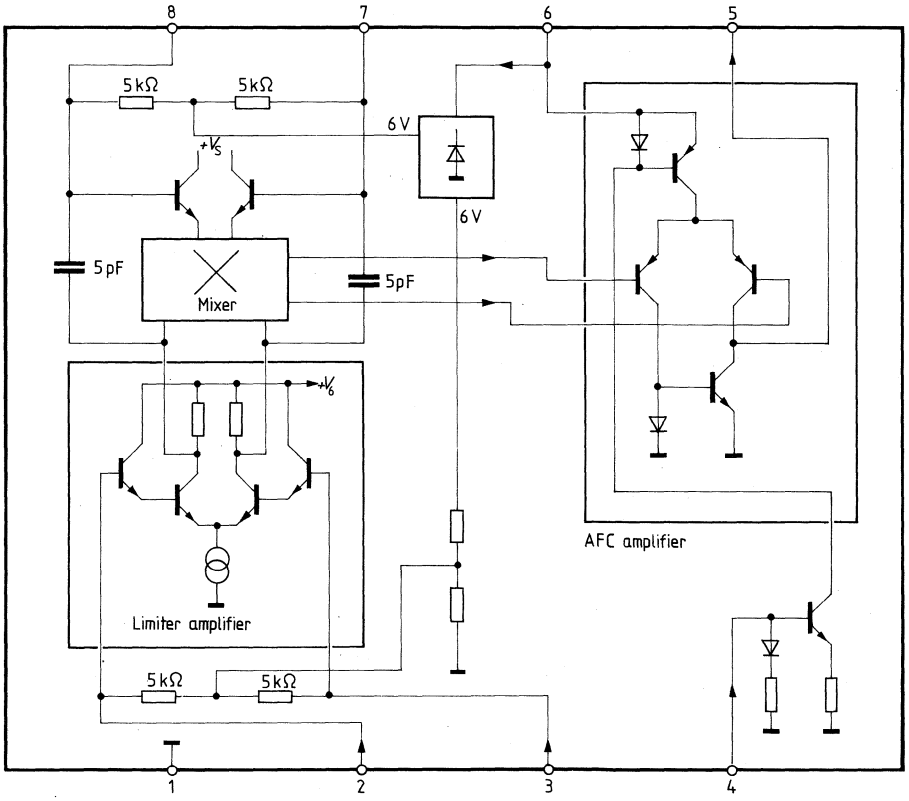
		min	type	max	
Current consumption	I_6	13	18	23	mA
Limiting use	$V_{2/3\,rms\,lim}$		60	80	mV
Input resistance	$R_{i\,2/3}$		10		kΩ
Programming current	I_4			1	mA
Output current (at $I_4 = 1$ mA)	$I_{q\,5}$	±600	±750	±900	µA
Output current: without signal	$I_{q\,5}$		0	±10% · I_4	µA
Output current for AFC OFF ($I_4 = 0$)	$I_{q\,5}$		0	±10	µA

1) intermittently 16.5 V

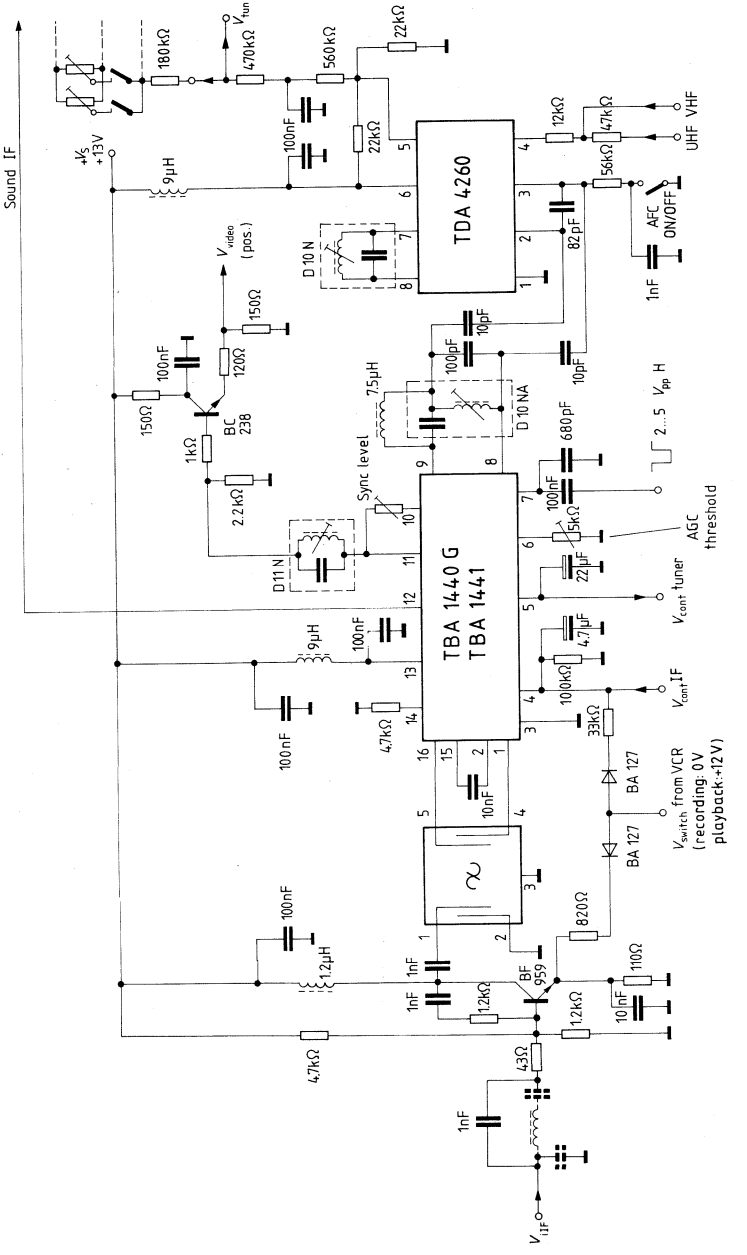
Test circuit



Block diagram



Application circuit



Preliminary data **Bipolar circuit**

Type	Ordering code	Package outline
TDA 4283 T	Q67000-A2388	DIP 22

The TDA 4283 T is a controlled AM broadband amplifier with FM demodulator (to produce the intercarrier) and subsequent sound IF limiter amplifier with coincidence demodulator, standard VCR connection and separate AF output.

Features

- High input sensitivity
- Large control range
- Very high signal-to-noise ratio
- Two intercarrier outputs
- VCR connection

Maximum ratings

Supply voltage range	$V_5 = V_S$	0 to 16	V
	V_2	0 to V_S	V
	V_3	V_{22} to V_S	V
	V_4	V_{22} to V_S	V
	I_6	−2 to 2	mA
	I_7	−2 to 2	mA
	V_8	0 to 6	V
	V_9	0 to 6	V
	V_{10}	0 to 6	V
	I_{11}	−2 to 2	mA
	I_{12}	−2 to 2	mA
	I_{13}	−1 to 1	mA
	I_{14}	−1 to 1	mA
	V_{15}	0 to V_S	V
	V_{16}	0 to V_S	V
	V_{17}	0 to V_S	V
	V_{18}	0 to V_S	V
	V_{20}	0 to V_S	V
	V_{21}	0 to V_S	V
	I_{22}	−2 to 2	mA
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	60	K/W

Operating range

AM/FM amplifier/supply voltage	V_5	10.5 to 15	V
Frequency range AM IF section	f_{AM}	20 to 60	MHz
Frequency range FM IF section	f_{FM}	0.01 to 12	MHz
Control voltage range AM IF section	V_2	0 to 4	V
Switching current range FM IF section	I_8	0.3 to 1	mA
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics ($V_S = 12$ V; $T_{amb} = 25$ °C)

		min	typ	max	
Current consumption	I_5		75		mA
Reference voltage	V_{22}		6		V
AM section:					
Input voltage at V_{max} $V_{6,7}$ ($V_{18/19} = 1$ mV) −3 dB	$V_{18\text{-}19}$			100	µV
Sound carrier output voltage ($V_{iVC} = 1$ mV) ($V_{iSC} = 300$ µV)	$V_{6,7}$	100			mV
AGC range $V_{6,7}$ ($V_{18/19} = 1$ mV) ±3 dB	a_{AGC}		60		dB
Signal-to-noise-ratio*) White/staircase signal DIN 45505 peak weighting	a_{white}		61		dB
Black picture DIN 45505 Peak weighting	a_{black}		66		dB
FM section:					
Input voltage for limiting $f_{IF} = 5.5$ MHz; $f = 30$ kHz	V_{i10}			60	µV
AF output voltage $V_{iIF} = 10$ mV; $f_{IF} = 5.5$ MHz $f = \pm 12.5$ kHz; $f_m = 1$ kHz; $Q_B \approx 28$	V_{11}	260	300		mV
VCR output voltage	V_{12}		500		mV
AF gain VCR playback	$G_{12\text{-}11}$		0.6		
AM suppression ($V_{iIF} = 1$ mV; $f_{IF} = 5.5$ MHz $f_m = 1$ kHz; $m = 30\%$)	a_{AM}		42		dB
Signal-to-noise ratio*)	$a_{S/N}$		85		dB
Total harmonic distortion AF output $f = 12.5$ kHz, $f_m = 1$ kHz	*THD*		1		%

*) For test conditions refer to page 441

Characteristics ($V_S = 12$ V; $T_{amb} = 25$ °C)

		min	typ	max	
Cross talk attenuation					
($V_{iIF} = 10$ mV; $V_{12\,rms} = 2$ V)	$a_{12\text{-}11}$	50	52		dB
($V_{iIF} = 10$ mV; $V_{12\,rms} = 0.3$ V)	$a_{12\text{-}11}$	60	65		dB
Range of volume control	$V_{AF\,max}/V_{AF\,min}$	70	85		dB
($V_{18} \geqq 4.8$ V / $V_{18} = 0$ V)					
Recommended operating conditions					
Input impedance	$Z_{20\text{-}21}$		1.8/2		kΩ/pF
Output impedance	$Z_{3\text{-}4}$		6.6/2		kΩ/pF
Output resistance	$R_{6,7}$		400		Ω
Input resistance	$R_{i\,9\text{-}10}$		800		Ω
Output resistance	$R_{15\text{-}16}$		5.4		kΩ
Output resistance					
recording	R_{q12}			500	Ω
playback	R_{q12}	10			kΩ
Deemphasis resistance	R_{17}		10		kΩ
Output resistance	R_{q11}			50	Ω
IF control voltage					
V_{max}	$V_{1\text{-}2}$	0			V
V_{min}	$V_{1\text{-}2}$			4	V
***) Test conditions**					
Video carrier/sound carrier	$a_{VC\text{-}SC}$		10		dB
Modulation frequency	f_{mod}		1		kHz
Frequency deviation	Δf		50		kHz
IF input voltage	V_{iIF}		20		mV

Circuit description

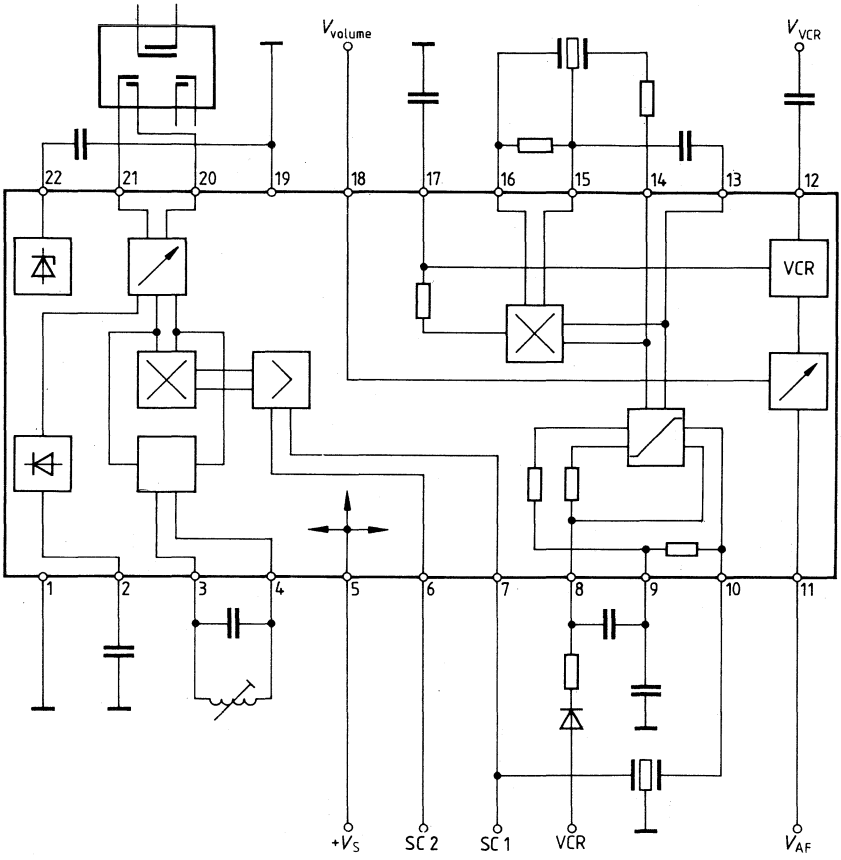
The integrated circuit contains two functional blocks:

1. A controlled AM aplifier with a peak rectifier to generate the AGC voltage. At the output of the FM demodulator, which is driven by the AM amplifier, the differential sound carrier frequencies 5.5 MHz and 5.74 MHz are available at one output each. The double sideband portions close to the carrier are suppressed. The 5.5 MHz carrier reaches the functional block 2 via an external selection.
2. An FM limiter amplifier with coincidence demodulator, a standard VCR connection and a separate AF output with volume control.

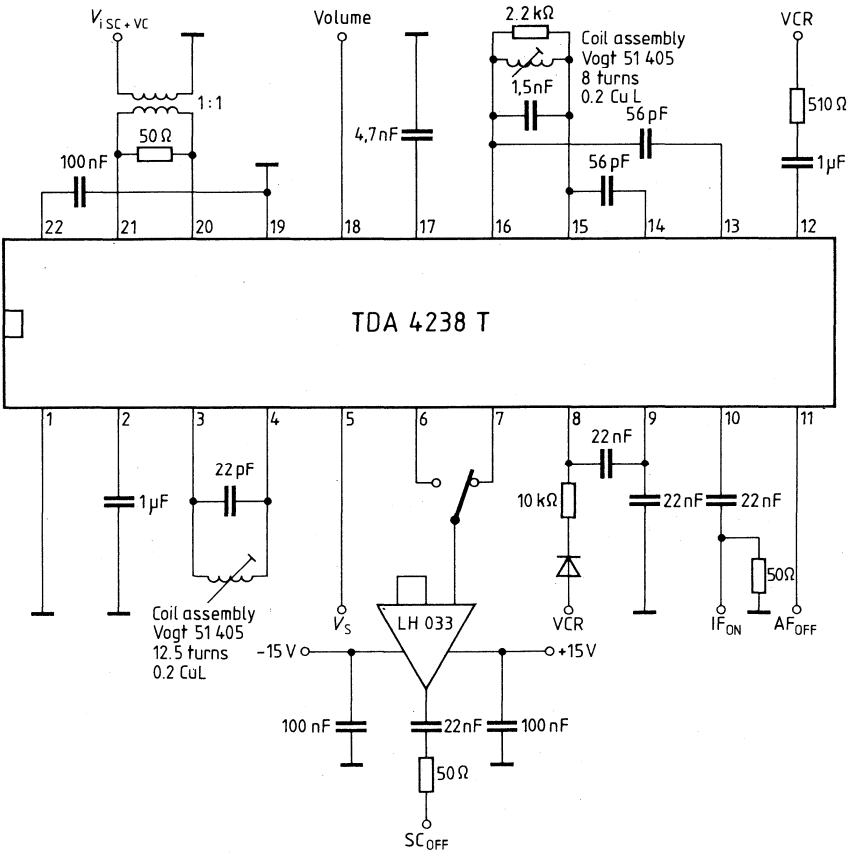
Pin configuration

Pin No.	Function
1	Ground
2	AM IF control
3	AM amplifier demodulator
4	AM amplifier demodulator
5	Supply voltage (plus)
6	AM amplifier sound carrier output SC1
7	Am amplifier sound carrier output SC2
8	FM IF amplifier feedback for working point
9	FM IF amplifier feedback for working point
10	FM IF amplifier IF input
11	AF output
12	VCR connection
13	FM IF amplifier emitter follower output
14	FM IF amplifier emitter follower output
15	FM amplifier demodulator
16	FM amplifier demodulator
17	Connection for deemphasis capacitor
18	Volume control
19	Ground
20	AM IF amplifier IF input
21	AM IF amplifier IF input
22	$V_{ref\,AM}$

Block diagram



Test and measurement circuit



Bipolar circuit

Type	Ordering code	Package outline
TDA 4290-2	Q67000-A1359	DIP 14
TDA 4290-2 S	Q67000-A1359-E20	

The tone control unit is provided for the DC voltage control of volume, treble, and bass. The volume characteristic can be changed from linear to physiological.

For mono application we recommend the TDA 4290-2, while the TDA 4290-2 S is especially suitable for stereo application.

Features

- Few external components
- High signal-to-noise ratio
- Low total harmonic distortion
- Satisfies the IEC 268-3 standards

Maximum ratings

Supply voltage	V_S	18	V
Control inputs	V_5, V_8, V_{14}	0 to V_S	V
Input signal	$V_{8\,rms}$	3	V
Load current	I_2	10	mA
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	90	K/W

Operating range

Supply voltage range	V_S	10.5 to 18	V
Volume control range	V_5	0 to 0.51 x V_2	V
Frequency range (−1 dB)	f_i	20 to 20,000	Hz
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics ($V_S = 14$ V; $T_{amb} = 25$ °C)

Measurement circuit 1

		min	typ	max	
Current consumption	I_S		35	50	mA
Reference voltage	V_2	4.5	4.85	5.2	V
Input resistance	R_{i9}	2.9	3.9		kΩ
Output resistance	$R_{q\,3/6}$		200		Ω
Changeover current	I_4		3.5		mA
Input current for set inputs ($V_{5/8/14} = 0.5 \times V_2$)	$-I_{5/8/14}$		4	20	µA
Attenuation					
($V_i = 300$ mV, $f = 1.6$ kHz, $V_8 = 0.5 \times V_2$, $V_{14} = 0.49 \times V_2$, S1 on physiology)					
$V_5 = 0.51 \times V_2$	$V_{q\,0} = V_q/V_i$	−3	0	3	dB
$V_5 = 0.41 \times V_2$	$V_q/V_{q\,0}$	−17	−15	−13	dB
$V_5 = 0.33 \times V_2$	$V_q/V_{q\,0}$	−33	−30	−27	dB
$V_5 = 0.25 \times V_2$	$V_q/V_{q\,0}$	−48	−44	−40	dB
Max. attenuation	$V_q/V_{q\,0}$	−75	−80		dB
Frequency response					
($V_i = 300$ mV, $V_5 = 0.51 \times V_2$, S1 any)					
Linearity $V_8 = 0.5 \times V_2$ $V_{14} = 0.49 \times V_2$, $f = 40$ to 15,000 Hz	$V_q/V_{q\,8}$	−3	0	3	dB
Influence at $f = 1$ kHz					
Trebles/basses max.	$V_q/V_{q\,0}$		2	3	dB
Trebles/basses min.	$V_q/V_{q\,0}$	−3	−2		dB
Treble emphasis ($f_i = 15$ kHz, $V_{14} = V_2$, $V_8 = 0.5 \times V_2$)	$V_q/V_{q\,8\,0}$	+15	+17		dB
Treble deemphasis ($f_i = 15$ kHz, $V_{14} = 0$ V, $V_8 = 0.5 \times V_2$)	$V_q/V_{q\,8\,0}$		−17	−15	dB
Bass emphasis ($f_i = 40$ Hz, $V_8 = V_2$, $V_{14} = 0.49 \times V_2$)	$V_q/V_{q\,8\,0}$	+15	+17		dB
Bass deemphasis ($f_i = 40$ Hz, $V_8 = 0$ V, $V_{14} = 0.49 \times V_2$)	$V_q/V_{q\,80}$		−17	−15	dB
Total harmonic distortion ($V_{i\,rms} = 300$ mV, $f_i = 40$ Hz to 15 kHz, control unit in 0 dB position)	THD		0.1	0.5	%
Disturbance voltage ($f_i = 20$ to 20,000 Hz, tone control in 0 dB position, volume −20 dB)	$V_{d\,rms}$		30	50	µV

TDA 4290-2 S

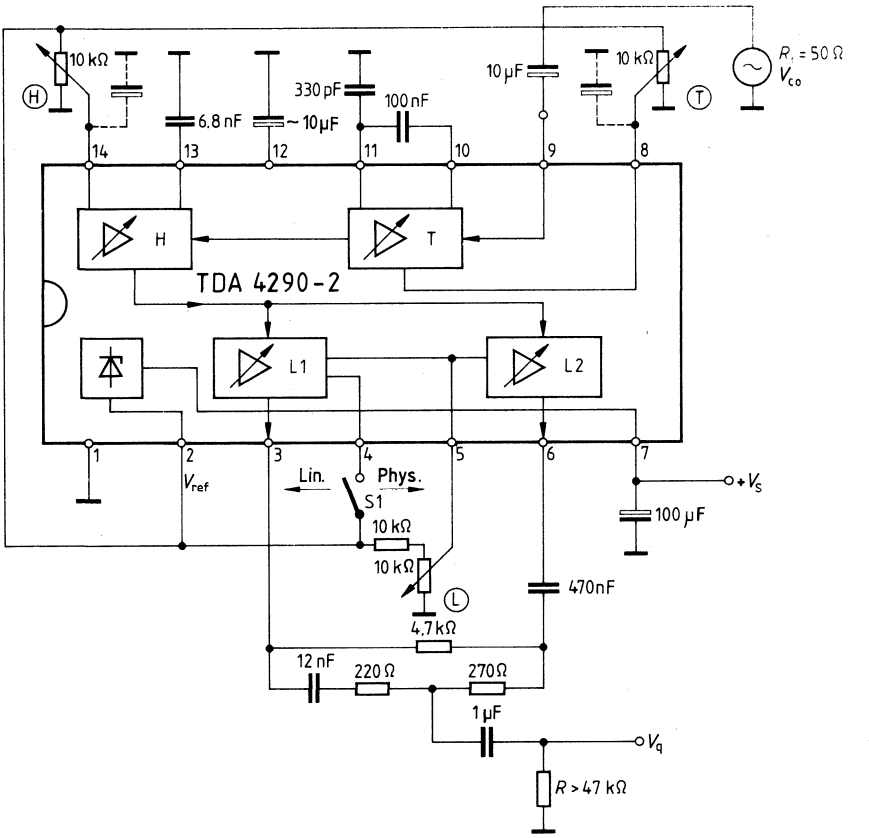
Physiology tone control in 0 dB position
(V_i = 300 mV, S1 at physiology)

f = 1.6 kHz		f = 40 Hz			f = 15 kHz			
		min	typ	max	min	typ	max	
V_q/V_{q0} = −15 dB	V_q/V_{q0}	−11.0	− 9.0	− 7.0	−16.5	−13.5	−10.5	dB
V_q/V_{q0} = −30 dB	V_q/V_{q0}	−20.5	−17.5	−14.5	−28.0	−25.0	−22.0	dB
V_q/V_{q0} = −45 dB	V_q/V_{q0}	−30.0	−27.0	−24.0	−41.0	−37.0	−33.0	dB

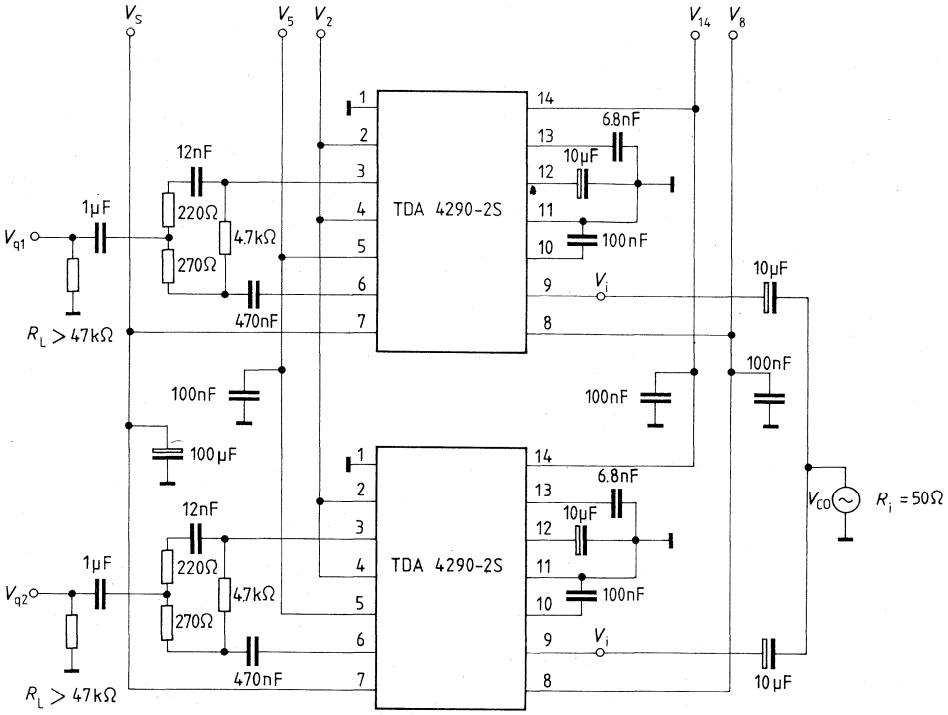
Synchronous operation (measurement circuit 2)
(V_i = 300 mV, f = 1.6 kHz, V_8 = 0.5 x V_2, V_{14} = 0.49 x V_2, S1 at physiology)

		min	typ	max	
V_{q1}/V_i = 0 dB	V_{q1}/V_{q2}	−1	0	1	dB
V_{q1}/V_i = −15 dB	V_{q1}/V_{q2}	−1.5	0	1.5	dB
V_{q1}/V_i = −30 dB	V_{q1}/V_{q2}	−2	0	2	dB
V_{q1}/V_i = −45 dB	V_{q1}/V_{q2}	−2.5	0	2.5	dB
V_{q1}/V_i = −60 dB	V_{q1}/V_{q2}	−3	0	3	dB

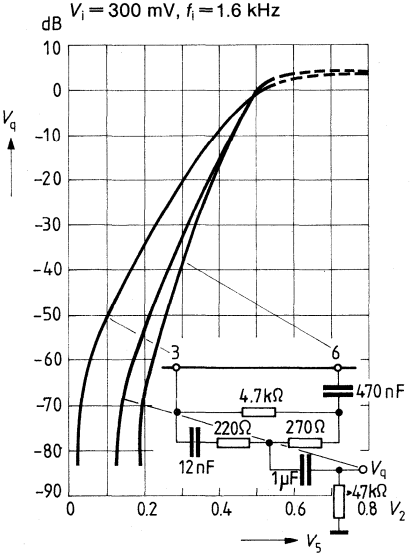
Measurement circuit 1 (mono operation)



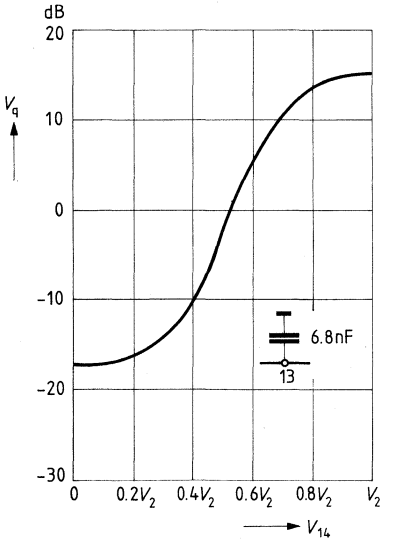
Measurement circuit 2 (stereo operation)



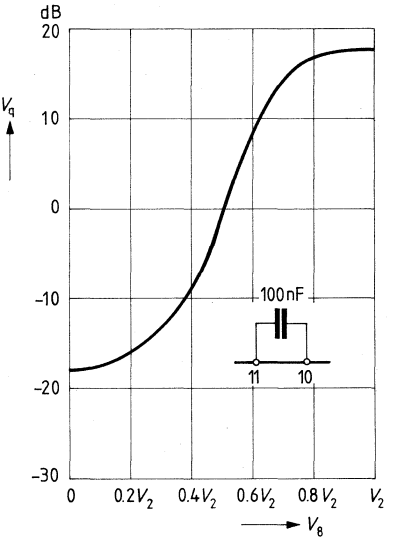
Physiological volume characteristic
(treble and bass control in linear position)
$V_i = 300$ mV, $f_i = 1.6$ kHz



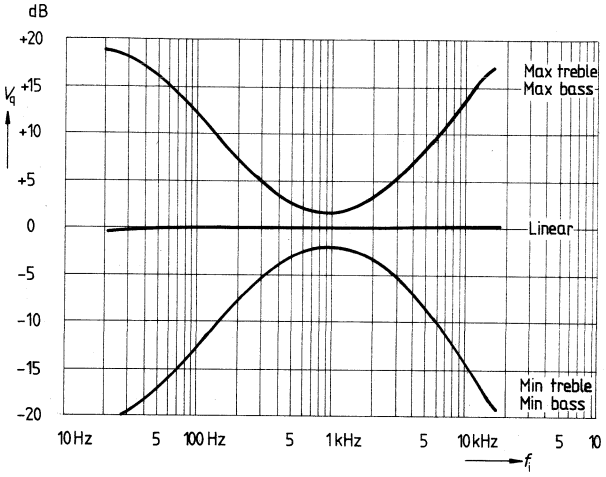
Treble control
S1 open; $V_{irms} = 300$ mV; volume = 0 dB
$V_i = 300$ mV, $f_i = 20$ kHz



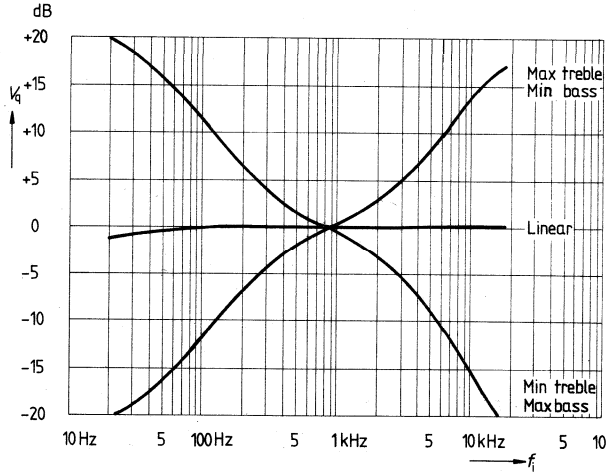
Bass control
S1 open; $V_{irms} = 300$ mV; volume = 0 dB
$V_i = 300$ mV, $f_i = 20$ Hz



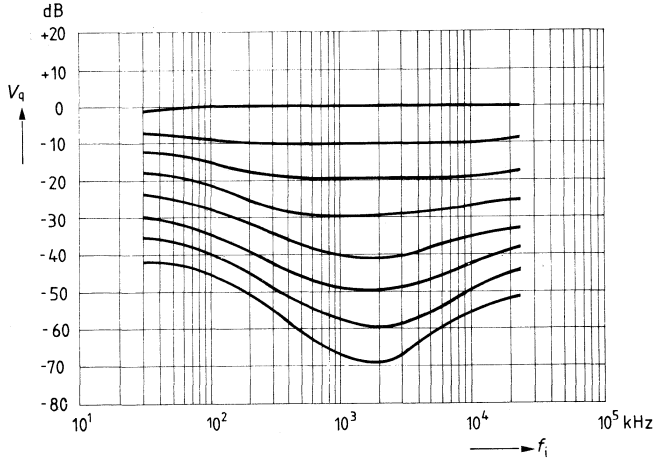
Bass and treble control
V_i = 300 mV ≙ 0 dB; S1 open



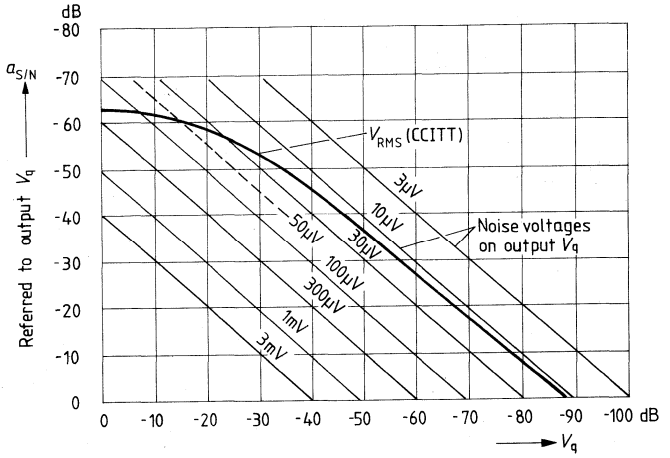
Bass and treble control
V_i = 300 mV ≙ 0 dB; S1 open



Physiological volume versus input frequency
S1 closed; $V_{irms} = 300$ mV ≙ 0 dB



Disturbance voltage spacing
Bandwidth 30 Hz to 20 Hz; $V_{irms} = 300$ V ≙ 0 dB; $f_i = 1$ kHz
S1 open; treble and bass control in linear position



Preliminary data **Bipolar circuit**

Type	Ordering code	Package outline
TDA 4292	Q67000-A2197	DIP 24

In conjunction with dc voltages, the stereo tone control integrated circuit regulates treble, bass, balance, and volume of the audio input signal.

For the first time a width control has been included for the AF signal. The integrated circuit TDA 4292 is in compliance with the hi-fi standards DIN 45500 and IEC 268-3.

Features

- Few external components
- Low total harmonic distortion
- Large output signal capability

Maximum ratings

Supply voltage	V_{S16}	18	V
Reference current	I_{ref1}	5	mA
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	70	K/W

Operating range

Supply voltage range	V_{S16}	8 to 15.75	V
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics ($V_S = 15$ V; $T_{amb} = 25$ °C)

		min	typ	max	
Total current consumption (P1...P4 = 22 kΩ)	I_{S16}		40		mA
Reference voltage	V_{ref1}		4.8	5.2	V
Input resistance	$R_{i4;22}$	10	14	18	kΩ
Gain for $V_{24} = V_{ref}$[1] (S1 open or closed; S2 open) $V_{3,2,23} = V_{ref}/2$	V_q/V_i		0		dB
Gain for $V_{24} = 0$[1] ($V_{irms} = 1$ V)	V_q/V_i			−85	dB
Control range balance[1] ($V_{24} = V_{ref}$; $V_{2,3} = V_{ref}/2$)	$V_{B\,max}$ $V_{B\,min}$		4 −30	6	dB dB
Bass emphasis[1] ($V_3 = V_{ref}$; $f_i = 40$ Hz)	$V_{B\,max}$		+12		dB
Bass deemphasis ($V_3 = 0$; $f_i = 40$ Hz)	$V_{B\,min}$		−12		dB
Treble emphasis[1] ($V_2 = V_{ref}$; $f_i = 15$ Hz)	$V_{T\,max}$		+12		dB
Treble deemphasis ($V_2 = 0$; $f_i = 15$ kHz)	$V_{T\,min}$		−12		dB
Channel separation S2 open	$a_{L\text{-}R}$	60			dB
Channel separation (antiphased) for S2 closed	$a_{L\text{-}R}$		5		dB
Input voltage[1] $V_{2,3}$ = any $V_{2,3} = V_{ref}/2$	 $V_{i\,rms\,4,22}$ $V_{i\,rms\,4,22}$			 1 3.5	 V V
Total harmonic distortion[1] ($V_{2,3}$ = as applied; $V_{irms} = 1$ V)	THD		0.5	1	%
Total harmonic distortion DIN 45500[1] ($V_{2,3} = V_{ref}/2$; $V_{irms} = 1$ V)	THD		0.3	0.6	%
Flutter and wow L-R	$\Delta a_{L\text{-}R}$			2	dB
Disturbance voltage spacing according DIN 45405 ($f = 20$ Hz to 20 kHz; $V_{irms} = 1$ V; $V_i/V_q = 0$ dB)	$a_{S+N/N}$		77		dB
Noise voltage with reference to output ($f = 20$ Hz to 20 kHz) $V_i/V_q = 0$ dB $V_i/V_q = 50$ dB	 $V_{n\,rms}$ $V_{n\,rms}$		 120 10	 150 20	 μV μV
Output resistance	$R_{q\,11,12,14,15}$		0.2	0.3	kΩ
Input current for adjusters	$I_{i\,2,3,23,24}$		7		μA
Input current for switches	$I_{i8,18}$			60	μA
Input frequency (−1 dB)	$f_{i\,4,22}$	20		20,000	Hz

Electrical data identified with [1] is only applicable at $V_S = 15$ V +5% and $V_{rms} = 1$ V. Furthermore, the maximum input voltage decreases in accordance with lower supply voltages.

Characteristics ($V_S = 15$ V; $T_{amb} = 25$ °C)

		min	typ	max	
Level of the switches or open	$V_{sch\,H}$ $V_{sch\,L}$	V_{ref} −1 0		V_{ref} 1	V V
Difference of the AF outputs with physiology on $V_L = 3/4\ V_{ref}$	ΔV_q		25		dB
Noise voltage at the output $f = 20$ Hz to 20 kHz DIN 45405 $V_i/V_q = -20$ dB	$V_{n\,vol}$			50	µV
Noise voltage CCIR DIN 45405 $V_L = V_{ref}$; $V_H = 0$	V_r			650	µV
Amplitude variation trebles, basses in middle position $V_{T,B} = V_{ref}/2$ $f_i = 40$ Hz, 1 kHz, 15 kHz			±0.5	±1.5	dB

Pin configuration

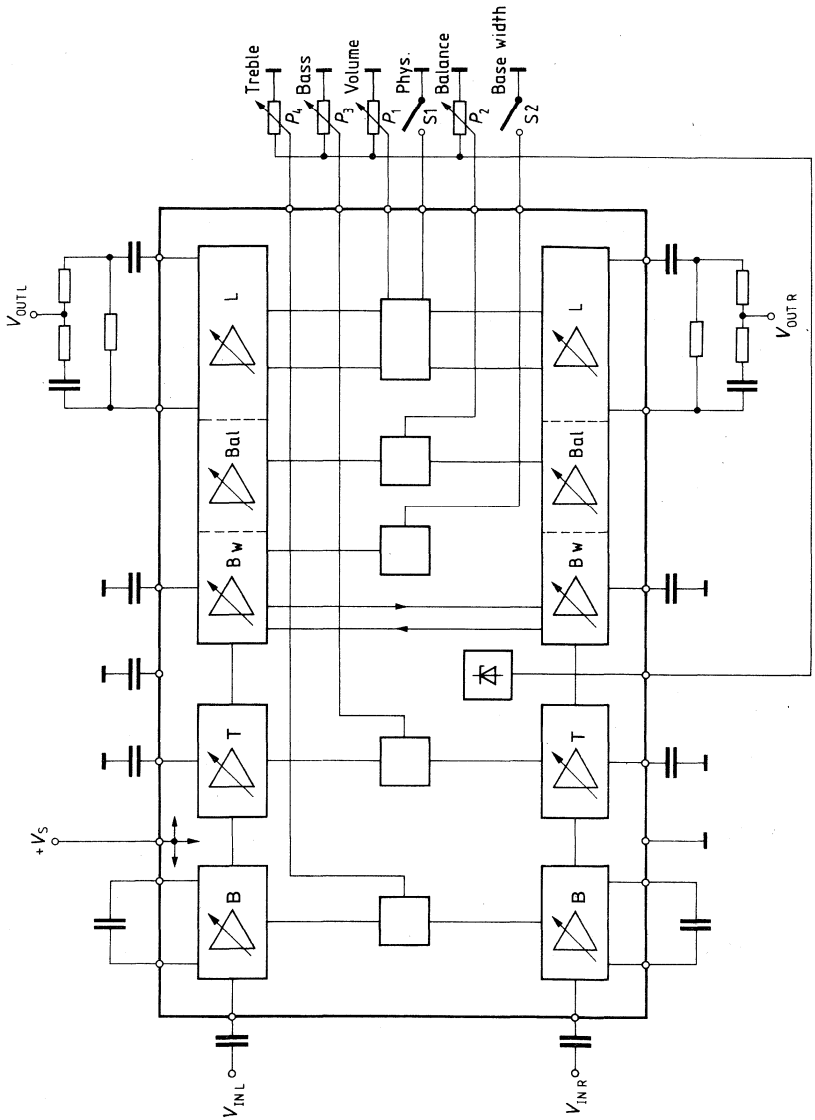
Pin No.	Function
1	Reference voltage
2	Treble control input
3	Bass control input
4	Input right
5	Cutoff frequency bass
6	Right
7	Cutoff frequency treble right
8	Switch input physiology
9	Start frequency base width right
10	Ground
11	Output right
12	Output right
13	Blockage
14	Output left
15	Output left
16	Supply voltage
17	Start frequency base width left
18	Switch input base width
19	Cutoff frequency treble left
20	Cutoff frequency bass
21	Left
22	Input left
23	Balance control input
24	Volume control input

Circuit description

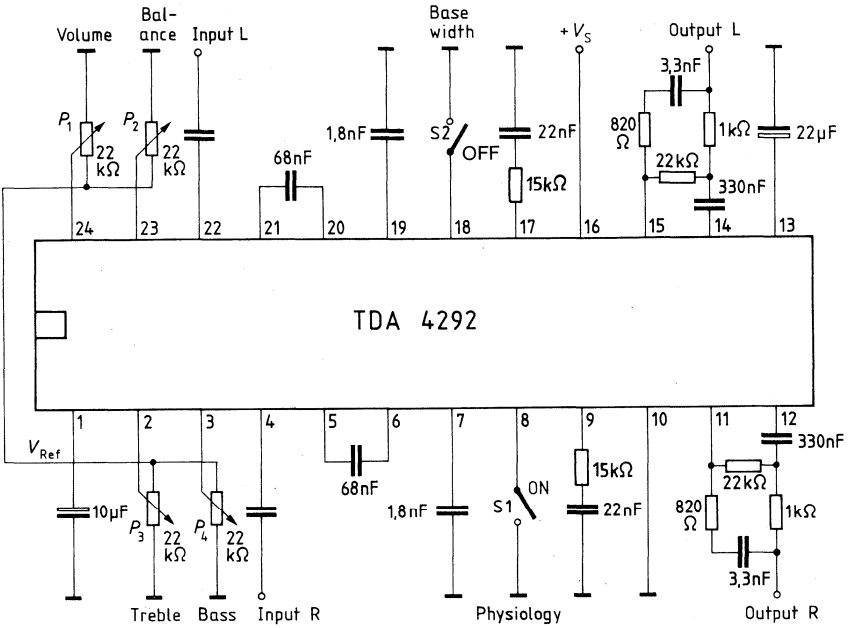
The component includes 5 operational amplifiers per stereo channel. The operational amplifiers are equipped with either dc voltage controlled attenuators or switches. By applying potentiometers to the externally connected capacitors, the emphasis or deemphasis of low or high frequencies can be controlled. The base width can be switched by the subsequent stage. This stage will not respond during open switch status. However, with a closed switch, antiphased crosstalk of estimated 66% occurs at a frequency of approx. 300 Hz, which has been determined by one of the external capacitors. To ensure that the base width effect remains independent of the balance setting, balance control is performed subsequently to the base width control. The volume control is comprised of 2 stages. The identical configuration and parallel layout of these stages, designed to affect base width, balance, and volume, provide at the same time simultaneous electrical and thermical tracking. In the volume stage the rising incline of the volume characteristic can be switched to lower values. Both outputs have been equipped with a resistor capacitor network for physiologically correct amplification adjustment. Frequency independent (linear) amplification adjustment is obtained during the identical rise of the volume characteristic at both outputs.

In order to prevent disruptive clicking noises, the delay switch releases the AF output voltage subsequently to the supply voltage and voltage stabilization in the component.

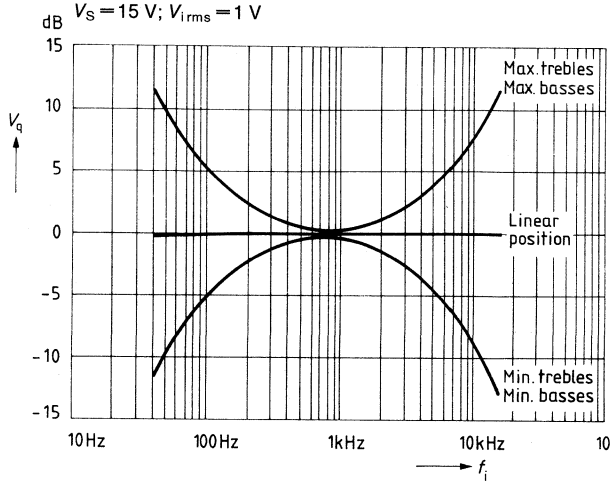
Block diagram



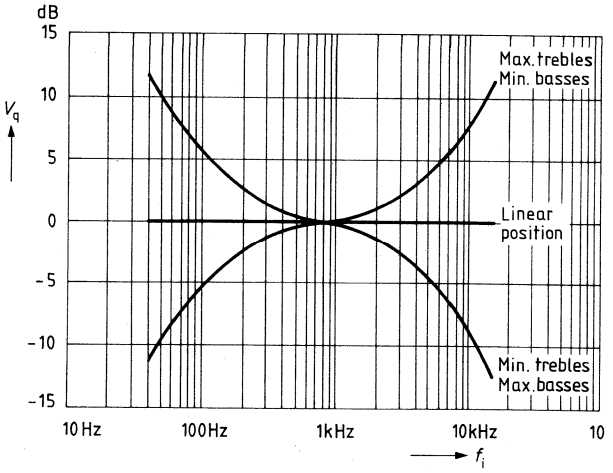
Application circuit



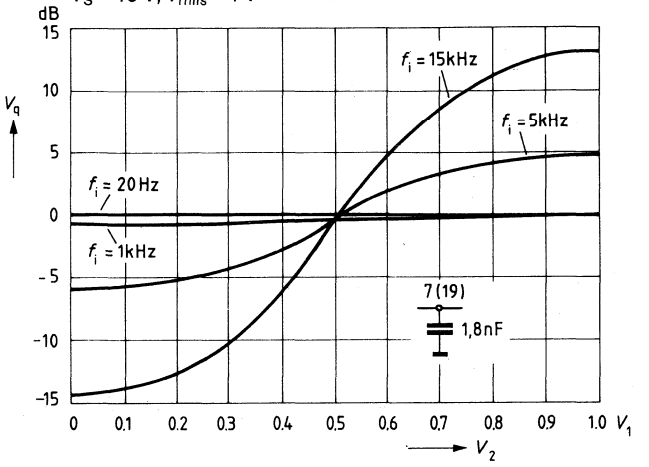
Bass and treble control
Physiology OFF, base width OFF
$V_S = 15$ V; $V_{irms} = 1$ V



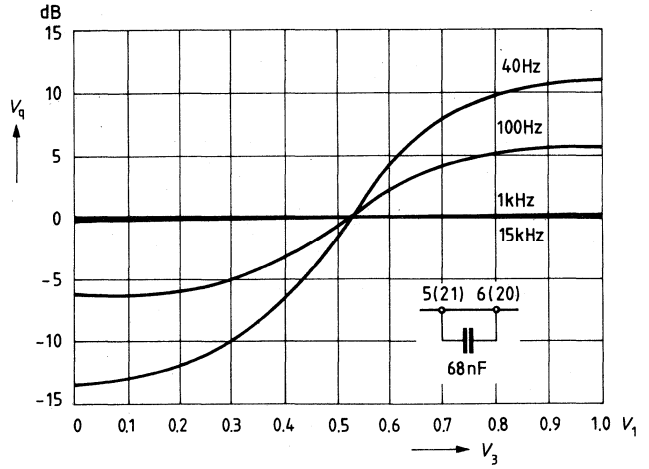
Bass and treble control
Physiology OFF; base width OFF
$V_S = 15$ V; $V_{irms} = 1$ V



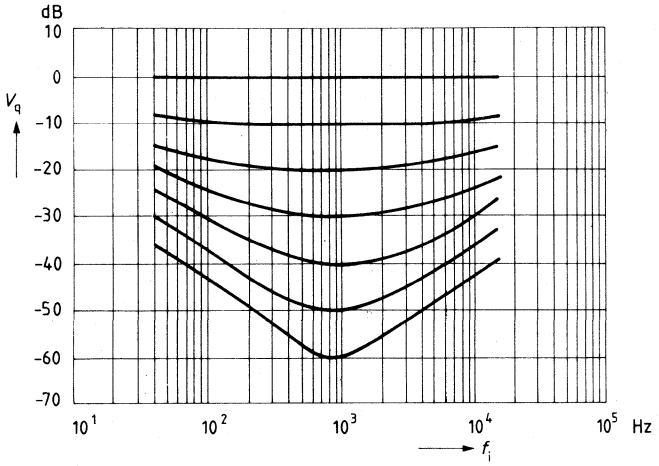
Treble control
Physiology OFF, base width OFF
$V_S = 15$ V; $V_{irms} = 1$ V



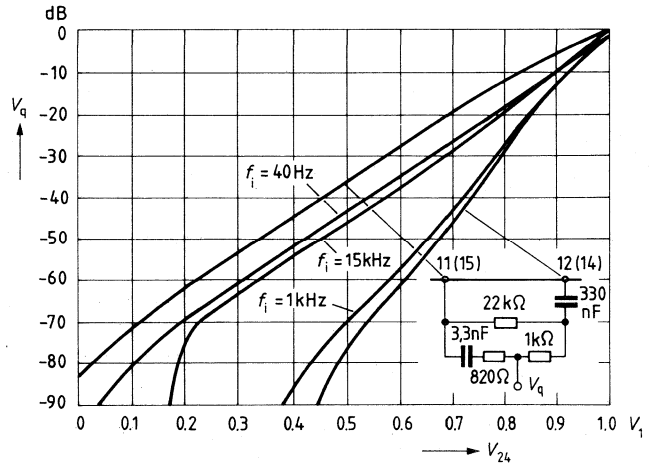
Bass control
Physiology OFF, base width OFF
$V_S = 15$ V; $V_{irms} = 1$ V



Physiological volume control
$V_{irms} = 1$ V



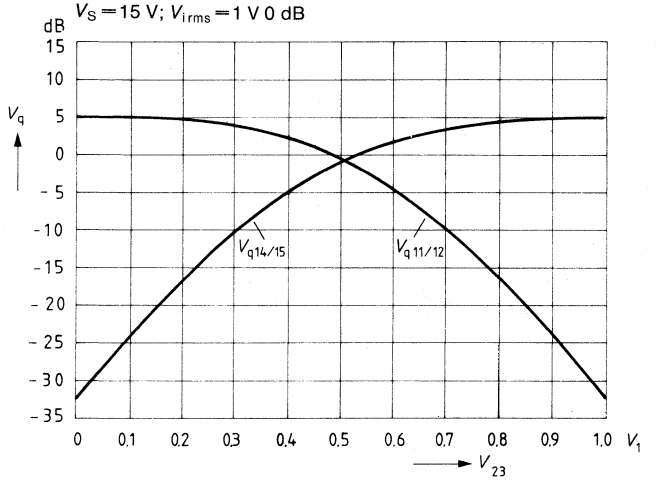
Volume control with physiology
$V_S = 15$ V; $V_{irms} = 1$ V



Balance

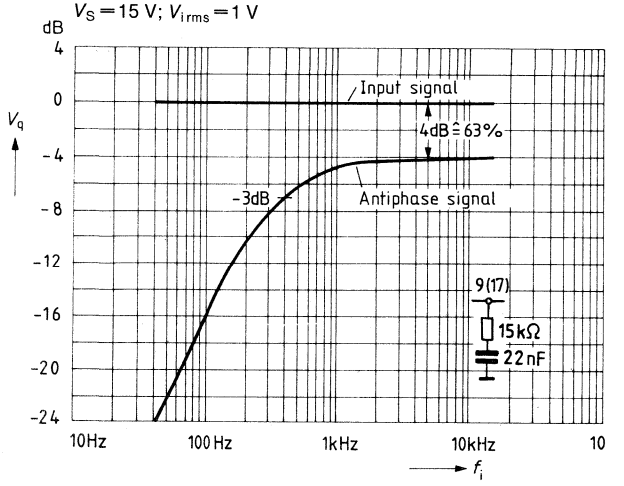
Physiology and base width OFF

$V_S = 15$ V; $V_{irms} = 1$ V 0 dB

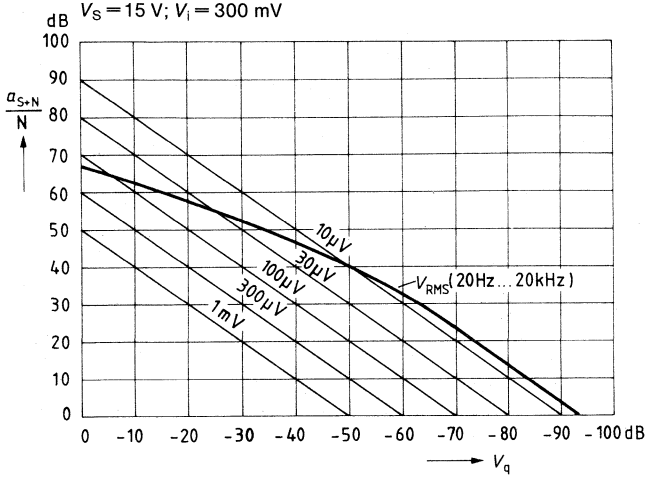


Base width

$V_S = 15$ V; $V_{irms} = 1$ V

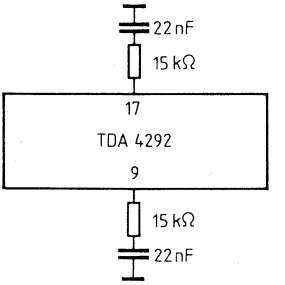


Disturbance voltage spacing
Physiology OFF, base width OFF
$V_S = 15$ V; $V_i = 300$ mV



Base width circuits

1.



a) **Stereo reception**

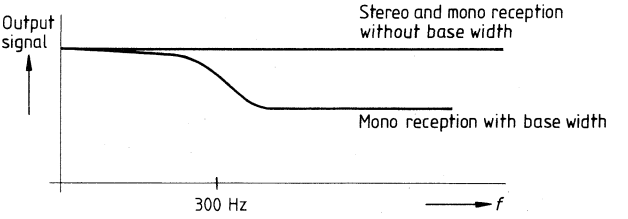
i.e. normal linear frequency response and stereo sensation with closely spaced loudspeakers.

With the base width ON the base-width effect has a time constant of 22 nF/15 kΩ, i.e. the subjective spacing between the loudspeakers is greater.

b) **Mono reception** (with base width ON)

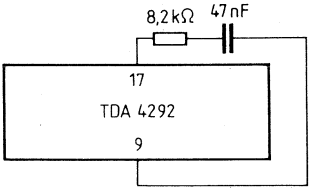
Normal linear frequency response and mono sensation.

With the base width ON there is a deemphasis of approx. −5 dB onwards from about 300 Hz. This causes slight treble deemphasis and the acoustic impression is duller and somewhat quieter.



Effect: At mono signal: trebles approx. −5 dB
At stereo signal: cross-talk over 300 Hz

2.

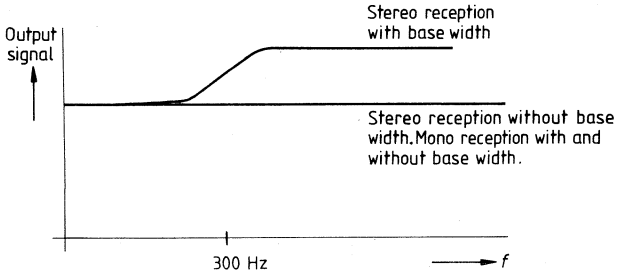


a) **Stereo reception and base width ON**

The trebles are emphasized from 300 Hz onwards by up to +5 dB (time constant 8.2 kΩ and 4 nF), i.e. with the base width switched on there is simultaneously a slight change in the timbre of the acoustic impression.

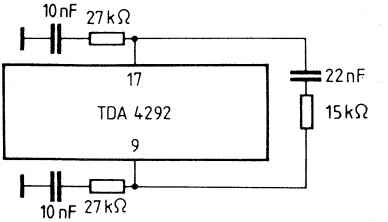
b) **Mono reception and base width ON**

Switching on the base width produces no change at all in the acoustic impression.



Effect: At mono signal: no influence
At stereo signal: trebles approx. +5 dB

3.



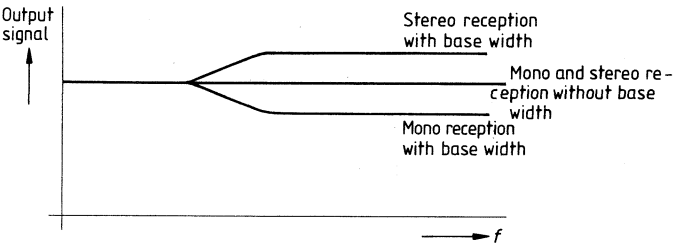
a) **Stereo reception and base width ON**

Emphasis of the trebles onwards from 300 Hz by +2.5 dB with the corresponding time constants.

b) **Mono reception and base width ON**

From about 300 Hz onwards deemphasis by about –2.5 dB.

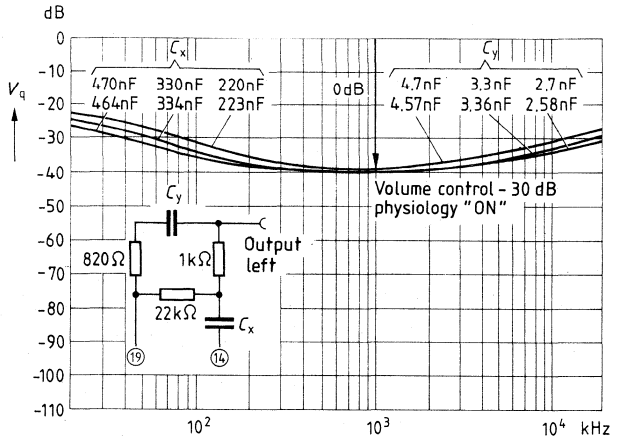
With the corresponding time constants this produces a slight loss of treble and makes the acoustic impression darker and quieter.



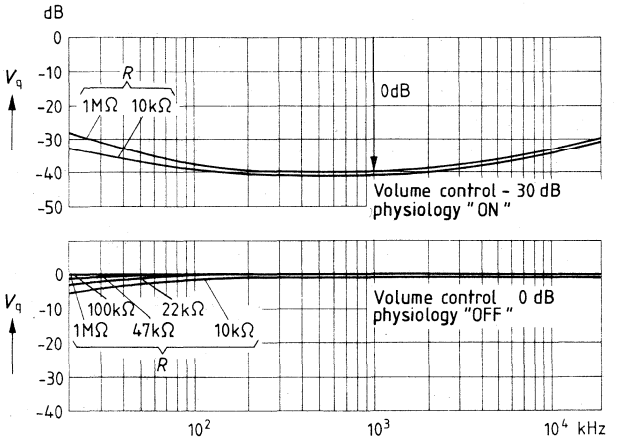
Effect: At mono signal: trebles approx. –2.5 dB
At stereo signal: trebles approx. +2.5 dB

Detailed information upon request

Physiological volume control (loudness) versus frequency and capacitance values C_x G_V deviations for different capacitances (R_L at output 1 MΩ).

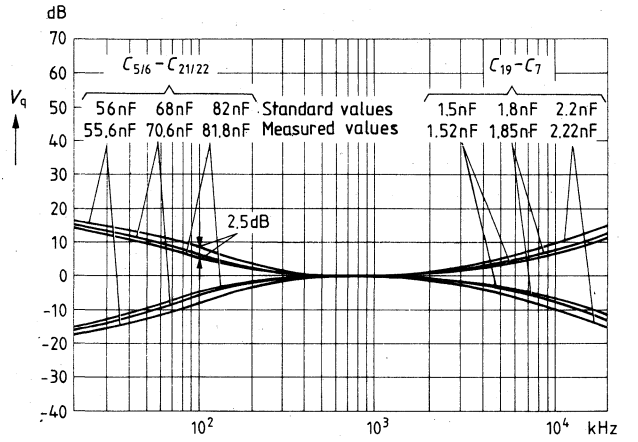


Physiological volume control (loudness) versus frequency and load resistance R
Output loaded with R ($C_y = 3.3$ nF; $C_x = 680$ nF).



Bass and treble control versus frequency

G_V deviations for different capacitances (load at output 1 MΩ)



Alteration of frequency response through component tolerances

- **Bass control**

Capacitor	Pin 21/20 – 5/6	$C = 68$ nF
68 nF − 20%	$G_V = +1.5$ dB	
68 nF	$G_V = 0$ dB	$f = 100$ Hz
68 nF + 20%	$G_V = -1$ dB	

- **Treble control**

Capacitor	Pin 19 – 7	$C = 1.8$ nF
1.8 nF − 20%	$G_V = -1$ dB	
1.8 nF	$G_V = 0$ dB	$f = 10$ kHz
1.8 nF + 20%	$G_V = +1.5$ dB	

- **Physiology network**

Capacitor for bass emphasis		$C_x = 330$ nF
330 nF − 30%	$G_V = -3$ dB	
330 nF	$G_V = 0$ dB	$f = 100$ Hz
330 nF + 40%	$G_V = +2$ dB	

- **Capacitor for treble emphasis** $C_y = 3.3$ nF

3.3 nF − 20%	$G_V = 1$ dB	
3.3 nF	$G_V = 0$ dB	$f = 10$ kHz
3.3 nF + 40%	$G_V = +2$ dB	

- **Terminating resistor**

$R_A = 10$ kΩ	$G_V = -5$ dB	
$R_A = 22$ kΩ	$G_V = -2.5$ dB	
$R_A = 47$ kΩ	$G_V = -1$ dB	$f = 20$ Hz
$R_A = 100$ kΩ	$G_V = -0.5$ dB	
$R_A = 1$ MΩ	$G_V = 0$ dB	

Bipolar circuit

Type	Ordering code	Package outline
TDA 4600-2	Q67000-A1451 E19	SIP 9
TDA 4600-2 D	Q67000-A2171	DIP 18 L9 (Pin 6 and pin 10 to 18 are connected to ground)

In addition to their use with TV receivers and video recorders, these integrated circuits can be applied in power supplies of hi-fi sets and active speakers due to their wide operational ranges and superior voltage stability during high load changes.

- Direct driving of switching transistor
- Low start-up current
- Reversing linear overload characteristic
- Collector current – proportional to base-current input

Maximum ratings

Suuply voltage	V_9	0 to 20	V
Voltages			
reference output	V_1	0 to 6	V
identification input	V_2	−0.6 to 0.6	V
controlled amplifier	V_3	0 to 3	V
collector current simulation	V_4	0 to 7	V
blocking input	V_5	0 to 7	V
base current cut-off point	V_7	0 to V_9	V
base current amplifier output	V_8	0 to V_9	V
Currents			
feedback, zero passage	I_{i2}	−3 to 3	mA
controlled amplifier	I_{i3}	−3 to 3	mA
collector current simulation	I_{i4}	0 to 5	mA
base current cut-off point	I_{q7}	0 to 1.5	mA
base current amplifier output	I_{q8}	−1.5 to 0	mA
Junction temperature	T_j	125	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistances			
junction-ambient TDA 4600-2	$R_{th\,JA}$	70	K/W
junction-case	$R_{th\,JC}$	15	K/W
junction-ambient TDA 4600-2 D[1])	$R_{th\,JA}$	60	K/W
junction-ambient TDA 4600-2 D[2])	$R_{th\,JA1}$	44	K/W

Operating range

Supply voltage range	V_9	7.8 to 18	V
Package temperature range TDA 4600-2	T_p	0 to 85	°C
Ambient temperature range TDA 4600-2 D[3])	T_{amb}	0 to 70	°C

1) Package soldered in PCB without cooling area

2) Package soldered in PCB with copper-clad 35 µ layer, cooling area 25 cm^2

3) $R_{th\,JA1} = 44$ K/W and $P_V = 1$ W

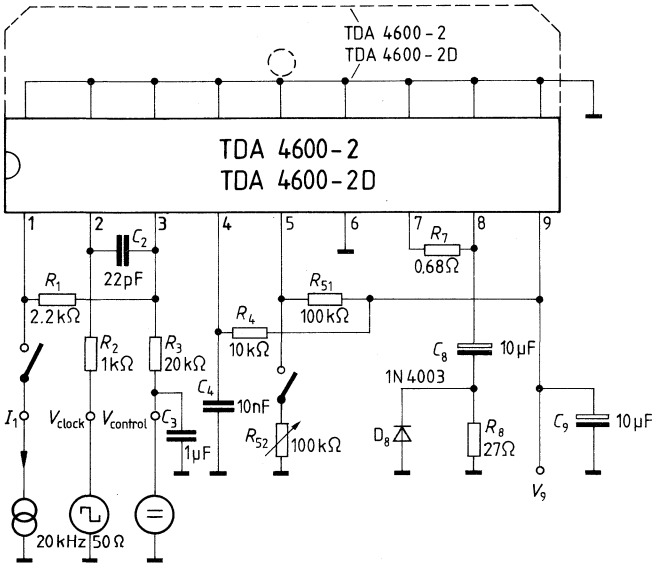
Characteristics (T_{amb} = 25 °C) according to test circuit 1 and diagram

		min	typ	max	
Start operation					
Current consumption (V_1 not yet switched on)					
V_9 = 2 V	I_9			0.5	mA
V_9 = 5 V	I_9		1.5	2.0	mA
V_9 = 10 V	I_9		2.4	3.2	mA
Switching point for V_1	V_9	11.0	11.8	12.3	V
Normal operation (V_9 = 10 V; $V_{control}$ = −10 V; V_{clock} = ±0.5 V; f = 20 kHz; duty cycle 1:2) after switch on					
Current consumption $V_{control}$ = −10 V	I_9	110	135	160	mA
$V_{control}$ = 0 V	I_9	55	85	110	mA
Reference voltage I_1 < 0.1 mA	V_1	4.0	4.2	4.5	V
I_1 = 5 mA	V_1	4.0	4.2	4.4	V
Temperature coefficient of reference voltage	TC_1		10^{-3}		1/K
Feedback voltage	V_2*)		0.2		V
Control voltage $V_{control}$ = 0 V	V_3	2.3	2.6	2.9	V
Collector current simulation voltage					
$V_{control}$ = 0 V	V_4*)	1.8	2.2	2.5	V
$V_{control}$ = 0 V/−10 V	ΔV_4*)	0.3	0.4	0.5	V
Blocking input voltage	V_5	5.5	6.3	7.0	V
Output voltage $V_{control}$ = 0 V	V_{q7}*)	2.7	3.3	4.0	V
$V_{control}$ = 0 V	V_{q8}*)	2.7	3.4	4.0	V
$V_{control}$ = 0 V/−10 V	ΔV_{q8}*)	1.4	1.8	2.2	V
Safety operation (V_9 = 10 V; $V_{control}$ = −10 V; V_{clock} = ±0.5 V; f = 20 kHz; duty cycle 1:2)					
Current consumption (V_5 < 1.8 V)	I_9	14	22	28	mA
Switch-off voltage (V_5 < 1.8 V)	V_{q7}	1.3	1.5	1.8	V
	V_4	1.8	2.1	2.5	V
Ext. blocking input					
enable voltage $V_{control}$ = 0 V	V_5		2.4	2.7	V
disable voltage $V_{control}$ = 0 V	V_5	1.8	2.2		V
Supply voltage					
for V_8 blocked $V_{control}$ = 0 V	V_9	6.7	7.4	7.8	V
Supply voltage for V_1 off	ΔV_9	0.3	0.6	1.0	V
(while further decreasing V_9)					
Characteristics (T_{amb} = 25 °C) according to test circuit 2					
Switch-on time (secondary voltages)	t_{on}		350	450	ms
Voltage change					
S3 = closed (ΔN_3 = 20 W)	ΔV_2		100	500	mV
Sound output power					
S2 = closed (ΔN_2 = 15 W)	ΔV_2		500	1000	mV
Standby operation					
(secondary useful load = 3 W)					
S1 = open	ΔV_2		20	30	V
	f	70	75		kHz
	$N_{primary\sim}$		10	12	VA

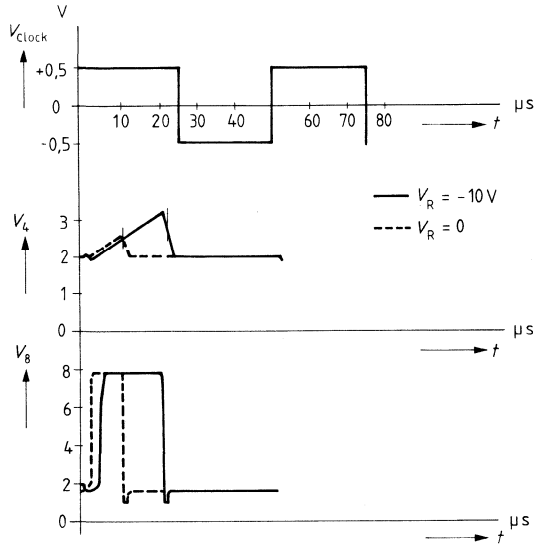
The cooling area has to be optimized according to the limit values (T_{amb}, T_j, $R_{th\,JC}$, $R_{th\,JA}$, $R_{th\,JA1}$)

*) only dc part

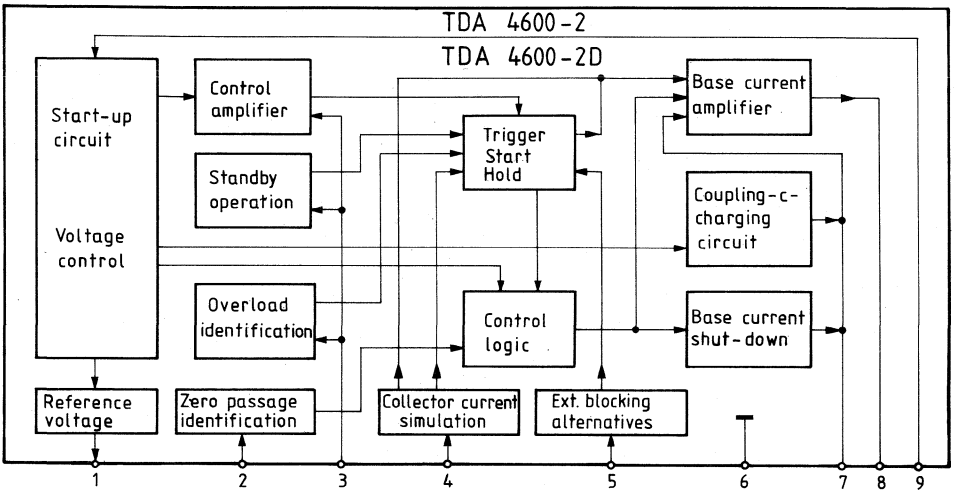
Test circuit 1



Test diagram for overload operations



Block diagram



Circuit description

During start-up, normal and overload operations the TDA 4600-2; or -2D regulates, controls and protects the switching transistor installed in the flyback converter power supplies.

A. Start-up operation

The start-up operation is divided into three consecutive phases:

1. An interal reference voltage is built up which supplies the voltage regulator and effects the charging of the coupling electrolytic capacitor and the switching transistor. During these procedures an I_9 current less than 3.2 mA will be maintained, if the supply voltage V_9 does not exceed $\approx$ 12 V.
2. At $V_9 \approx 12$ V an internal reference voltage $V_1 = 4$ V is suddenly released to provide all IC components with the exception of the control logic with a thermally stable and overload-resistant current.
3. In concurrence with the release of the reference voltage the control logic is activated by an additional stabilization circuit, and the IC is now ready for operation.

Above sequential start-up phases ensure the charging of the switching transistor by the coupling electrolytic capacitor and subsequent precision switching.

B. Normal Operation

Zero passages of the feedback coil are registered at pin 2 and forwarded to the control logic.

At pin 3 (input control, overload, and standby recognition) the rectified amplitude variations of the feedback coil are applied. The regulating (control) amplifier operates with an input voltage of about 2 V and a current of about 1.4 mA. According to the internal reference voltage, the operating region of the regulating amplifier will be defined by the collector current simulation pin 4 and the overload recognition. The simulation of the collector current is generated by an external *RC* network at pin 4 and an internally set voltage level. By increasing the capacitance (10 nF), the collector current of the switching transistor is increased as well and establishes the desired control range. The control range extends between a 2 V clamped dc voltage and an ac voltage rising as a sawtooth wave, which may vary up to a maximum amplitude of 4 V (reference voltage).

By reducing the secondary load to 20 W, the switching frequency increases to about 50 kHz at an almost constant pulse duty factor (on-time to period approx. 1/3). During additional secondary load reduction to about 1 W, the switching frequency will change to approx. 70 kHz, while the pulse duty factor falls to approx. 1/11. At the same time, the collector peak current falls below 1 A.

The output level of the regulating (control) amplifier, the overload recognition, and the collector current simulation are compared in the trigger and the control logic is instructed accordingly. Pin 5 will provide additional blocking alternatives, i.e. the output at pin 8 is blocked at a voltage of less than 2.2 V at pin 5.

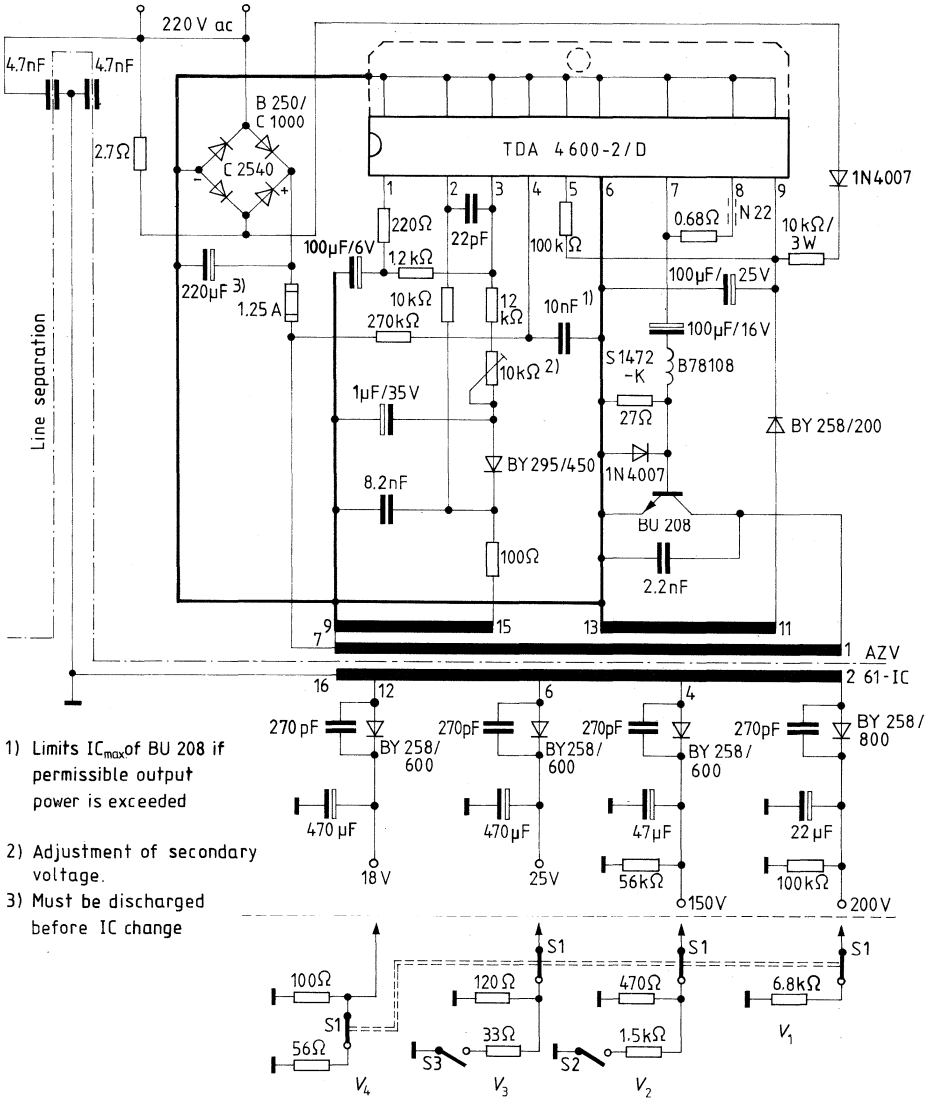
Based on the start-up circuit, the zero crossing identification, and the trigger-activated release, the control logic flipflops are set which control both the base current amplification and shut-down. The base current amplifier forwards the sawtooth voltage V_4 to pin 8. Also, a current feedback with an external resistance of $R \approx 0.68\ \Omega$ is inserted between pin 8 and pin 7. The resistance value determines the maximum amplitude of the base current for the switching transistor.

C. Safety features

The base current shut-down, released by the control logic, clamps the output of pin 7 at 1.6 V and thus blocks the driving of the switching transistor. This preventive method will go into effect, if the voltage at pin 9 falls below typ. 7.4 V or if voltages of less than typ. 22 V are present at pin 5. In case of short-circuited secondary windings in the SMPS, the fault condition will be continuously monitored by the IC.

With the load completely removed from the secondary winding in the SMPS, the IC is set at a small pulse duty factor. The total power consumption of the SMPS is kept below $n = 6$ to 10 W during both operating conditions. After the output has been blocked at a supply voltage V_9 of less than or equal to typ. 7.4 V, an additional voltage reduction of $\Delta V_9 = 0.6$ V will switch off the reference voltage (4 V).

Test circuit 2 and application circuit

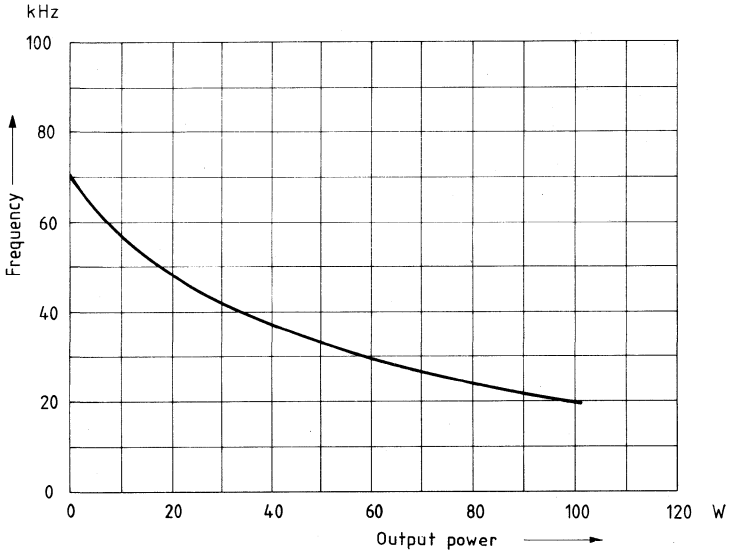


1) Limits IC_{max} of BU 208 if permissible output power is exceeded

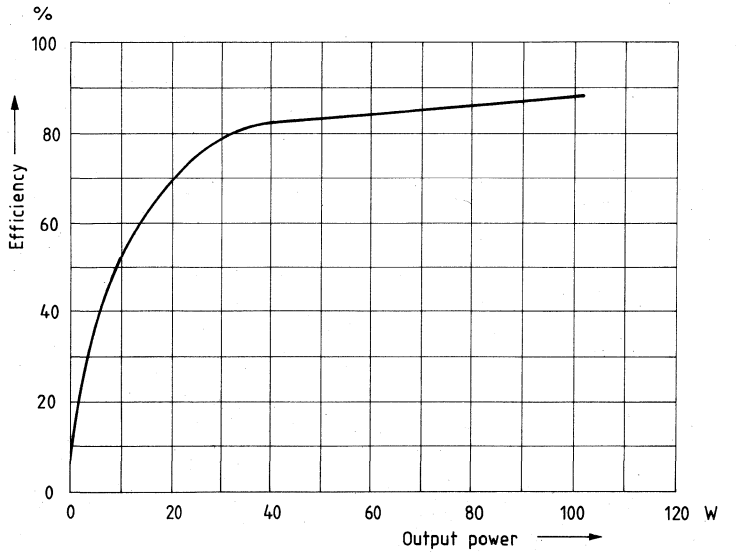
2) Adjustment of secondary voltage.

3) Must be discharged before IC change

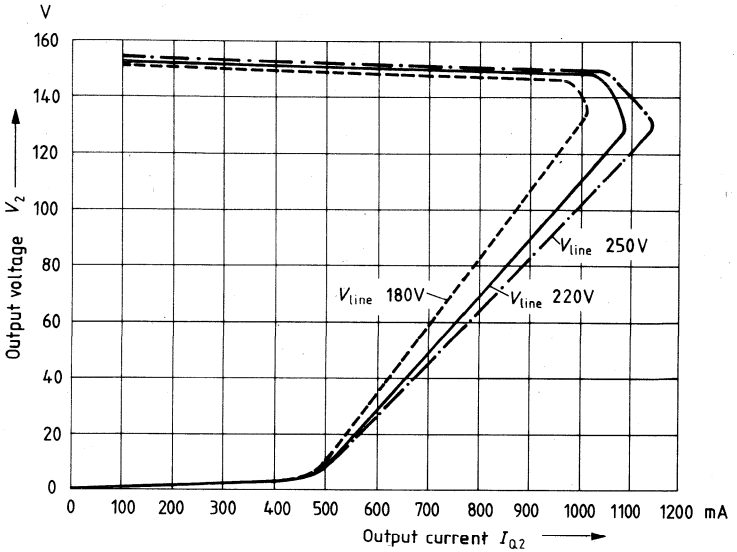
Frequency versus output power



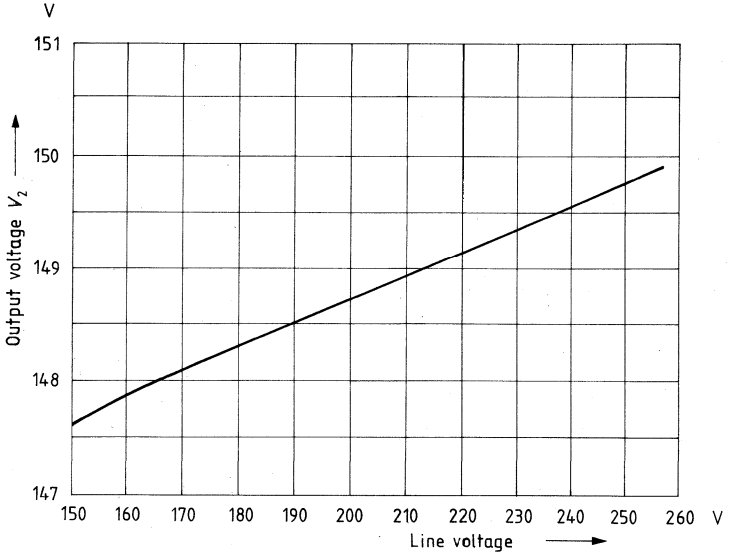
Efficiency versus output power



Load characteristic V_2 versus I_{q2}



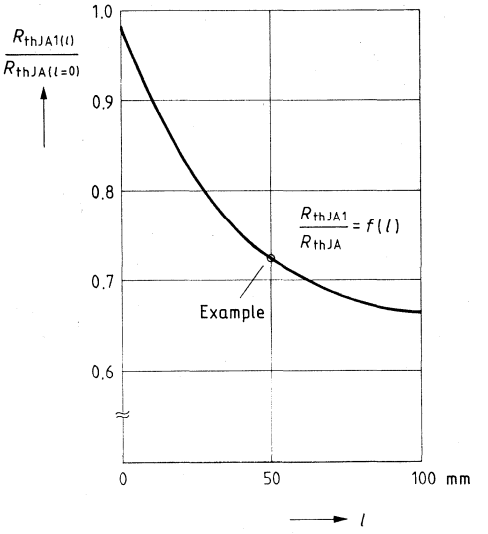
Output voltage V_2 (mains change)



Thermal resistance (only applicable to TDA 4600-2 D)

Standardized, ambience-related thermal resistance $R_{th\ JA\ 1}$ versus lateral length l of a square cooper-clad cooling area (35 µm copper lamination).

$R_{th\,JA}$ $(l = 0)$ = 60 K/W
T_{amb} = 70 °C
P_V = 1 W
PCB in vertical position
circuit in vertical position
static air



Pin configuration

Pin No.	Function
1	V_{ref} output
2	Zero passage identification
3	Input regulating amplifier, overload amplifier
4	Collector current simulation
5	Possible connection for additional protective circuit
6	Ground
7	DC voltage output for charging the coupling capacitor
8	Pulse output – driving the switching transistor
9	Current supply input

only applicable to TDA 4600-2D

10	interconnected (ground)
11	
12	
13	
14	
15	
16	
17	
18	

Bipolar circuit

Type	Ordering code	Package outline
TDA 4610	Q67000-A1523	SIP 3

The TDA 4610 is used for pincushion correction in color TV sets. Moreover, the circuit offers the possibility of performing trapezoidal corrections as well as setting the picture width and the degree of the pincushion correction. By making use of the switching operation, the diode modulation is controlled directly, thus resulting in very low power dissipation.

Features

- Low power dissipation
- Wide regulating range
- Simple tuning
- Few external components

Maximum ratings

Operating voltage	V_{S1}	36	V
Voltages			
Vertical input	V_7	V_{S1}	V
Parabola position	V_6	V_{S1}	V
Correction of parabola error	V_8	5	V
Correction onset	V_9	5	V
Flyback	V_4	42	V
Horizontal picture width	V_3	V_{S1}	V
Final stage output	V_{K2}	42	V
Current			
Final stage output	I_2	1.5	A
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (junction-case)	$R_{th\,JC}$	12	K/W
Thermal resistance (system-air)	$R_{th\,SA}$	70	K/W

Operating range

Supply voltage range	V_{S1}	12 to 36	V
Ambient temperature range	T_{amb}	0 to 70	°C

1. Characteristics ($V_{S1} = 24$ V; $T_{amb} = 25$ °C)

		min	typ	max	
Current consumption	I_5		10	12	mA
Input current vertical	$-I_7$		100		µA
Input current parabola position	$-I_6$		100		µA
No-load voltage parabola position	V_8		0.7		V
Input current	$-I_8$		0.4		mA
No-lad voltage correction onset	V_9		3.6		V
Input current correction onset	$-I_9$		0.4		mA
Input current picture width	I_3		0.2		mA
Saturation voltage final stage ($I_2 = 1$ A)	V_2		2.0	2.5	V

2. Characteristics ($V_{K2} = 40$ V; $T_{amb} = 25$ °C)

Parabola position with R_6 (diagram 1)		±10			%
Parabola correction					
Onset point with R_9 (diagram 2)		75			%
Permissible deviation referred to onset point (diagram 2)				10	%
Intensity of parabola correction with R_8 increase of the parabola adjustable up to 0					
Parabola amplitude with R_4	$V_{PA\,pp}$	5		20	V
Useful voltage range of the parabola (parabola amplitude $V_{PA} = 5\ V_{pp}$)	V_P	2		40	V

Circuit description

The vertical sawtooth voltage (2 V_{pp} increasing from 0, flyback time < 0.1 ms) is applied to two differential amplifiers.

Antiphase signals are available at the outputs of the differential amplifiers. The differential amplifier 1 controls the multiplexer which converts the sawtooth signal into a symmetrical parabola.

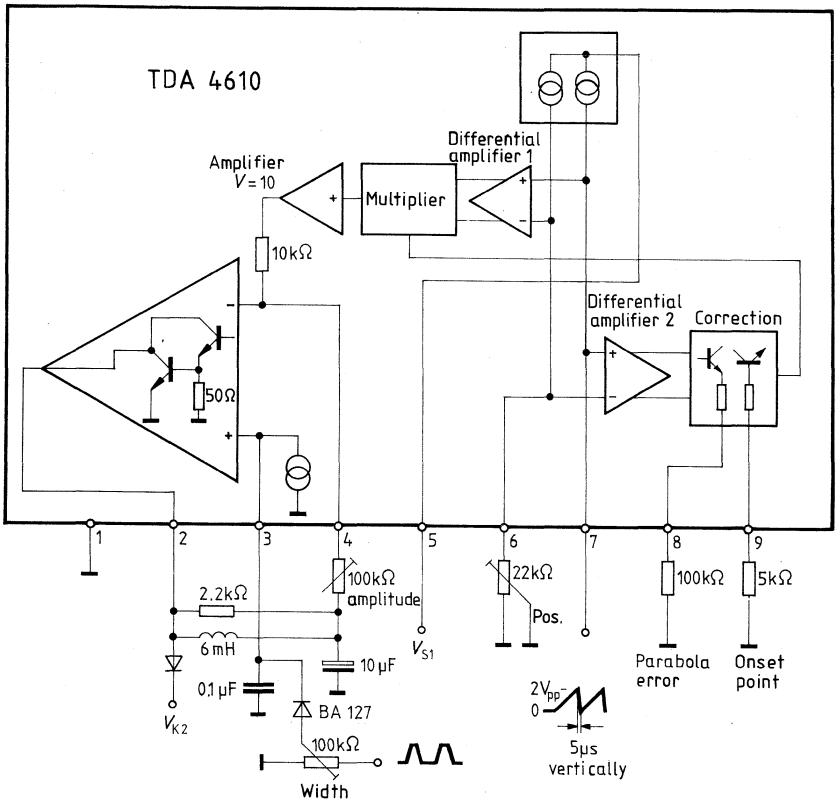
The differential amplifier 2 controls a correction voltage circuit by which the shape of the parabola can be adjusted to suit the characteristics of the tube.

The parabola signal is amplified and fed to the pulse width modulator. The modulator controls the final output transistor.

Pin configuration

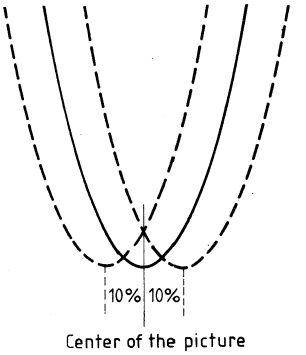
Pin No.	Function
1	Ground
2	Final stage output
3	Horizontal picture width
4	Flyback
5	Supply voltage
6	Parabola position adjustment
7	Vertical input
8	Correction of parabola error
9	Adjustment of onset point

Block diagram and test circuit

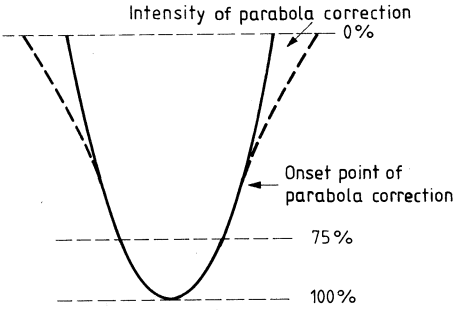


Pulse diagrams 1 and 2

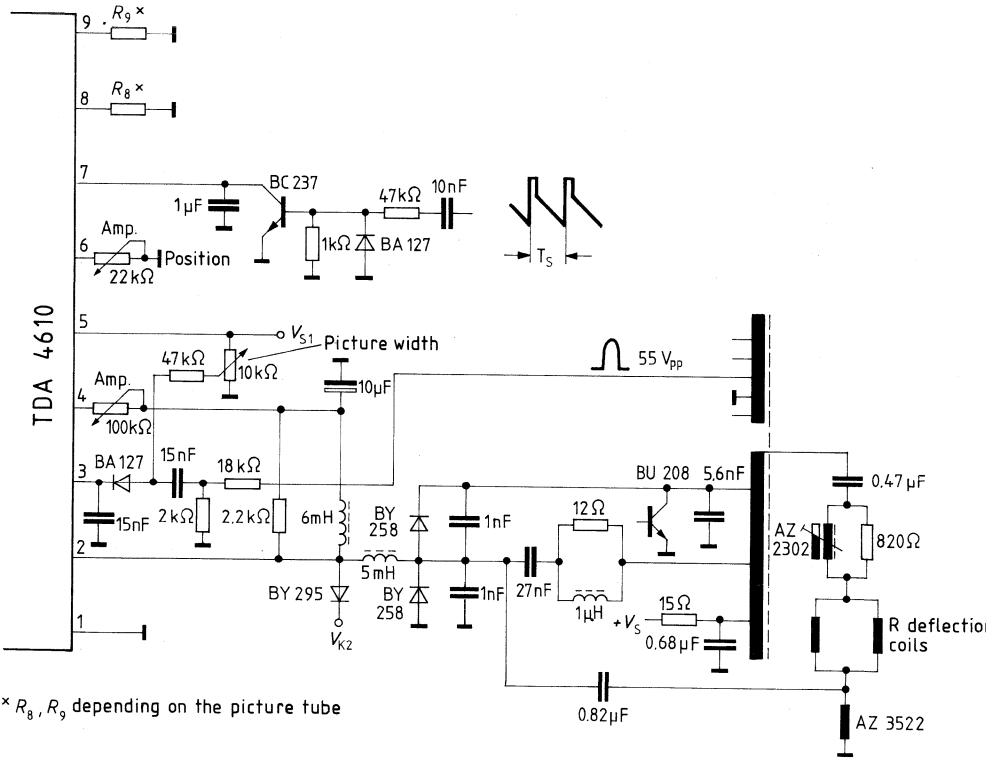
Parabola position



Parabola correction



Application circuit



× R_8, R_9 depending on the picture tube

Bipolar circuit

Type	Ordering code	Package outline
TDA 4920	Q67000-A1846	SIP 9

The TDA 4920 can be applied as a class B stereo amplifier or mono amplifier in bridge configuration for AF signals and as power op amp. In addition, the component is provided with a protective circuitry against overtemperature and overload.

Features

- Double op amp as AF power amplifier
- Universal application as stereo or bridge amplifier
- Wide supply voltage range
- Minimal external components
- Outputs AC and DC short-circuit-proof
- Integrated feedback

Maximum ratings

Supply voltage	V_5	18	V
Output peak current (not periodic)	$I_{q1,9}$	2.5	A
Output peak current (periodic)	$I_{q1,9}$	2	A
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	–20 to 135	°C
Thermal resistance (system-air)	$R_{th\,SA}$	70	K/W
(system-case)	$R_{th\,SC}$	12	K/W

Operating range

Supply voltage range	V_S	3.5 to 13.5	V
Voltage gain	G_V	25 to 40	dB
Ambient temperature range	T_{amb}	–20 to 85	°C

Characteristics ($V_S = 6$ V; $T_{amb} = 25$ °C)

		min	typ	max	
Quiescent current	I_5		17	25	mA
Output offset voltage	$V_{1\text{-}9}$			±50	mV
Input resistance	$R_3; R_7$		100		kΩ
Voltage gain stereo	G_V		40		dB
Voltage gain bridge	G_V		40		dB
Output power stereo ($f = 1$ kHz; $G_V = 40$ dB; $R_L = 2\ \Omega$)					
$THD = 10\%$	$P_{1,9}$	1.1	1.2		W
$THD = 1\%$	$P_{1,9}$	0.9	1.0		W
Output power bridge ($f = 1$ kHz; $G_V = 40$ dB; $R_L = 4\ \Omega$)					
$THD = 10\%$	$P_{1\text{-}9}$	2.2	2.3		W
$THD = 1\%$	$P_{1\text{-}9}$	1.8	1.9		W
Line hum suppression ($R_L = 2\ \Omega$; $R_S = 10$ kΩ; $f_{hum} = 100$ Hz; $V_{hum} = 0.5$ V)	a_{hum}		37		dB
Current consumption ($R_L = 2\ \Omega$; $f = 1$ kHz; $P_1 = P_9 = 1.2$ W)	$I_{5\,tot}$		720		mA
Efficiency ($f = 1$ kHz; $R_L = 2\ \Omega$; $P_1 = P_9 = 1.2$ W)	η		56		%
Total harmonic distortion ($f = 40$ Hz to 10 kHz; $G_V = 40$ dB; $P_1 = P_9 = 0.05$ to 0.9 W)	THD		0.5	1.0	%
Input sensitivity ($G_V = 40$ dB; $f = 1$ kHz; $R_L = 2\ \Omega$; $P_1 = P_9 = 0.5$ W)	V_i		10		mV
Cross talk attenuation ($f = 1$ kHz; $G_V = 40$ dB; P_1 or $P_9 = 1.2$ W)	a_{CR}		50		dB
Transmission range (−3 dB)			40 Hz to 50 kHz		
Disturbance voltage ($B = 30$ Hz to 20 kHz) in acc. with DIN 45405 with reference to input $R_L = 2\ \Omega$; $R_S = 10$ kΩ	V_d		5.5		μV
Noise voltage (CCIR-filter)	V_n		15		μVs

Characteristics ($V_S = 9$ V; $T_{amb} = 25$ °C)

		min	typ	max	
Quiescent current	I_5		18	28	mA
Output offset voltage	V_{1-9}			±50	mV
Input resistance	$R_3; R_7$		100		kΩ
Voltage gain stereo	G_V		40		dB
Voltage gain bridge	G_V		40		dB
Output power stereo ($f = 1$ kHz; $G_V = 40$ dB; $R_L = 4\ \Omega$)					
$THD = 10\%$	$P_{1,9}$	1.9	2.0		W
$THD = 1\%$	$P_{1,9}$	1.4	1.5		W
Output power stereo ($f = 1$ kHz; $G_V = 40$ dB; $R_L = 2\ \Omega$)					
$THD = 10\%$	$P_{1,9}$	2.8	3.0		W
$THD = 1\%$	$P_{1,9}$	2.3	2.5		W
Output power bridge ($f = 1$ kHz; $G_V = 40$ dB; $R_L = 8\ \Omega$)					
$THD = 10\%$	P_{1-9}	3.6	3.8		W
$THD = 1\%$	P_{1-9}	2.8	3.0		W
Output power bridge ($f = 1$ kHz; $G_V = 40$ dB; $R_L = 4\ \Omega$)					
$THD = 10\%$	P_{1-9}	5.8	6.0		W
$THD = 1\%$	P_{1-9}	4.8	5.0		W
Line hum suppression ($R_L = 4\ \Omega$; $R_S = 10$ kΩ; $f_{hum} = 100$ Hz; $V_{hum} = 0.5$ V)	a_{hum}		37		dB
Current consumption ($R_L = 2\ \Omega$; $f = 1$ kHz; $P_1 = P_9 = 3$ W)	$I_{5\,tot}$		1.05		A
Efficiency ($f = 1$ kHz; $R_L = 2\ \Omega$; $P_1 = P_9 = 3$ W)	η		63		%
Total harmonic distortion ($f = 40$ Hz to 10 kHz; $G_V = 40$ dB; $P_1 = P_9 = 0.05$ to 2 W; $R_L = 2\ \Omega$)	THD		0.5	1.0	%
Input sensitivity ($G_V = 40$ dB; $f = 1$ kHz; $R_L = 2\ \Omega$; $P_1 = P_9 = 1$ W)	V_i		14.1		mV
Cross talk attenuation ($f = 1$ kHz; $G_V = 40$ dB; P_1 (P_9) = 3 W at 2 Ω)	a_{CR}		50		dB
Transmission range (−3 dB)			40 Hz to 50 kHz		
Disturbance voltage ($B = 30$ Hz to 20 kHz) in acc. with DIN 45405	V_d		5.5		μV
Noise voltage (CCIR-filter) with reference to input $R_L = 4\ \Omega$; $R_S = 10$ kΩ	V_n		15		μVs

Circuit description

The IC contains two complete amplifiers and can be used for a wide variety of applications with a minimum of external circuitry.

The TDA 4920 can be applied as stereo amplifier or amplifier in bridge configuration for operating voltages between 4 V and 17 V, with load impedance of greater than or equal to 1 Ω.

The prestages are differential amplifiers with extreme negative feedback (external offset equalization is possible). Internal frequency compensation in the driver amplifier limits the transmission range.

Thermal overload of the power output stage transistors is prevented by a temperature protective circuit in each amplifier.

The upper power element is equipped with an SOA protective circuit, rendering the outputs of the amplifiers AC and DC short-circuit-resistant.

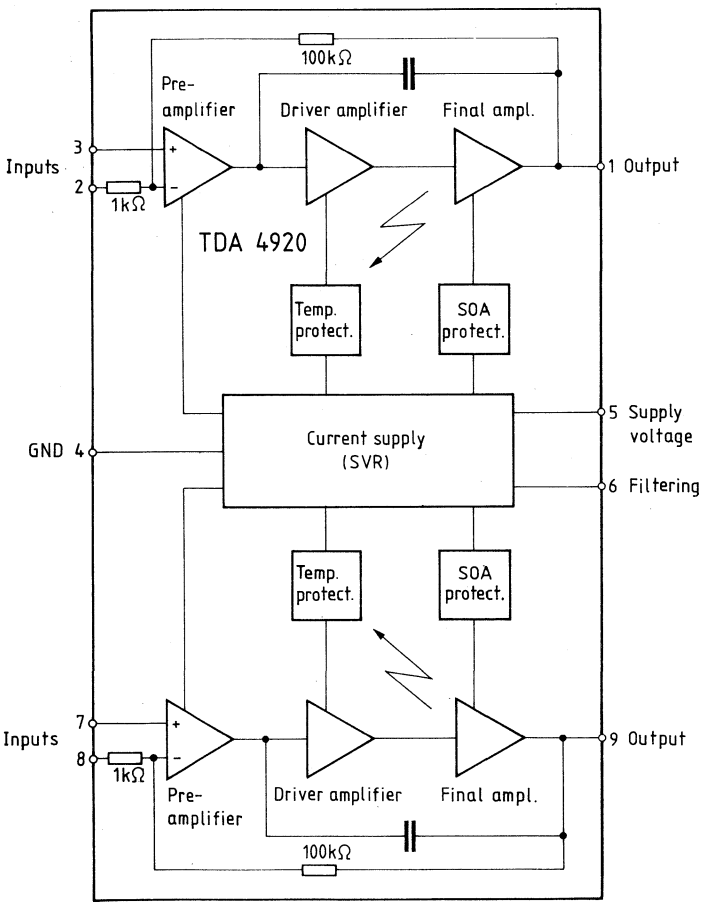
The switch-on behavior is optimized by internal circuitry and is almost independent of the generator resistance.

An integrated feedback divider from 100 kΩ to 1 kΩ sets the amplification to typically 40 dB.

Should the user require an amplification lower than 40 dB (min. permissible amplification is 25 dB), stereo operation allows an additional external feedback resistor R_F to be connected in series to the capacitor at pin 8.

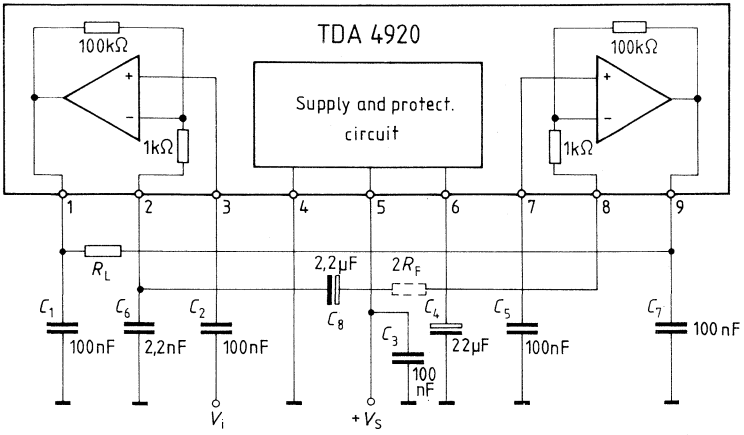
In case of bridge operation, that resistor has 2 R_F and lies between pins 8 and 2 in series to the capacitor.

Block diagram



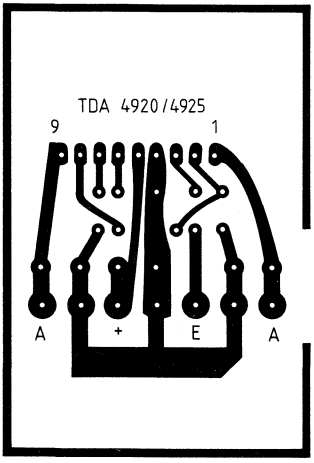
Test and application circuit

Bridge operation

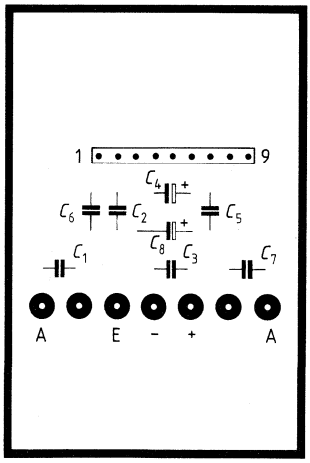


V_S	6 V	9 V	12 V
R_L	4 Ω	4 Ω	8 Ω

Layout

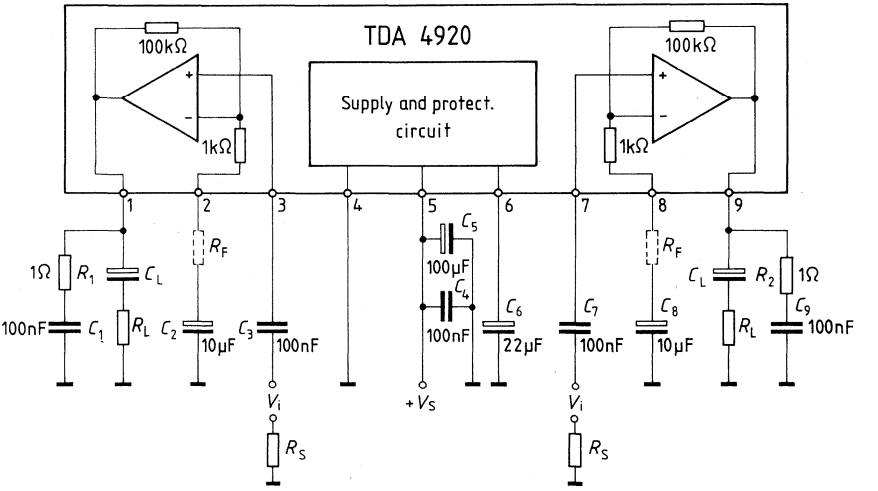


Plug-in location plan



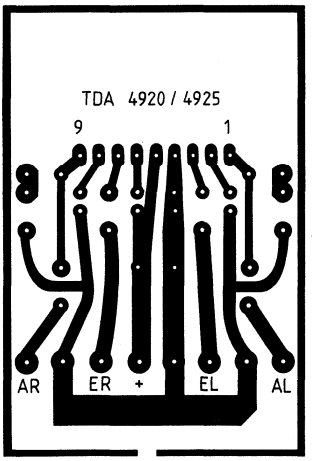
Test and application circuit

Stereo operation

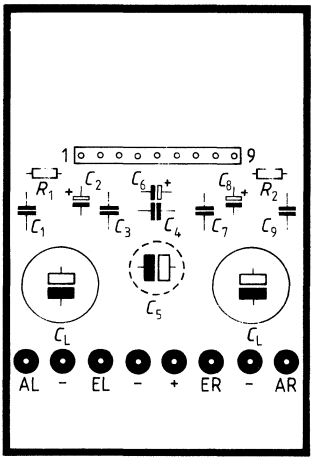


V_S	6 V	9 V	12 V
R_L	2 Ω	2 Ω	4 Ω
C	2200 µF	2200 µF	1000 µF

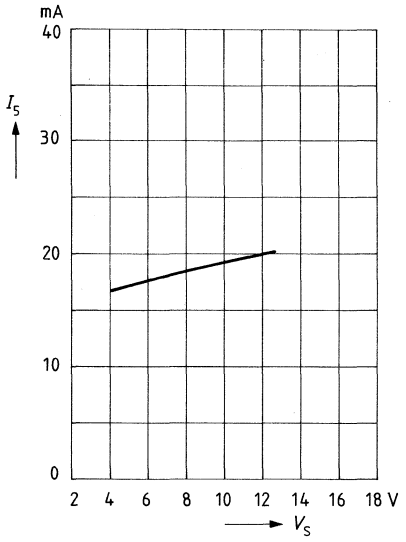
Layout



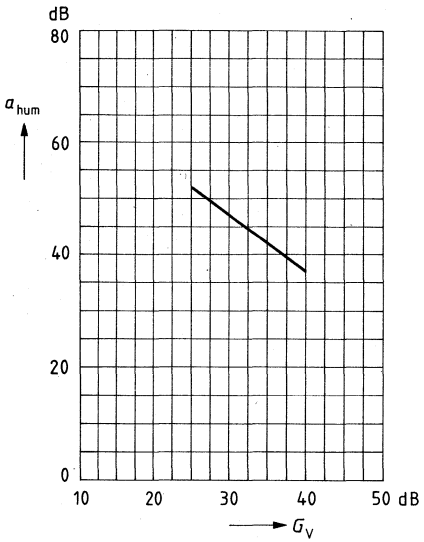
Plug-in location plan



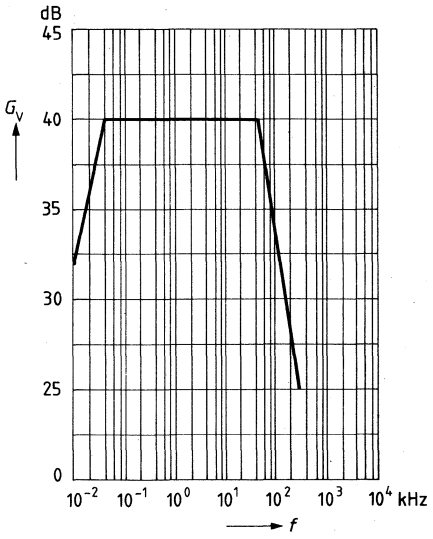
Quiescent current versus supply voltage



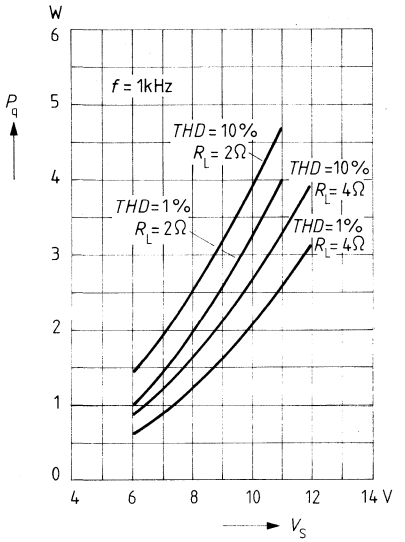
Line hum suppression versus voltage gain



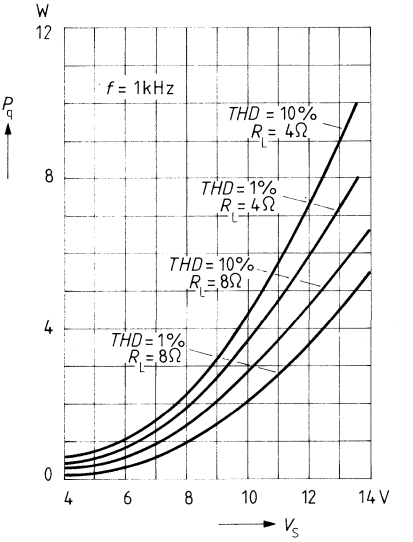
Voltage gain versus frequency



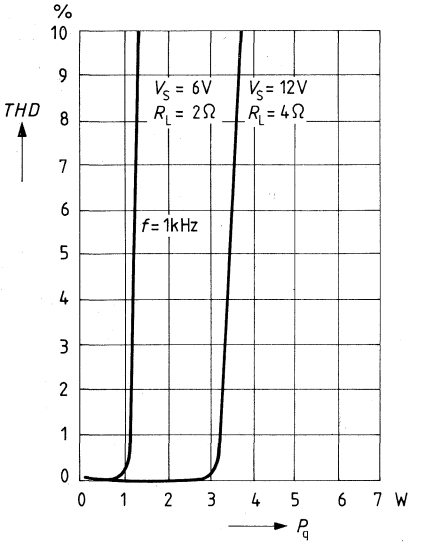
Stereo operation
Output power versus supply voltage



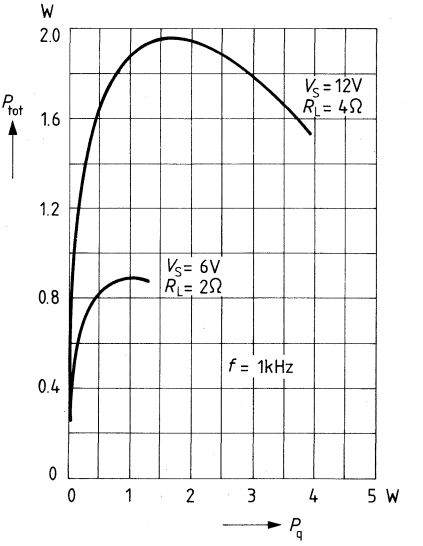
Bridge operation
Output power versus supply voltage



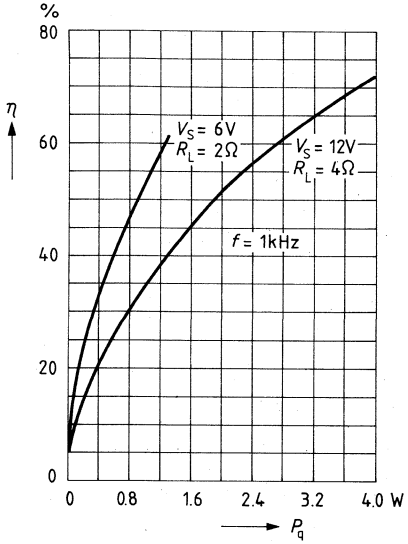
Stereo operation
Distortion factor versus output power



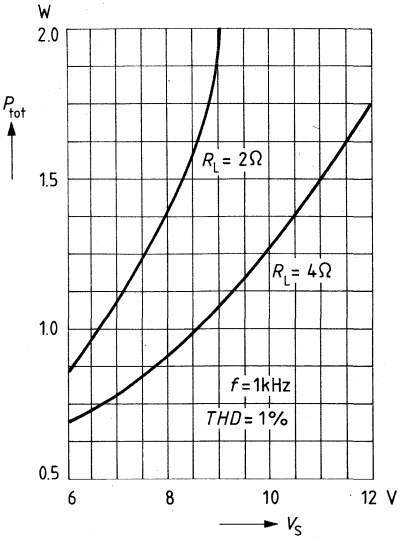
Stereo operation
Total power dissipation versus output power



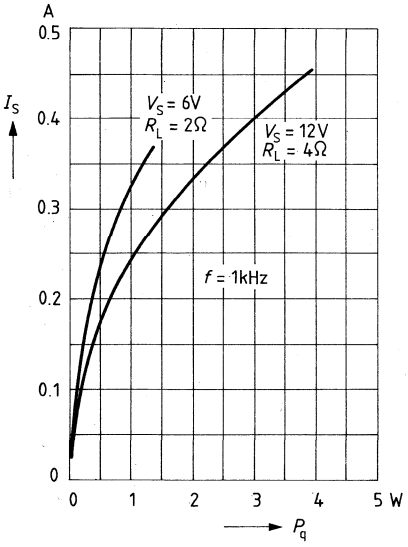
Stereo operation
Efficiency versus output power



Total power dissipation versus supply voltage



Supply current versus output power



Bipolar circuit

Type	Ordering code	Package outline
TDA 4925	Q67000-A1893	SIP 9

The TDA 4925 can be applied as a class B stereo amplifier or mono amplifier in bridge configuration for AF signals and as power op amp. In addition, the component is provided with a protective circuitry against overtemperature and overload.

Features

- Double op amp as AF power amplifier
- Universal application as stereo or bridge amplifier
- Wide supply voltage range
- Minimal external components
- Outputs AC and DC short-circuit-proof
- Integrated feedback

Maximum ratings

Supply voltage	V_5	25	V
Supply voltage ($t \leqq 50$ ms)	V_5	36	V
Output peak current (not periodic)	$I_{q\,1,9}$	2.5	A
Output peak current (periodic)	$I_{q\,1,9}$	2	A
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	–20 to 135	°C
Thermal resistance (system-air)	$R_{th\,SA}$	70	K/W
(system-case)	$R_{th\,SC}$	12	K/W

Operating range

Supply voltage range	V_5	3.5 to 17	V
Voltage gain	G_V	25 to 40	dB
Ambient temperature range	T_{amb}	–20 to 85	°C

Characteristics ($V_S = 14.4$ V; $T_{amb} = 25$ °C)

		min	typ	max	
Quiescent current	I_5		20	30	mA
Output offset voltage	$V_{1\text{-}9}$			±50	mV
Input resistance	$R_{i3}; R_{i7}$		100		kΩ
Voltage gain stereo	G_V		40		dB
Voltage gain bridge	G_V		40		dB
Output power stereo ($f = 1$ kHz; $G_V = 40$ dB; $R_L = 4\ \Omega$)					
$THD = 10\%$	$P_{1,9}$	5.0	5.2		W
$THD = 1\%$	$P_{1,9}$	4.1	4.3		W
Output power bridge ($f = 1$ kHz; $G_V = 40$ dB; $R_L = 8\ \Omega$)					
$THD = 10\%$	$P_{1\text{-}9}$	9.8	10.1		W
$THD = 1\%$	$P_{1\text{-}9}$	8.2	8.4		W
Line hum suppression ($R_L = 4\ \Omega; R_S = 10$ kΩ; $f_{hum} = 100$ Hz; $V_{hum} = 0.5$ V)	a_{hum}		37		dB
Current consumption ($R_L = 4\ \Omega; f = 1$ kHz; $P_1 = P_9 = 5.2$ W)	$I_{5\,tot}$		1		A
Efficiency ($f = 1$ kHz; $R_L = 4\ \Omega; P_1 = P_9 = 5.2$ W)	η		72		%
Total harmonic distortion ($f = 40$ Hz to 10 kHz; $G_V = 40$ dB; $P_1 = P_9 = 0.05$ to 4.1 W)	THD		0.5	1.0	%
Input sensitivity ($G_V = 40$ dB; $f = 1$ kHz; $R_L = 4\ \Omega$; $P_1 = P_9 = 4$ W)	V_i		40		mV
Cross talk attenuation ($f = 1$ kHz; $G_V = 40$ dB; P_1 or $P_9 = 5.2$ W)	a_{CR}		60		dB
Transmission range (−3 dB)		40 Hz to 50 kHz			
Disturbance voltage ($B = 30$ Hz to 20 kHz) in acc. with DIN 45405	V_d		5.5		μV
Noise voltage (CCIR-filter) with reference to input $R_L = 4\ \Omega; R_S = 10$ kΩ	V_n		12	15	μVs

Circuit description

The IC contains two complete amplifiers and can be used for a wide variety of applications with a minimum of external circuitry.

The TDA 4925 can be applied as stereo amplifier or amplifier in bridge configuration for operating voltages between 4 V and 17 V, with load impedances of greater than or equal to 1 Ω. The prestages are differential amplifiers with extreme negative feedback (external offset equalization is possible.) Internal frequency compensation in the driver amplifier limits the transmission range.

Thermal overload of the power output stage transistors is prevented by a temperature protective circuit in each amplifier.

The upper power element is equipped with an SOA protective circuit, rendering the outputs of the amplifiers AC and DC short-circuit-resistant.

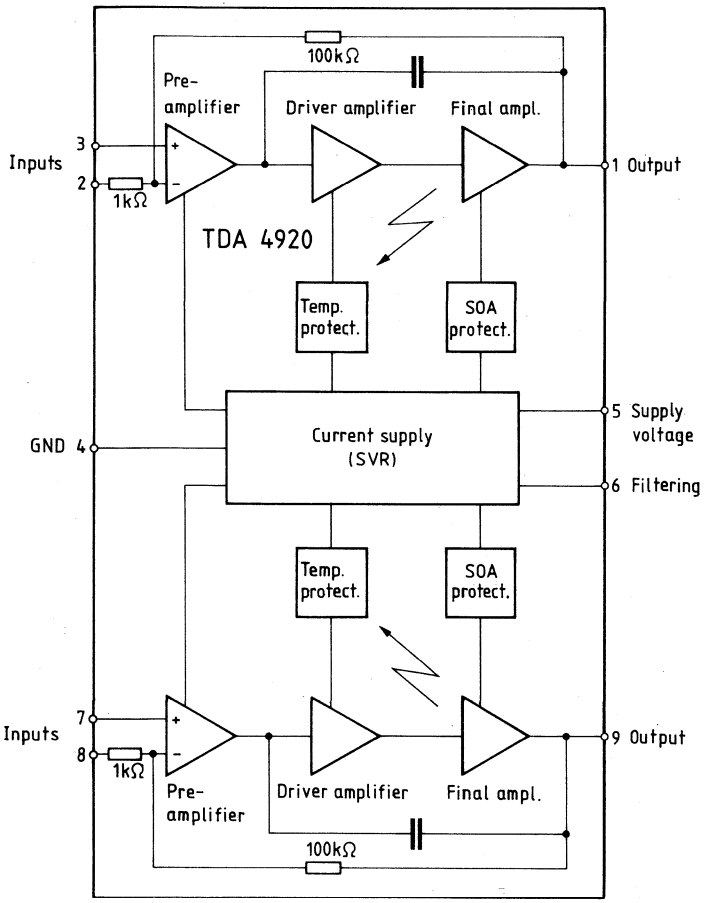
The switch-on- behavior is optimized by internal circuitry and is almost independent of the generator resistance.

An integrated feedback divider from 100 kΩ to 1 kΩ sets the amplification to typically 40 dB.

Should the user require an amplification lower than 40 dB (min. permissible amplification is 25 dB), stereo operation allows an additional external feedback resistor R_F to be connected in series to the capacitor at pin 8.

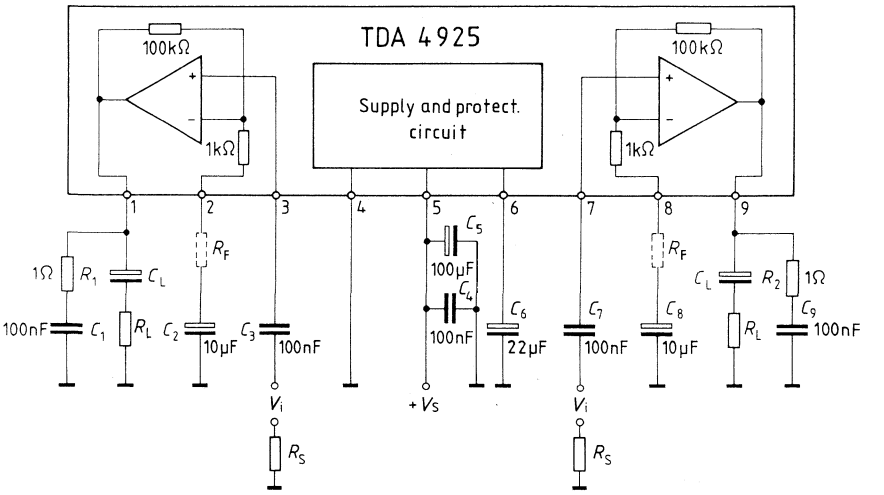
In case of bridge operation, that resistor has 2 R_F and lies between pins 8 and 2 in series to the capacitor.

Block diagram



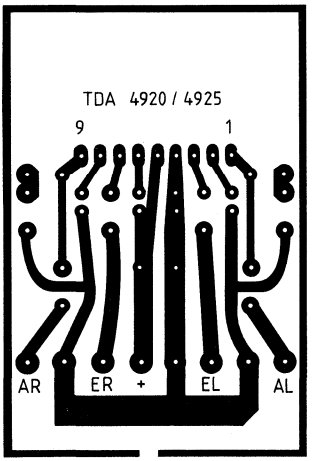
Test and application circuit

Stereo operation

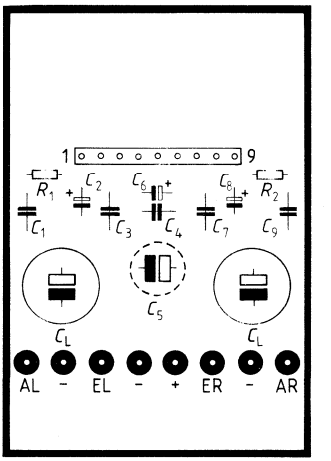


V_S	14.4 V
R_L	4 Ω
C	1000 µF

Layout

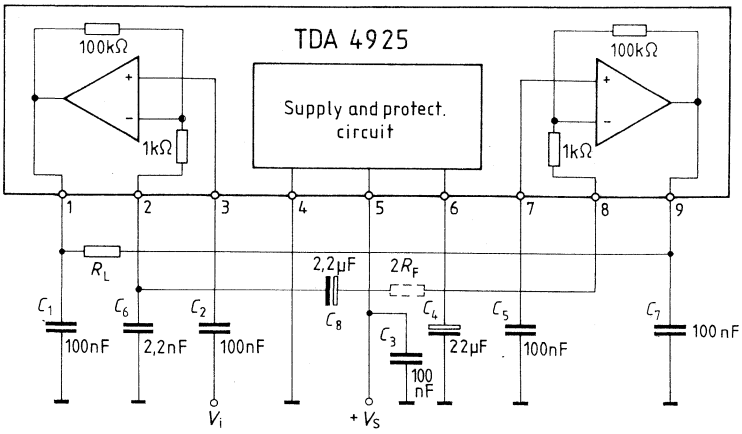


Plug-in location plan



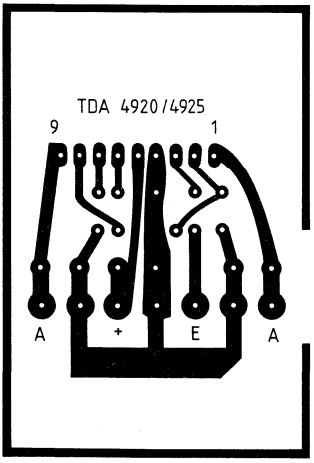
Test and application circuit

Bridge operation

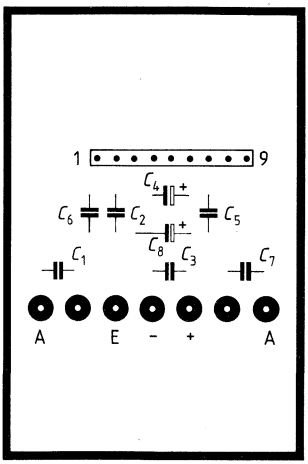


V_S	14.4 V
R_L	8 Ω

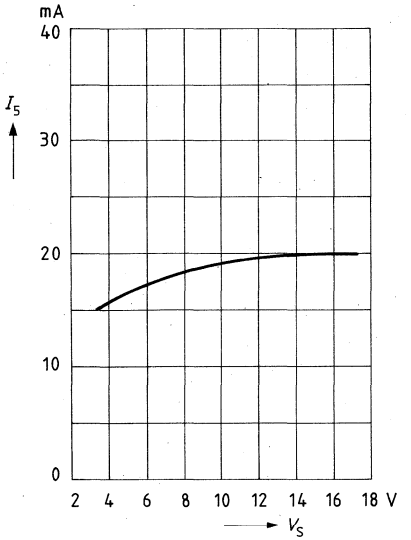
Layout



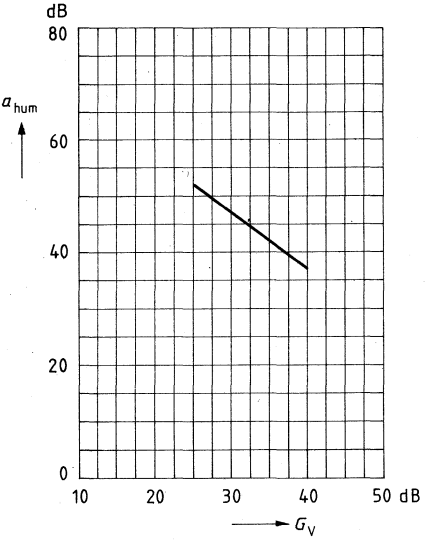
Plug-in location plan



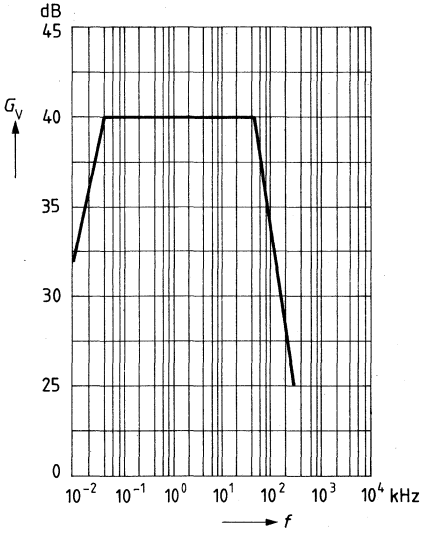
Quiescent current versus supply voltage



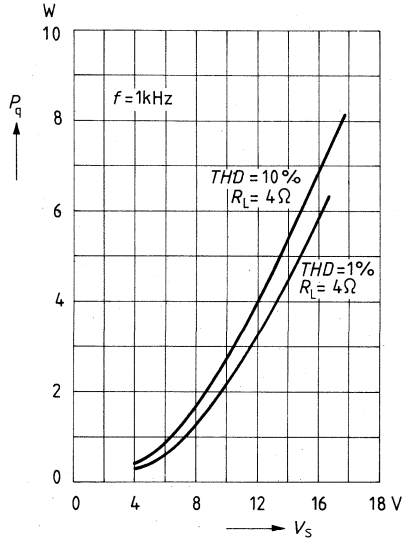
Line hum suppression versus voltage gain



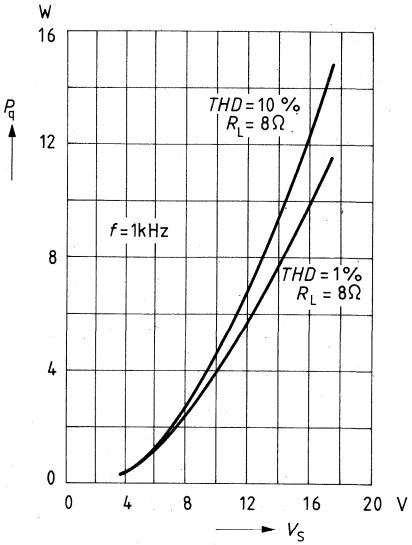
Voltage gain versus frequency



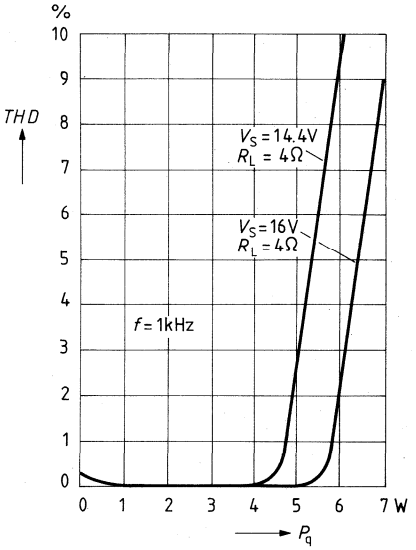
Stereo operation
Output power versus supply voltage



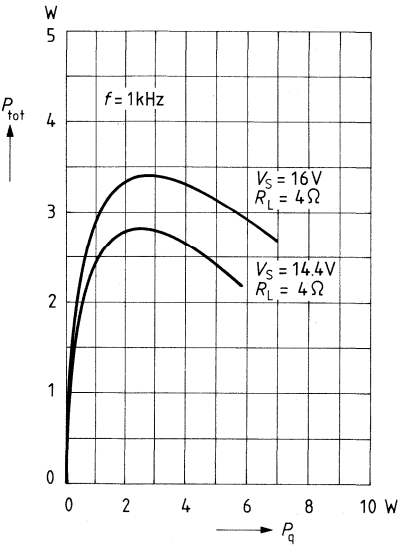
Bridge operation
Output power versus supply voltage



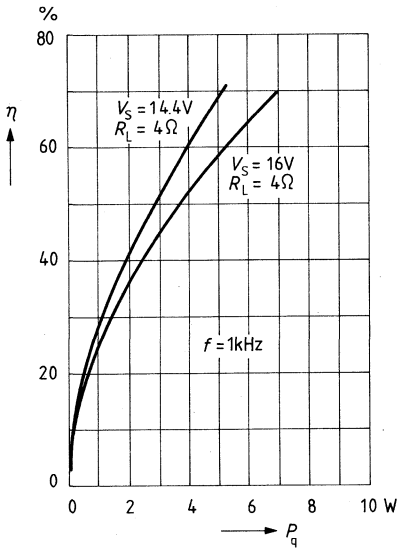
Stereo operation
Distortion factor versus
output power



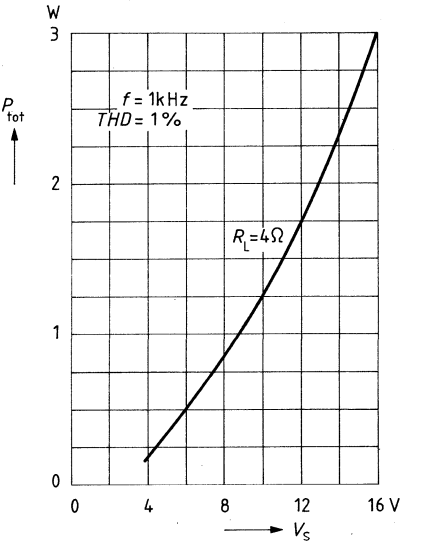
Stereo operation
Total power dissipation versus
output power



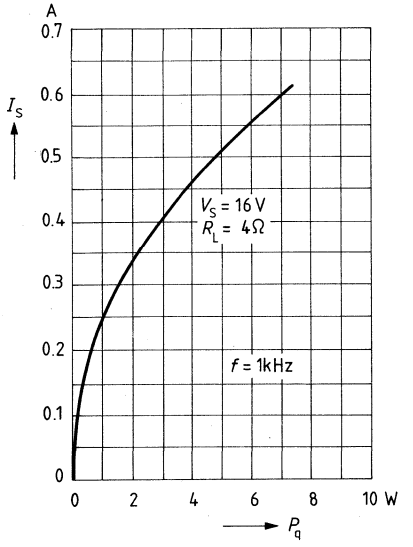
Stereo operation
Efficiency versus output power



Total power dissipation versus supply voltage



Supply current versus output power



Preliminary data **Bipolar circuit**

Type	Ordering code	Package outline
TDA 4930	Q67000-A2156	SIP 9

The TDA 4930 can be applied as a class B stereo amplifier or mono amplifier in bridge configuration for AF signals. In addition, the component is provided with a protective circuitry against overtemperature and overload.

Features

- Universal application as stereo amplifier or mono amplifier in bridge configuration
- Wide supply voltage range
- Minimal external components
- Outputs AC and DC short-circuit-resistant

Maximum ratings

Supply voltage	V_S	32	V
Output peak current	I_1; I_9	2.5	A
Input voltage	V_2; V_3; V_7	−0.3 to V_S	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−50 to 150	°C
Thermal resistance (system-case)	$R_{th\,JC}$	6	K/W

Operating range

Supply voltage range	V_S	8 to 26	V
Package temperature range	T_C	−20 to 85	°C

Characteristics ($V_S = 19$ V; $T_{amb} = 25$ °C)

		*	min	typ	max	
Quiescent current ($V_i = 0$)	I_5	1		30	60	mA
Output voltage ($V_i = 0$)	$V_{9(1)}$	1	9.0	9.5	10.8	V
Input resistance[1]	$R_{7(3)}$	1		20		Ω
Output power ($f = 1$ kHz)						
– stereo operation						
$THD = 1\%$	$P_{9(1)}$	1	7	8		W
$THD = 10\%$		1	9	10		W
– bridge operation						
$THD = 1\%$	$P_{9(1)}$	2	14	16		W
$THD = 10\%$		2	18	20		W
Line hum suppression[2]	a_{hum}	1	40	46		dB
$f_r = 100$ Hz; $V_r = 0.5$ V						
Current consumption	I_5	1		1.5		A
$P_9 = P_1 = 10$ W; $f = 1$ kHz						
Efficiency	η	1		70		%
$P_9 = P_1 = 10$ W; $f = 1$ kHz						
Total harmonic distortion	THD	1		0.2	0.5	%
$P_{9(1)} = 0.05$ to 6 W						
$f = 40$ Hz to 15 kHz						
Cross-talk attenuation	a_{CR}	1		50		dB
$f = 1$ kHz; P_9 or $P_1 = 10$ W						
Transmission range[3]	B		40 Hz to 60 kHz			
Disturbance voltage ($B = 30$ Hz to 20 kHz)	V_d	1		5		μV
in acc. with DIN 45405 referred to input[4]						
Noise voltage (CCIR filter)	V_n	1		15		μVs
in accordance with DIN 45405						
referred to the input[4]						
Difference in transmission measure	ΔG_V	1			1	dB
$P_9 = P_1 = 7$ W						
$f = 40$ Hz to 20 kHz						
Voltage gain stereo	G_V	1		30		dB
Voltage gain bridge configuration	G_V	2		36		dB
DC output voltage at	$V_{9(1)}$	2		0.15	0.30	V
active DC protection						
if $S_{1(9)}$ is closed; $V_S \geqq 10$ V						

1) $S_{2a(b)}$ open/closed
2) $S_{1a(b)}$ and S_3 in position 2
3) $P_{9(1)} = 6$ W; −3 dB referred to 1 kHz
4) $S_{1a(b)}$ in position 2
*) No. of test circuit

Circuit description

The IC contains 2 complete amplifiers and can be used for a wide variety of applications with a minumim of external circuitry.

The TDA 4930 can be applied as stereo amplifier or amplifier in bridge configuration for operating voltages ranging between 8 V and 26 V, with speakerload impedance from 1 to 16 Ω.

The prestages are differential amplifiers with extreme, negative feedback. Internal frequency compensation in the driver amplifier limits the gain-bandwidth product to 4.5×10^6 Hz.

The power output stages are comprised of quasi-pnp transistors (small saturation voltage).

Each power element is equipped with an independent protective circuit, rendering the outputs of the amplifiers AC and DC short-circuit-resistant.

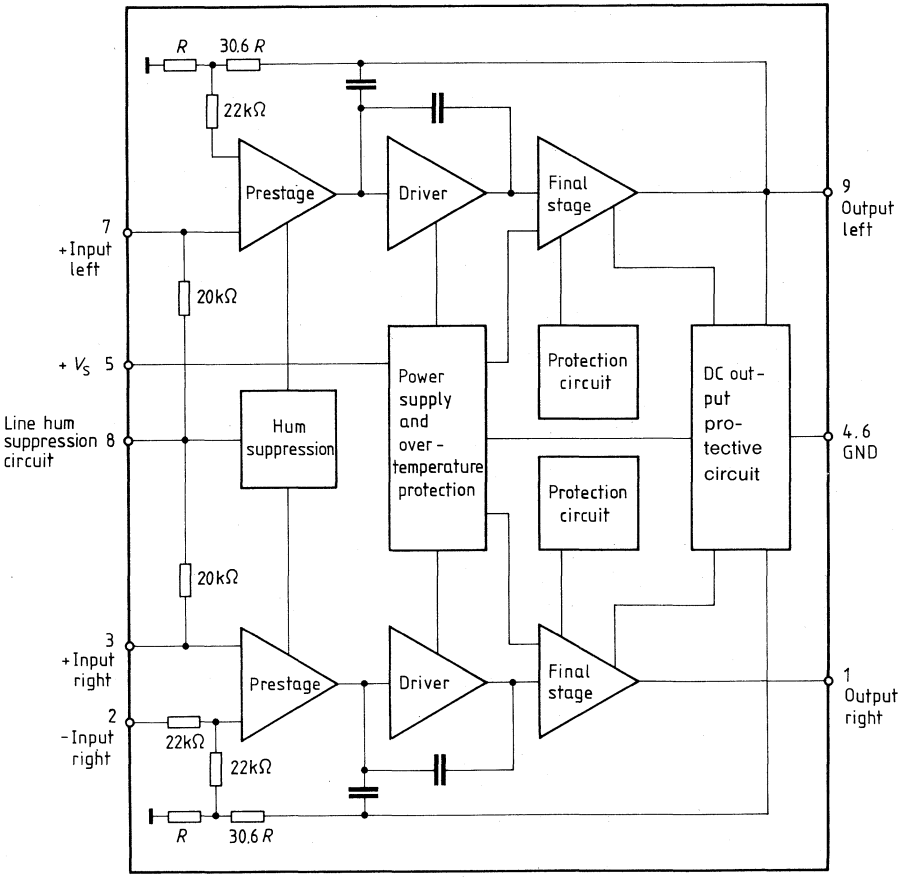
A DC protective circuit of the outputs prevents overloading of the loudspeakers, if ground connections become apparent during bridge operations. To avoid overheating, a temperature fuse affecting both amplifiers prevents current supply to the power output stages during inadmissibly high chip temperatures.

As a special economic feature, the negative feedback resistances for $G_v = 30$ dB and the input voltage reference divider have been integrated.

Pin configuration

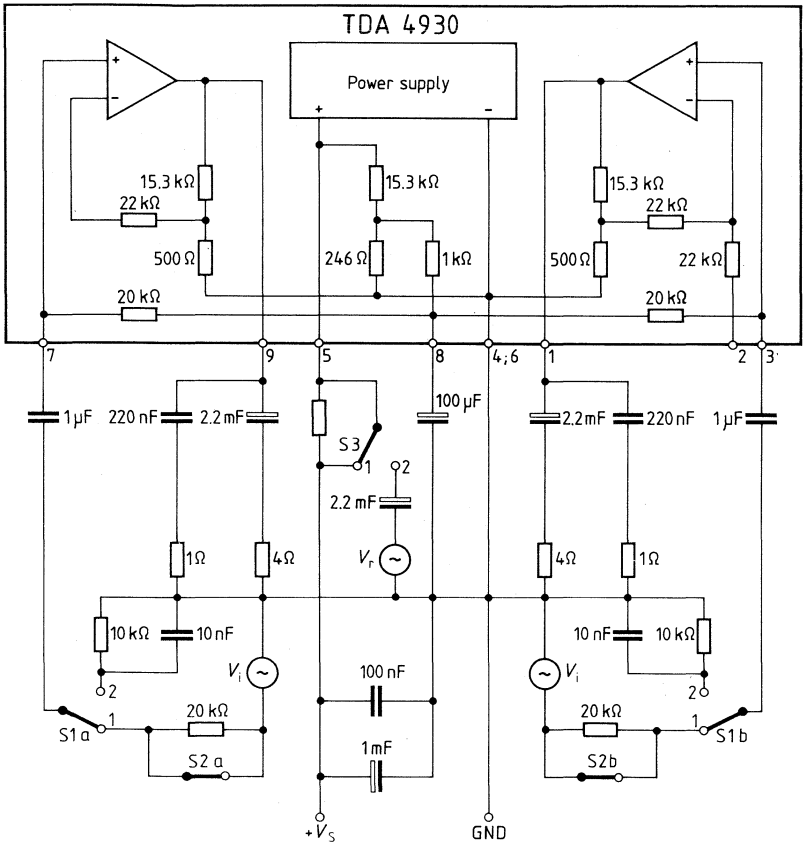
Pin No.	Function
1	Output right channel
2	Inverting input right channel (more than 22 kΩ)
3	Non-inverting input right channel
4	Ground
5	$+V_S$
6	Ground
7	Non-inverting input left channel
8	Line hum suppression right and left channel
9	Output left channel

Block diagram



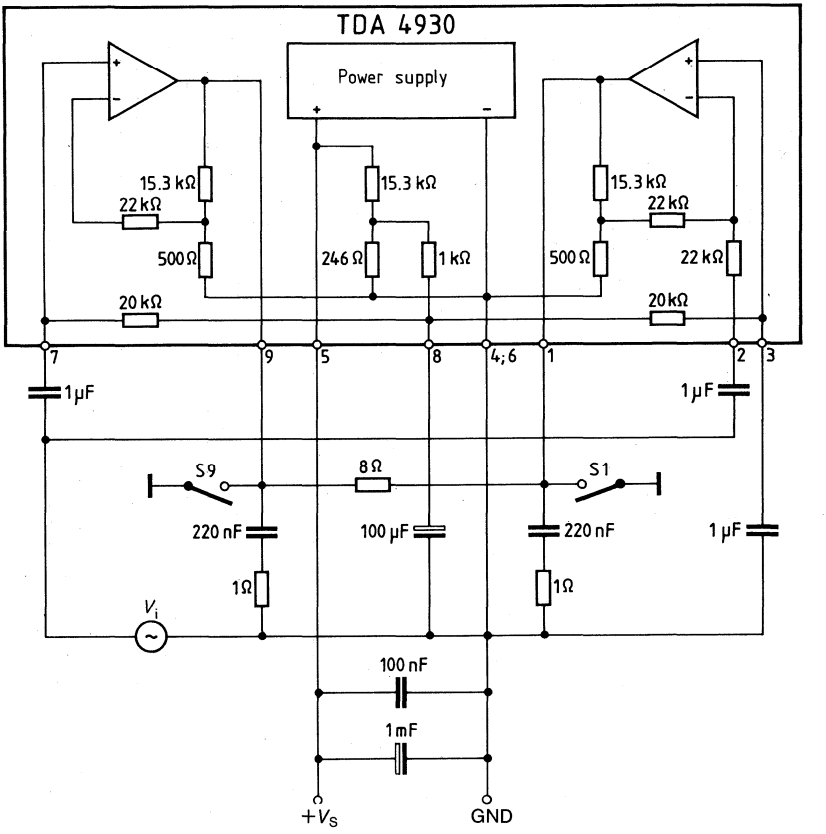
Test and measuring circuit

1. Stereo operation



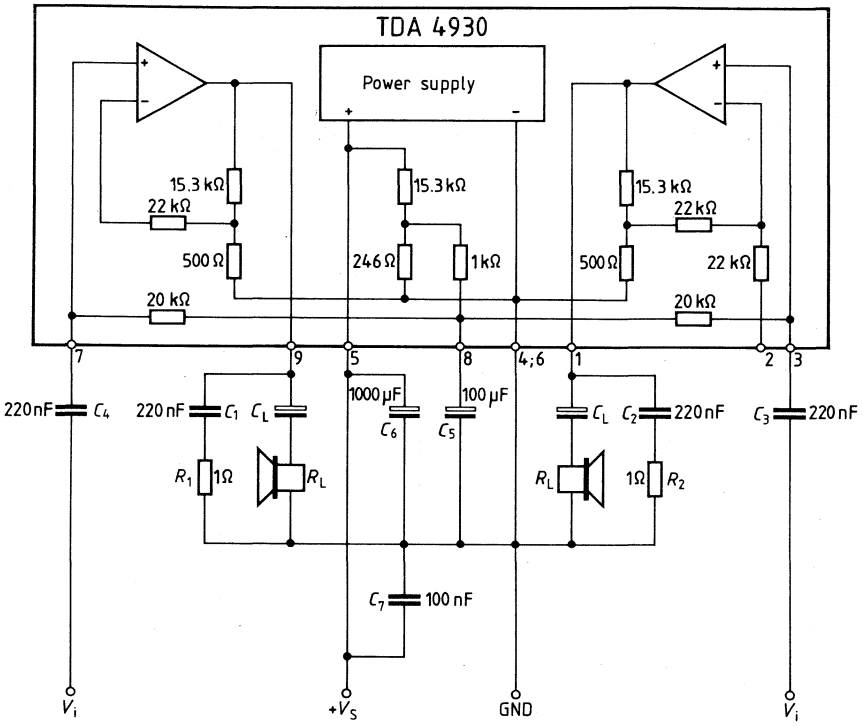
Test and measuring circuit

2. Bridge operation



Application circuit

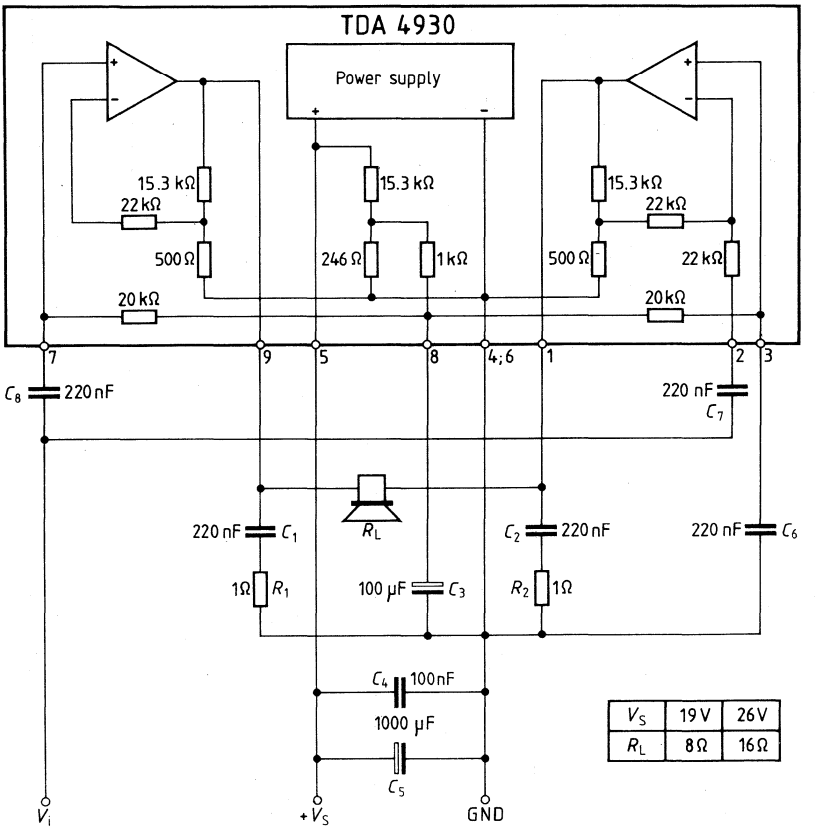
1. Stereo operation



V_S	19 V	26 V
R_L	4Ω	8Ω
C_L	1000µF	470µF

Application circuit

2. Bridge operation



V_S	19 V	26 V
R_L	8 Ω	16 Ω

FM IF Amplifier with Pilot Tone Decoding for TV Stereo Application

TDA 4940

Bipolar circuit

Type	Ordering code	Package outline
TDA 4940	Q67000-A1872	DIP 22

The TDA 4940 has been designed as an intercarrier FM-IF limiter amplifier. It includes a coincidence demodulator, an AF output and a decoding device. The decoding device is based on the two carrier system ("dual-channel audio") and decodes the pilot carriers during multi-channel audio as used in TV sets. In connection with the decoder components TDA 4941, TDA 4942 or TDA 4944, two different audio signals are available. It is possible to select the stereo tone mode or the original soundtrack, while on the second channel, the synchronization of the original soundtrack in e.g. another language will be available.

Features

- Good limiting characteristics
- PLL circuit, eliminates alignment of pilot tone decoder
- Few external components

Maximum ratings

Supply voltage	V_S	16.5	V
Input voltage line flyback	V_{13}	V_S	V
Input voltage mono compulsory	V_7	V_S	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance	$R_{th\,SA}$	70	K/W

Operating range

Supply voltage	V_S	10 to 15.8	V
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics ($V_S = 12$ V; $T_{amb} = 25$ °C)

		min	typ	max	
Total current consumption	I_{S8}	16	26	34	mA
Reference voltage	V_{ref5}	5.2	6	6.8	V
FM section ($f_{IF} = 5.74$ MHz; $Q_B \approx 25$; $V_{iIF} = 1$ mV; $\Delta f = \pm 30$ kHz; $f_{mod} = 1$ kHz)					
Limiting use	$V_{lim\ rms}$		20	40	µV
Input resistance	R_{i2-3}	600	800	1000	Ω
AM suppression ($m = 30\%$)	a_{AM}		42		dB
Signal-to-noise ratio ($V_{iIF} = 10$ mV)	$a_{S/N}$		85		dB
Total harmonic distortion	THD		1	3	%
Demodulator input resitance	R_{i19-20}	4	5.4	7	kΩ
AF output voltage ($\Delta f = 12.5$ kHz)	$V_{q18\ rms}$	200	300	400	mV
AF output resistance	R_{q18}		100		Ω
Pilot carrier decoding					
Output voltage stereo	V_6	10.5		V_S	V
mono	V_6		6		V
dual audio	V_6	0		1.5	V
Input mono compulsory low	V_7	0		0.7	V
high	V_7	1.3		V_S	V
pulse width	τ_H	500			µs
Input voltage line flyback	$V_{13\ pp}$	4.5		V_S	V
Input resistance	R_{i13}		33		kΩ

Circuit description

FM section

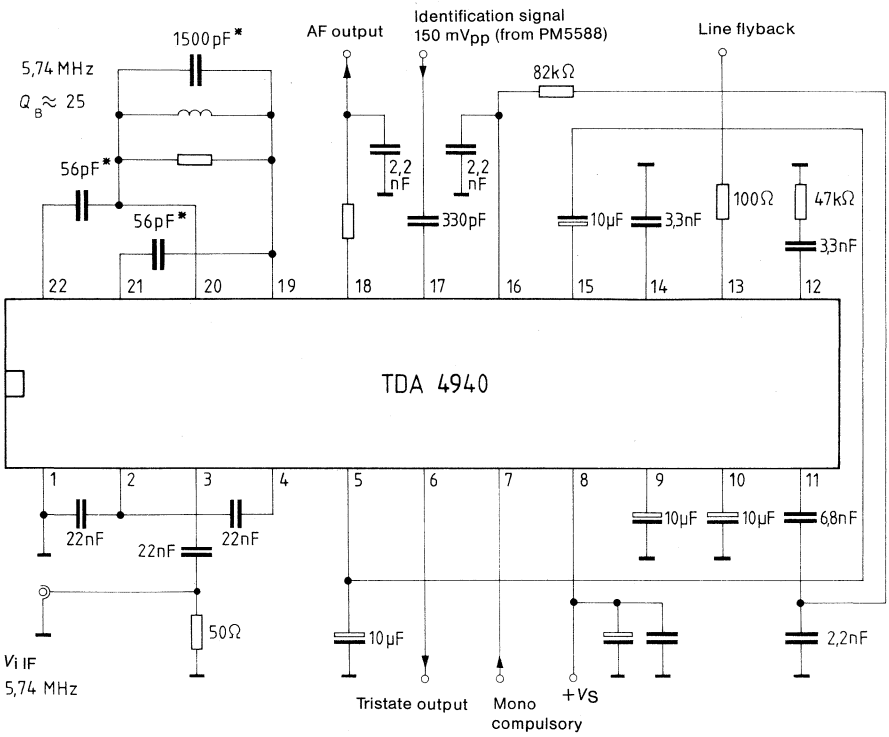
The TDA 4940 includes an 8 stage limiter amplifier, an FM coincidence demodulator as well as an AF output. Deemphasis is provided by an external *RC* circuit.

Pilot carrier decoding

A PLL synthesizer generates the pilot carrier frequency $f_p = 3.5 \times f_H$. The line flyback pulse is used as reference frequency. Via a high-pass filter, the modulated pilot carrier is routed from the AF output to the synchronous demodulator. However, the internal pilot carrier is synchronized with a phase regulating circuit. Via the external band-pass filter, the synchron-demodulated identifying signals are forwarded to the decoding circuit. Decoding is performed with a frequency-selective, phase-resistant RMS rectifier of very narrow bandwidth as well as a comparator. The "stereo" status ($f_{ST} = f_H/133$), as well as the "dual audio" ($f_{DT} = f_H/57$) and the "mono" status ($f_M = 0$) are evaluated during multiplex operations. The current operating status is provided via a tristate output. It is possible to set "mono" with a positive pulse edge at input 7.

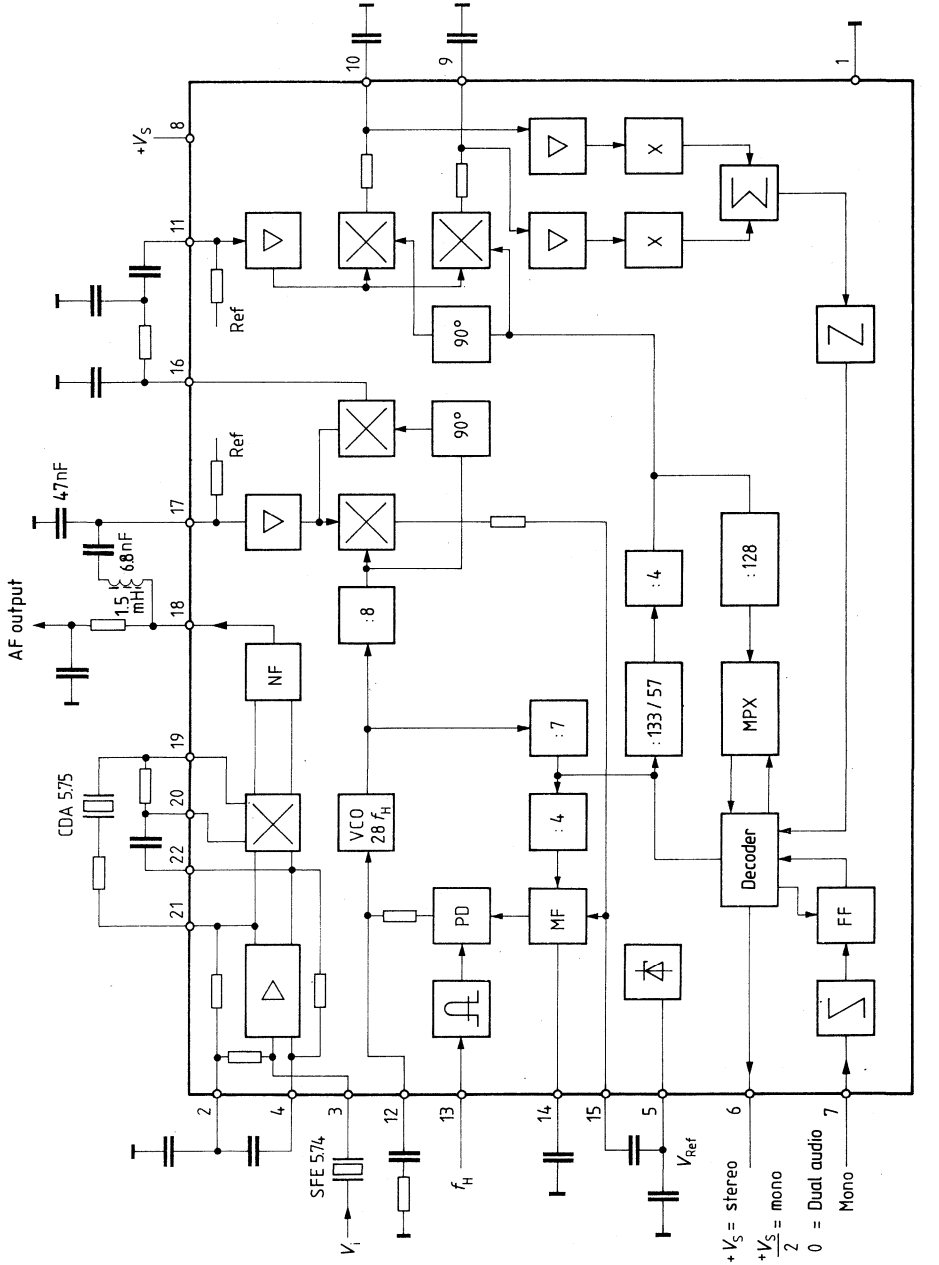
$f_{DT} = f_{ZT}$ = dual tone pilot carrier
f_{ST} = stereo tone pilot carrier
f_M = mono pilot carrier
f_H = horizontal deflection frequency

Test circuit

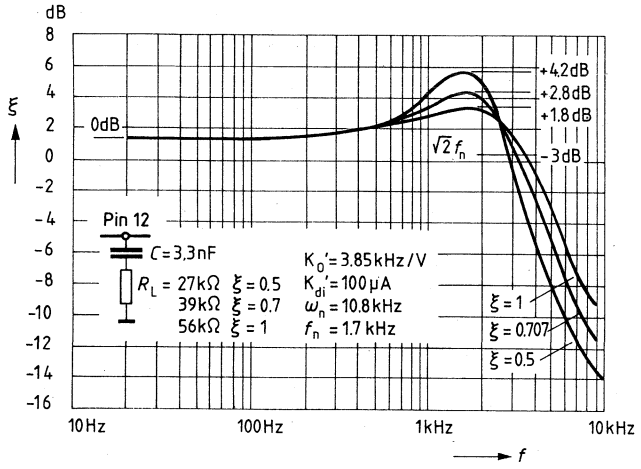


* STYROFLEX capacitor

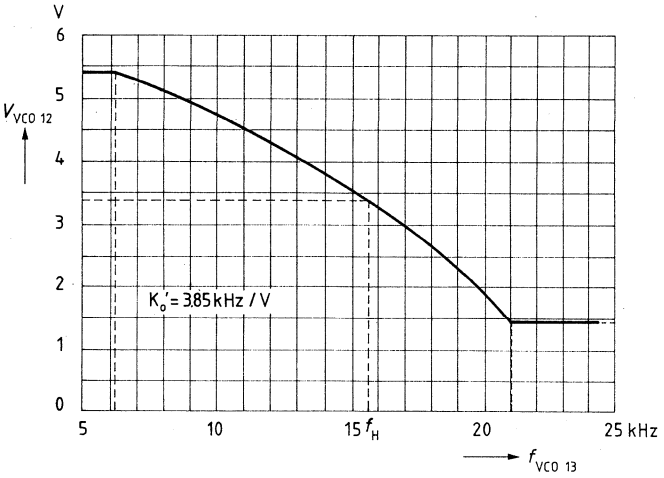
Block diagram



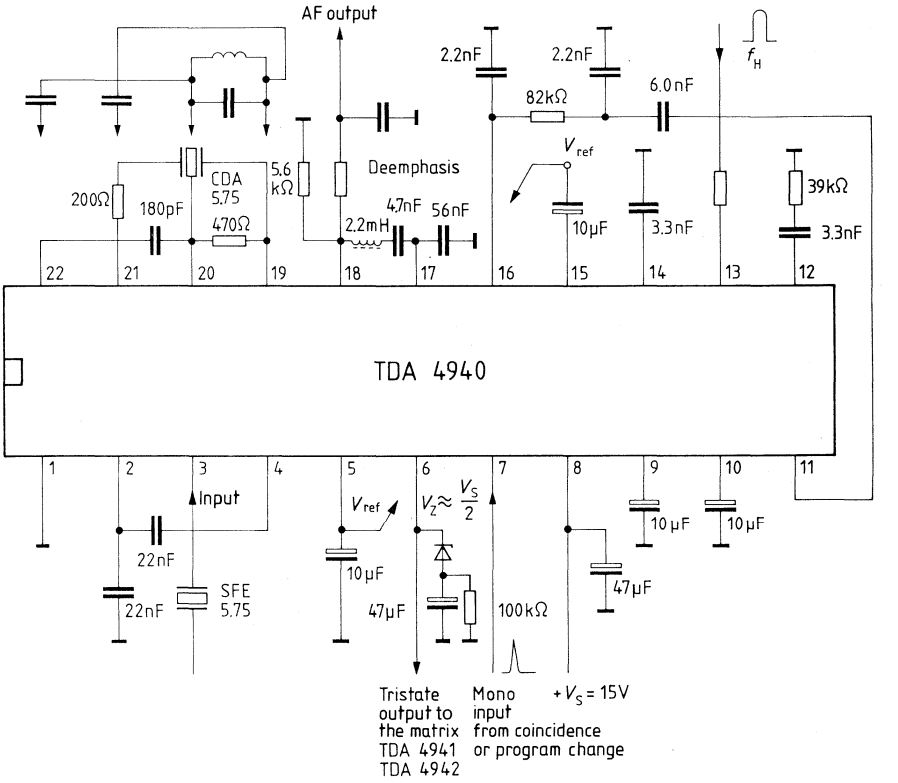
PLL transfer function



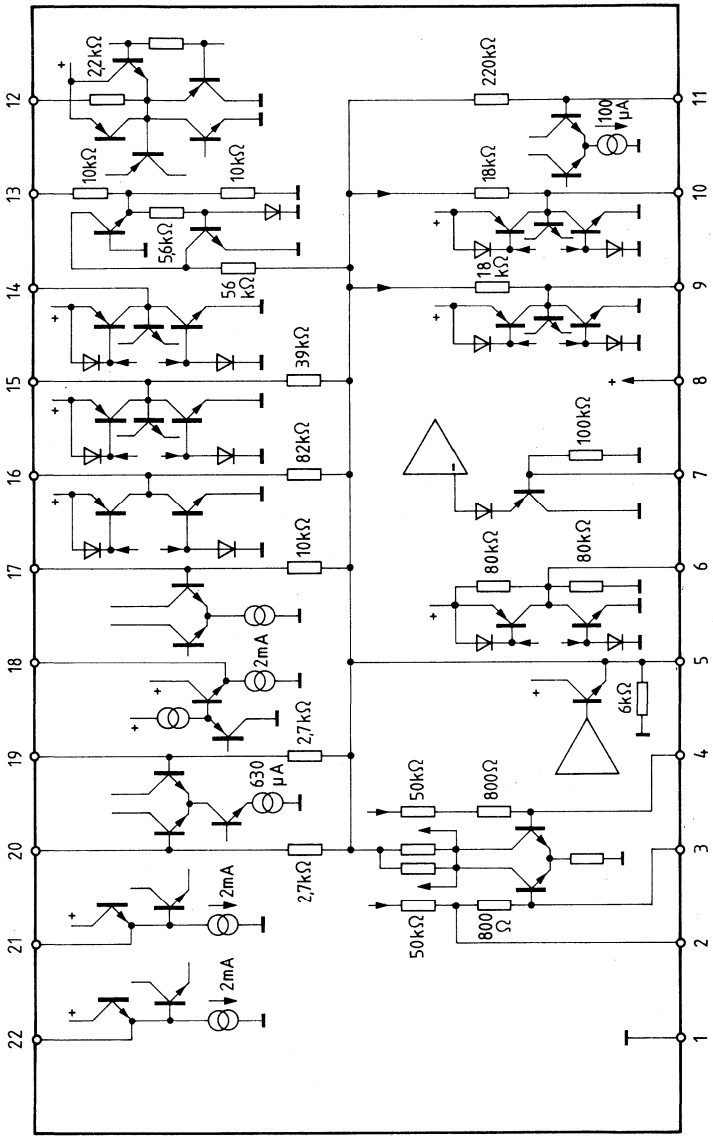
VCO tracking



Application circuit



Internal Pin Diagram



Bipolar circuit

Type	Ordering code	Package outline
TDA 4941	Q67000-A1952	DIP 22

Switchable matrix, CCIR VCR input/output, analog switches, AF output with balance control, headset amplifier with independent volume and balance control, LED driver.

Features

- Switchable matrix
- Stereo-VCR input/output
- All outputs are short-circuit-resistant

Maximum ratings

Supply voltage	V_S	16.0	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	70	K/W

Operating range

Supply voltage range	V_S	10 to 15.8	V
Frequency range (−1 dB)	f_i	20 to 20,000	Hz
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics ($V_S = 12$ V; $T_{amb} = 25$ °C)

		min	typ	max	
Total current consumption (without LED)	I_S		20	35	mA
LED driver current (each LED)	$I_{3,4}$	10	15	23	mA
Inverse current (LED's OFF)	$I_{3,4}$			50	µA
Reference voltage	V_{ref5}	4.5	4.8	5.2	V
Input resistance audio I	R_{i2}	11	15	20	kΩ
Input resistance audio II	R_{i22}	22	30	40	kΩ
Input resistance VCR	$R_{i17,19}$	40	51	64	kΩ
Input current of the adjustable inputs balance AF	I_{ad7}		3	10	µA
Input current of the adjustable inputs balance EP	I_{ad8}	±20	±45	±70	µA
Input current of the adjustable inputs volume EP	I_{ad11}	20	45	70	µA
Input current of the switches k 1/2, VCR stereo	$I_{6,14,15}$		20	30	µA
VCR P/R	I_{20}			300	µA
Input voltage audio I $THD = 0.7\%$	$V_{i2\,rms}$		150	600	mV
Input voltage audio II $THD = 0.7\%$	$V_{i22\,rms}$		300	1200	mV
Input voltage VCR playback	$V_{i17,19\,rms}$		0.5	2	V
Output voltage VCR					
($V_{i2} = 150$ mV)	$V_{q17,19\,rms}$	400	500	650	mV
($V_{i22} = 300$ mV)	$V_{q17,19\,rms}$	400	500	650	mV
AF output voltage					
($V_{i2} = 150$ mV)	$V_{q12,13\,rms}$	200	300	400	mV
($V_{i22} = 300$ mV)	$V_{q12,13\,rms}$	200	300	400	mV
Output voltage earphone (EP)					
($V_{i2} = 150$ mV)	$V_{q9,10\,rms}$	200	300	400	mV
($V_{i22} = 300$ mV)	$V_{q9,10\,rms}$	200	300	400	mV
AF output voltage					
($V_{17} = V_{19} = 500$ mV)	$V_{q12,13\,rms}$	200	300	400	mV
Output voltage earphone (EP)					
($V_{17} = V_{19} = 500$ mV)	$V_{q9.10\,rms}$	200	300	400	mV
Control range balance	$G_{B\,max}$	+3	+5	+6	dB
($V_{7,8} = 0 \ldots V_5$)	$G_{B\,min}$	−15	−12	−9	dB

Characteristics ($V_S = 12$ V; $T_{amb} = 25$ °C)

		min	typ	max	
Control voltage balance					
V_{qR} = max; V_{qL} = min	$V_{7,8}$		0		V
V_{qL} = max; V_{qR} = min			V_{Ref}		V
Voltage balance center	$V_{7,8}$	0.48	0.5 V_5	0.52	V
$V_R = V_L$					
Control range volume	G_L	85			dB
$V_{11} = 0 \ldots V_5$					
Output resistance AF output	$R_{q12,13}$		0.2	0.4	kΩ
Output resistance VCR output	$R_{q17,19}$		0.2	0.4	kΩ
Output resistance earphone output	$R_{q9,10}$		0.2	0.4	kΩ
Total harmonic distortion					
(V_{i2} = 0.5 V)	$THD_{9,13,17}$			0.5	%
(V_{i22} = 1 V)	$THD_{10,12,19}$			0.5	%
Channel separation	$a_{L/R}$	60			dB
AF, EP, VCR; f = 1 kHz					
Flutter and wow	$a_{L/R}$			2	dB
mono; volume = max					
volume = −30 dB					
Disturbance voltage spacing (all outputs)	$a_{S/N}$	60	70		dB
(V_i = 300/150 mV = 0 dB)					
volume = max;					
(f_i = 20 Hz to 20 kHz)					
Noise voltage at AF output	$V_{n12,13}$		100	300	µV
RF/VCR operation; balance center					
Noise voltage at earphone output	$V_{n9,10}$		10	30	µV
volume = min					
(f_i = 20 Hz to 20 kHz)					
Cross-talk attenuation VCR/AF/EP	$a_{9,10,12,13}$	60			dB
($V_{17} = V_{19} = 2\ V_{rms}$)					
($V_{20} = 0$; $V_{11} = V_5$)					
Cross-talk attenuation matrix	$a_{9,10}$	60			dB
(V_2 = 600 mV)					
AF/EP during VCR playback	$a_{12,13}$	60			dB
(V_{22} = 1200 mV)					
Switching input audio I/audio II					
H-input voltage = audio I	$V_{H6,14}$	4		V_S	V
or open					
L-input voltage = audio II	$V_{L6,14}$	0		2.8	V

Characteristics ($V_S = 12$ V; $T_{amb} = 25$ °C)

		min	typ	max	
Stereo input VCR-stereo					
H input voltage = stereo or open	V_{iH15}	4		V_S	V
L input voltage = stereo	V_{iL15}	0		2.8	V
Switching input VCR-P/R					
H input voltage = VCR-P	V_{iH20}	8		V_S	V
L input voltage = VCR-R or open	V_{iL20}	0		5	V
Switching voltage matrix					
Dual audio	V_{sw21}	0		1/6 V_S	V
Mono	V_{sw21}	1/3 V_S		2/3 V_S	V
Stereo	V_{sw21}	5/6 V_S		V_S	V

Truth table

Pin 14	Pin 6	Pin 15	Pin 20	Pin 21	Pin 4	Pin 3	
S1/AF	S2/KH	S3/VCR stereo	S4/VCR play/record	Tristate input	LED 1	LED 2	
X	X	X	open ≙ L	Stereo = V_S	ON	ON	VCR recording
X	X	X	L	Mono = $V_S/2$	OFF	OFF	VCR recording
Open H	X	X	L	2 tone = 0 V	ON	OFF	VCR recording
Ground L	X	X	L	2 tone = 0 V	OFF	ON	VCR recording
X	X	Stereo H ≙ V_S	V_S ≙ H	–	OFF	OFF	VCR playback
X	X	H	H	–	OFF	OFF	VCR playback
Open H	X	Mono L	H	–	ON	OFF	VCR playback
Ground L	X	L	H	–	OFF	ON	VCR playback

X = undetermined

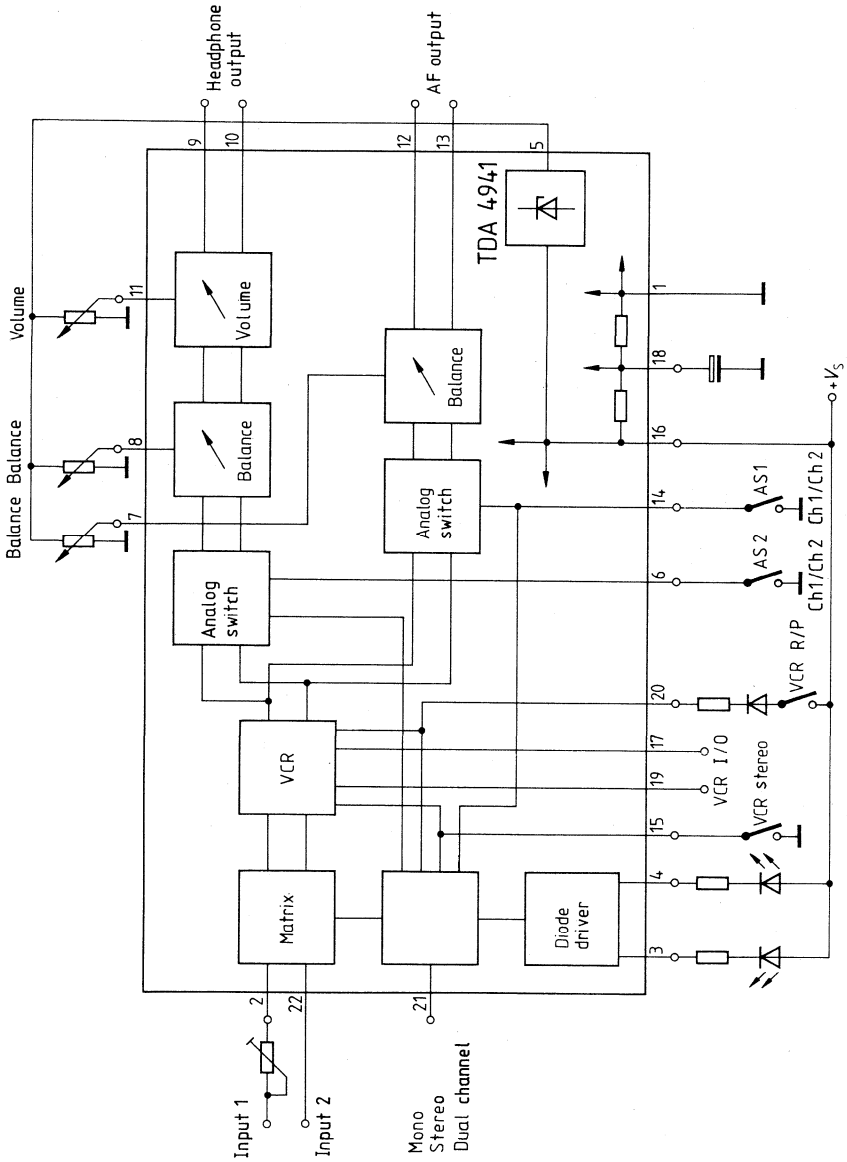
Circuit description

The TDA 4941 contains a switchable matrix with tristate input to provide the necessary L-R information. The switch input is controlled by the preceding pilot tone decoding integrated circuit. During dual audio operations, analog switches enable the selection of audio I or audio II respectively. Analog switch I affects the AF output via a DC voltage controlled balance control. The separately switchable analog switch II controls the headset output, which is equipped with a DC voltage controlled volume and balance control. The switch inputs for the analog switches are effective during two-channel operations only and not during stereo or mono modes. The LED driver displays the position of analog switch I and/or stereo or mono operations. Also, the position of analog switch I will be indicated again by the driver during VCR playback. A standard VCR device can be connected to the stereo VCR input/output. All outputs are short-circuit resistant.

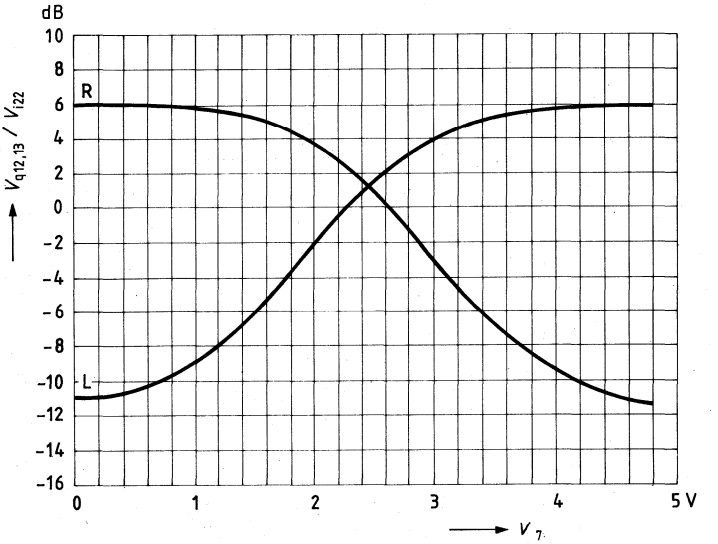
Pin configuration

Pin No.	Function
1	Ground
2	Audio I 5.5 MHz demodulator
3	LED driver audio II
4	LED driver audio I
5	Stabilized voltage
6	Audio I/audio II – change-over switch headset output
7	Balance control AF output
8	Balance control earphone output
9	Headset output left
10	Headset output right
11	Headset volume control
12	AF output right
13	AF output left
14	Audio I/audio II – interchange AF switch
15	VCR stereo switch
16	Supply voltage
17	VCR input/output left/audio I
18	Decoupling
19	VCR input/output right/audio II
20	VCR recording/playback change-over switch
21	Mono-stereo dual audio switch-over
22	Audio II 5.75 MHz demodulator

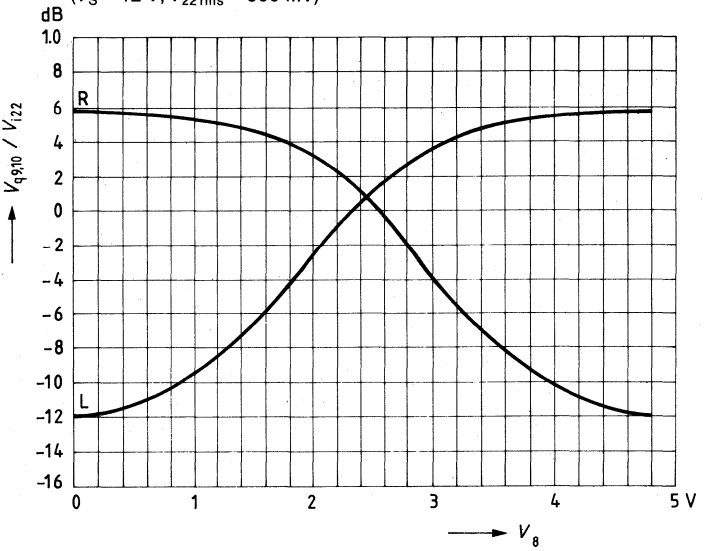
Block diagram



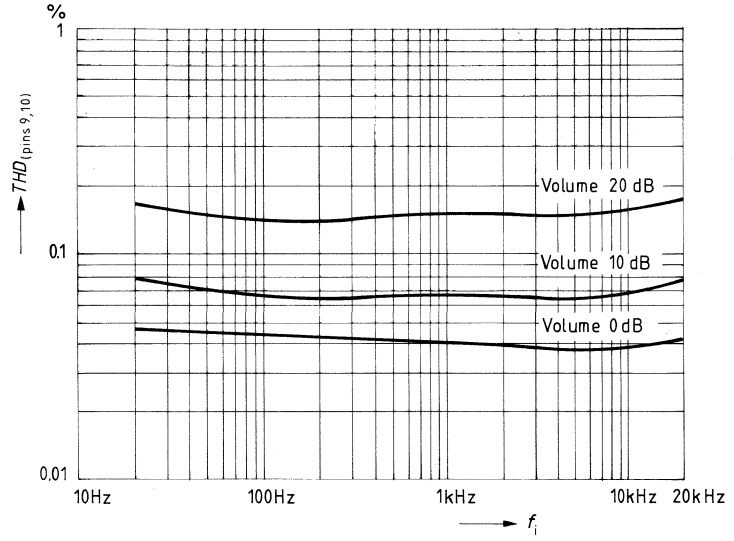
Balance AF output versus V_7
($V_S = 15$ V; $V_{i22\,rms} = 500$ mV)



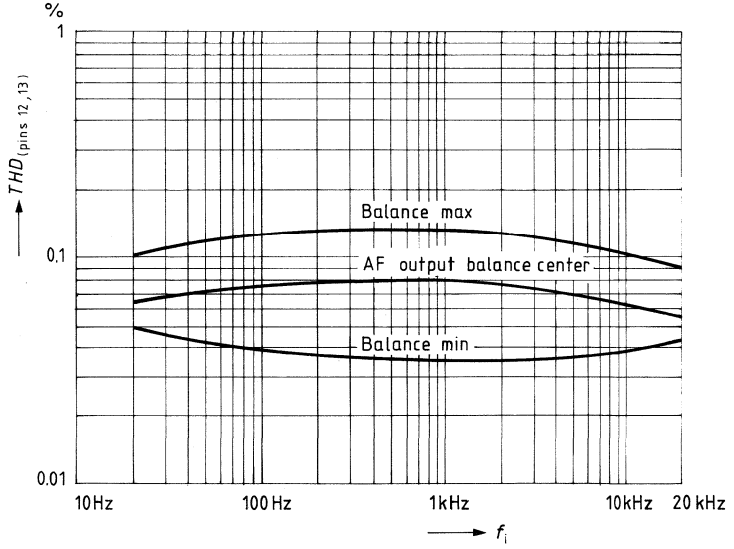
Balance earphone output versus V_8
($V_S = 12$ V; $V_{22\,rms} = 500$ mV)



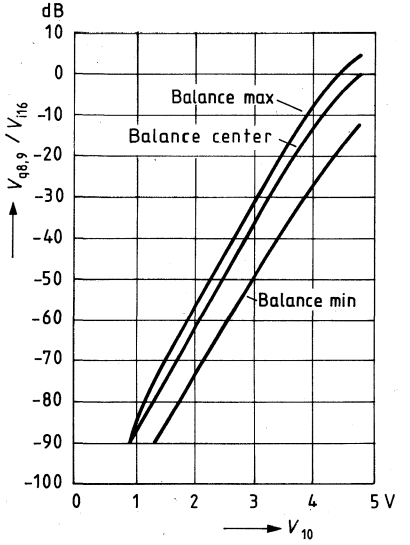
Total harmonic distortion versus input frequency
($V_S = 12$ V; $V_{irms} = 300$ mV)



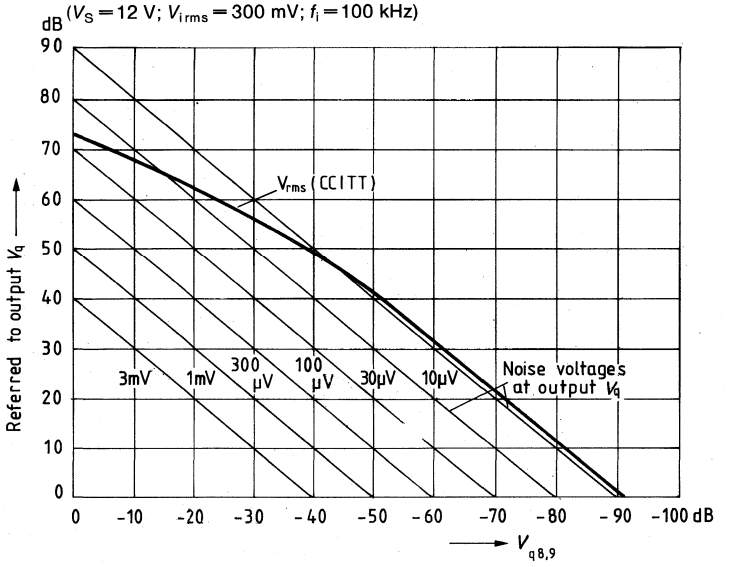
Total harmonic distortion versus input frequency
($V_S = 12$ V; $V_{irms} = 300$ mV)



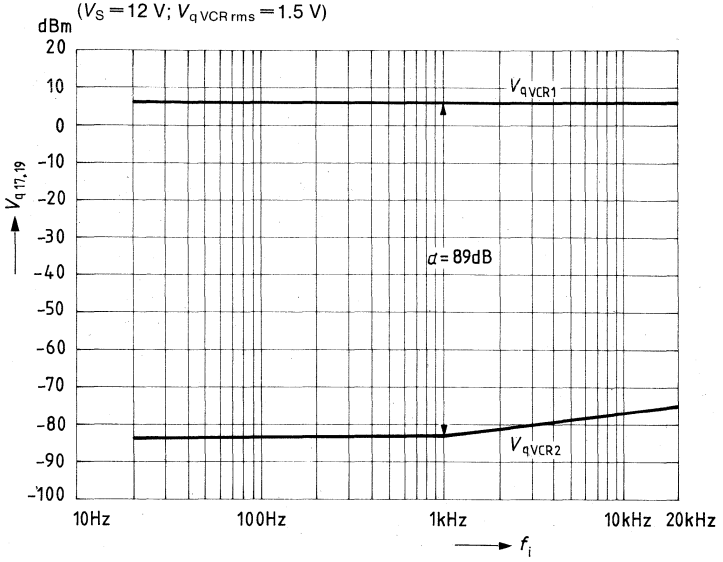
Volume control earphone output versus V_{11}
($V_S = 12$ V)



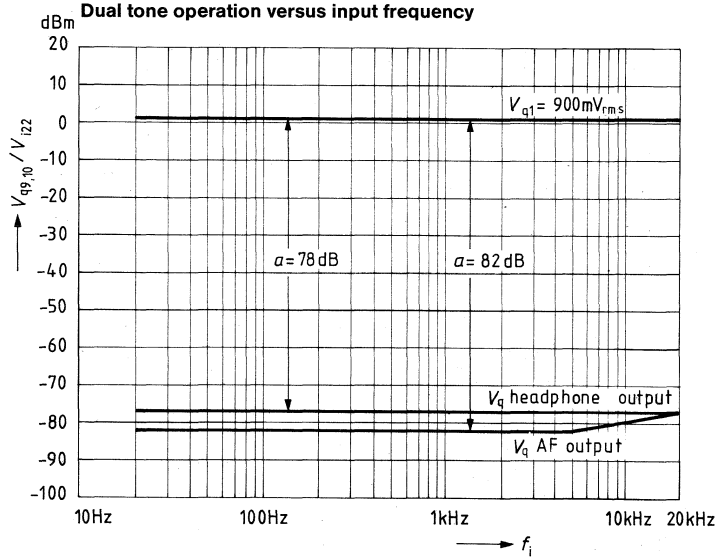
Disturbance voltage spacing versus attenuation
($V_S = 12$ V; $V_{irms} = 300$ mV; $f_i = 100$ kHz)



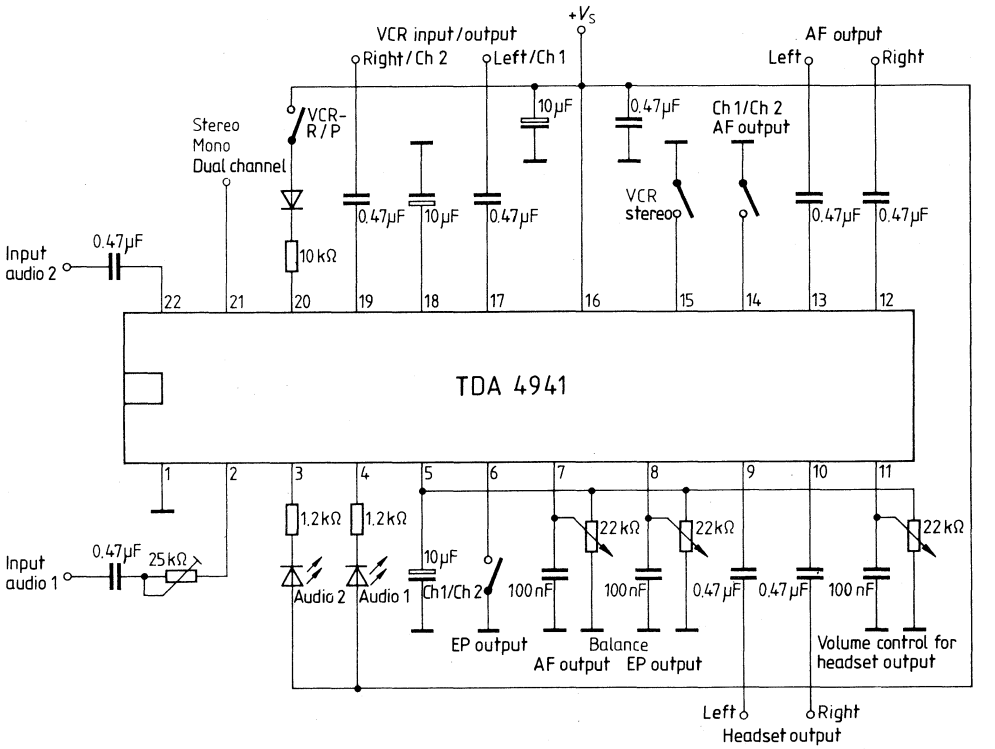
Cross talk attenuation
VCR output (pins 17, 19) versus input frequency
(V_S = 12 V; $V_{q\,VCR\,rms}$ = 1.5 V)



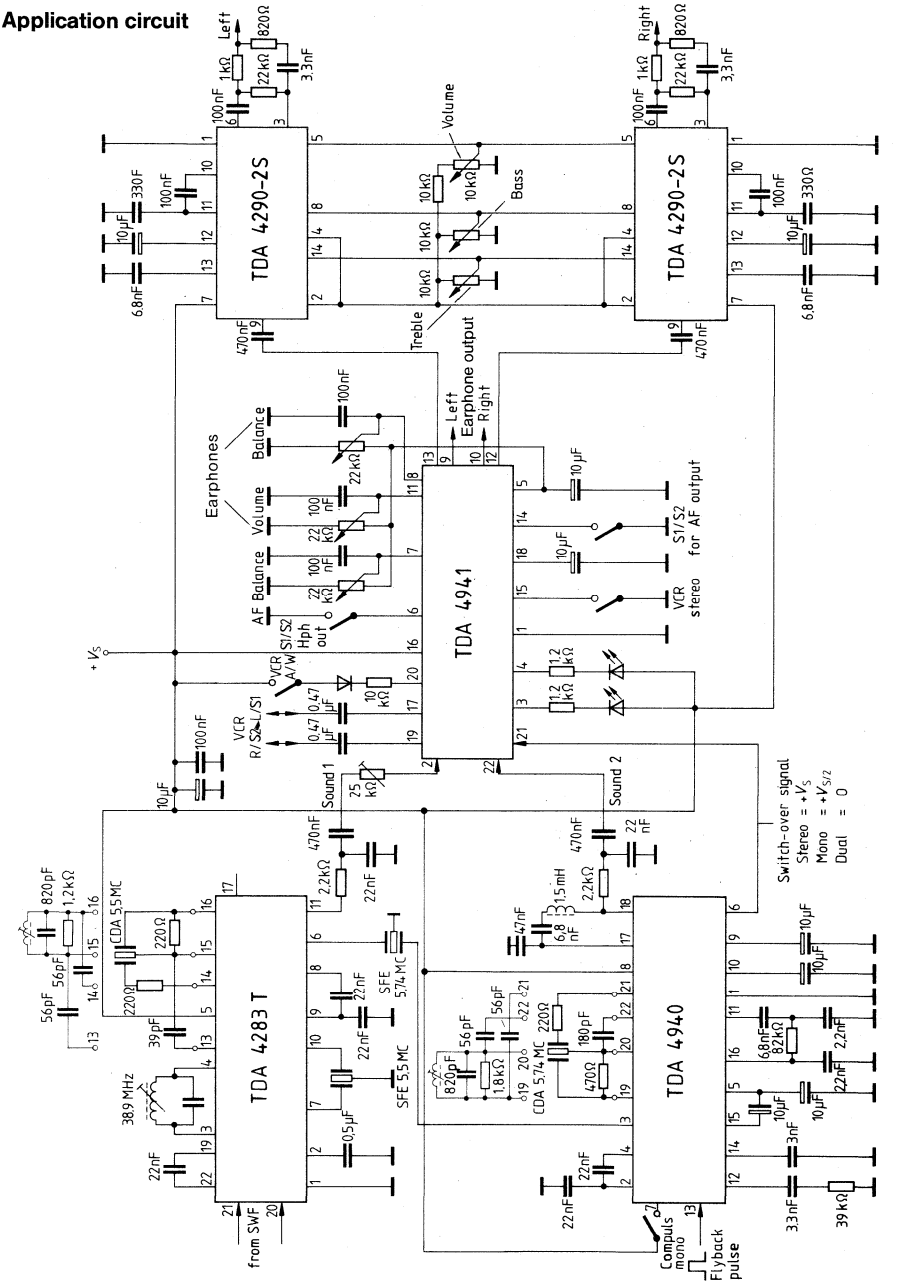
Cross talk attenuation
Dual tone operation versus input frequency



Application circuit



Application circuit



Bipolar circuit

Type	Ordering code	Package outline
TDA 4942	Q67000-A1926	DIP 16

The TDA 4942 contains a switchable matrix with tristate input to provide *L-R* information. The switch input is controlled by the immediately preceding pilot tone decoding IC. During dual operation the subsequent analog switch enables the selection of audio I or audio II. The LED driver displays the position of the analog switch, and/or stereo or mono operation. The analog switch controls the audio tape recorder output as well as the AF output. This output is equipped with a dc voltage regulated volume and balance control.

Features

- Switchable matrix
- Tape recorder output
- All outputs are short-circuit-resistant

Maximum ratings

Supply voltage (1 minute)	V_S	16.5	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	70	K/W

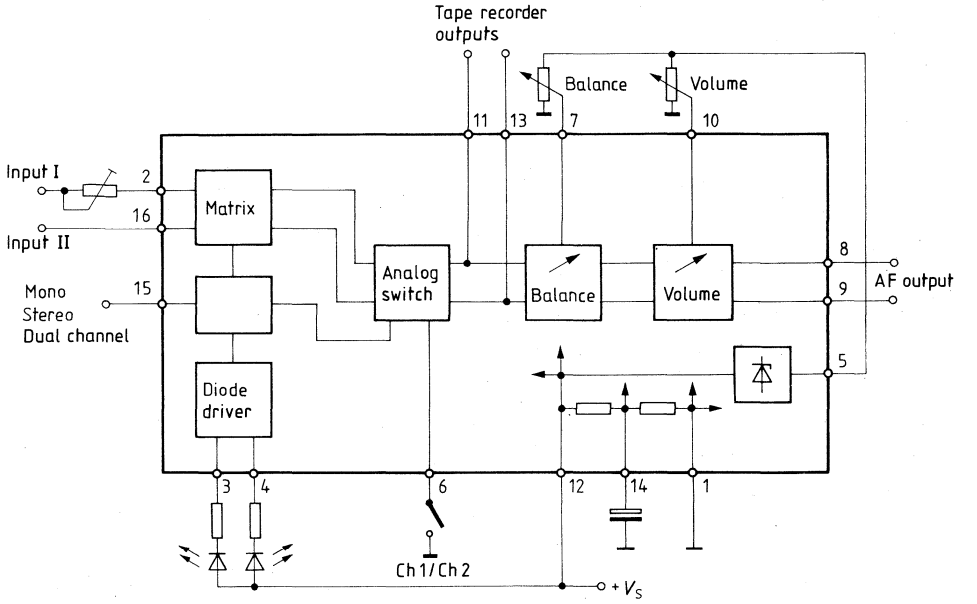
Operating range

Supply voltage range	V_S	10 to 15.8	V
Frequency range (−1 dB)	f_i	20 to 20,000	Hz
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics ($V_S = 12$ V; $T_{amb} = 25$ °C)

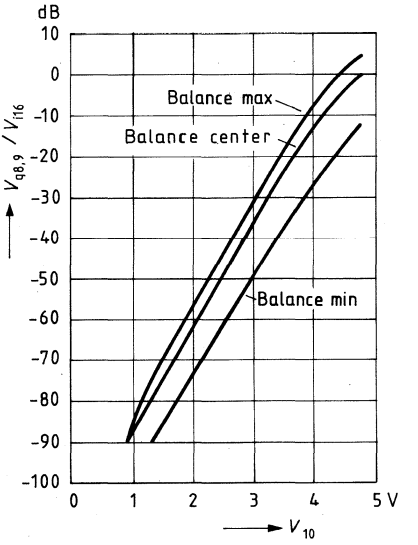
		min	typ	max	
Total current consumption (without LED)	I_{S12}		15		mA
LED driver current (each LED)	$I_{LED3,4}$	10	15		mA
Reference voltage	V_{ref5}		4.8		V
Input resistance audio I	R_{i2}		15		kΩ
Input resistance audio II	R_{i16}		30		kΩ
Input current of the adjust. input	$I_{ad7,10}$		3.5		μA
Input current of the switch	I_{sw6}		20		μA
Input voltage audio I ($THD = 0.7\%$)	$V_{i2\,rms}$		150	600	mV
Input voltage audio II ($THD = 0.7\%$)	$V_{i16\,rms}$		300	1200	mV
Output voltage tape rec. output ($V_{i2} = 150$ mV)	$V_{qTR11,13\,rms}$		150		mV
Output voltage tape rec. output ($V_{i16} = 300$ mV)	$V_{qTR11,13\,rms}$		150		mV
AF output voltage ($V_{i2} = 150$ mV)	$V_{qAF8,9\,rms}$		300		mV
AF output voltage ($V_{i16} = 300$ mV)	$V_{qAF8,9\,rms}$		300		mV
AGC range balance ($V_{bal} = 0 \ldots V_{ref}$)	$G_{bal\,max}$		+6		dB
AGC range balance ($V_{bal} = 0 \ldots V_{ref}$)	$G_{bal\,min}$		−12		dB
Voltage balance center ($V_{right} = V_{left}$)	V_{bal7}	0.48	0.5 V_{ref}	0.52	V
AGC range volume ($V_{vol} = 0 \ldots V_{ref}$)	ΔG_{vol}	85			dB
Output resistance AF output	$R_{qAF8,9}$		0.2		kΩ
Output resistance tape rec. output	$R_{qTR11,13}$		0.5		kΩ
Total harmonic distortion ($V_i = 0.5$ or 1 V)	$THD_{8,9,11,13}$			0.5	%
Channel separation	$a_{L/R\,8\text{-}9,11\text{-}13}$	60			dB
Channel deviation (volume = max)	$a_{L/R\,8\text{-}9}$			2	dB
Disturbance voltage spacing (volume = max; $f_i = 20$ Hz to 20 kHz)	$a_{S/N}$		70		dB
Noise voltage at the AF output (volume = min; $f_i = 20$ Hz to 20 kHz)	$V_{nAF8,9}$		10		μV
Switch input					
H input voltage ≙ audio I (or open)	V_{6H}	4		V_S	V
L input voltage ≙ audio II	V_{6L}	0		2.8	V
Control voltage balance ($V_{qr} = \max$; $V_{ql} = \min$)	V_{bal7}		0		V
Control voltage balance ($V_{ql} = \max$; $V_{qr} = \min$)	V_{bal7}		V_{ref}		V
Switch voltage matrix					
dual audio	V_{sw15}	0		1/6 V_S	V
mono	V_{sw15}	1/3 V_S		2/3 V_S	V
stereo	V_{sw15}	5/6 V_S		V_S	V

Block diagram

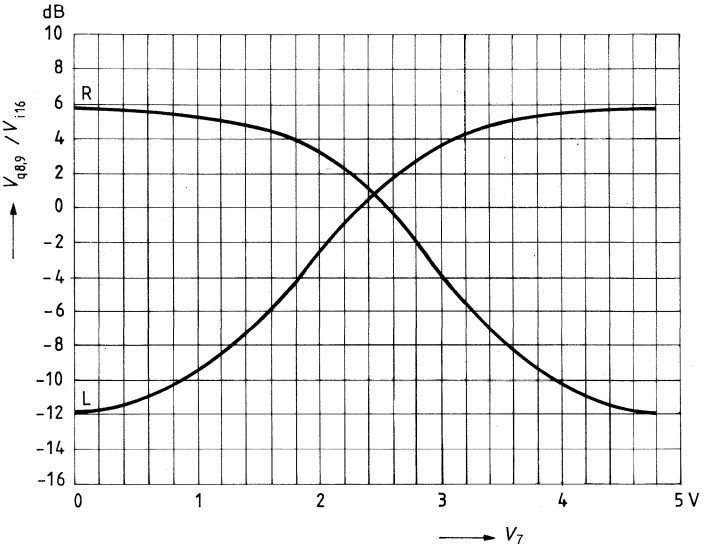


Truth table

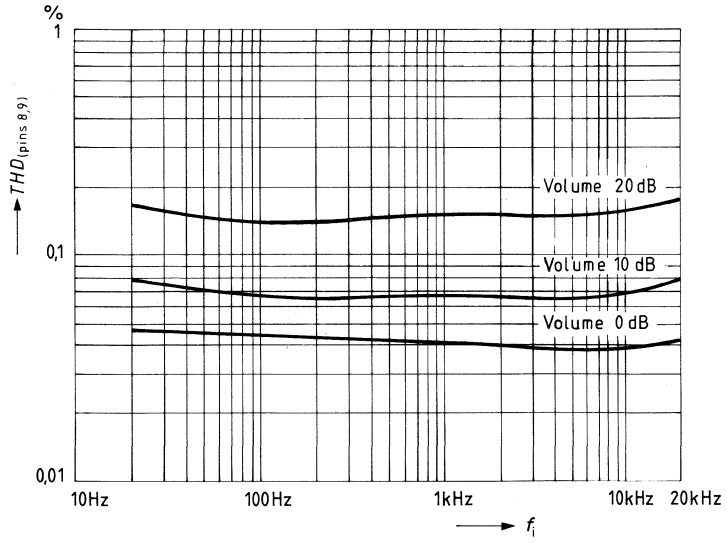
Pin 6	Pin 15	Pin 4	Pin 3
S1/AF	Tristate input	LED 1	LED 2
Any	Stereo = V_S	ON	ON
Any	Mono = $V_S/2$	OFF	OFF
Open H	2 tone = 0 V	ON	OFF
Ground L	2 tone = 0 V	OFF	ON



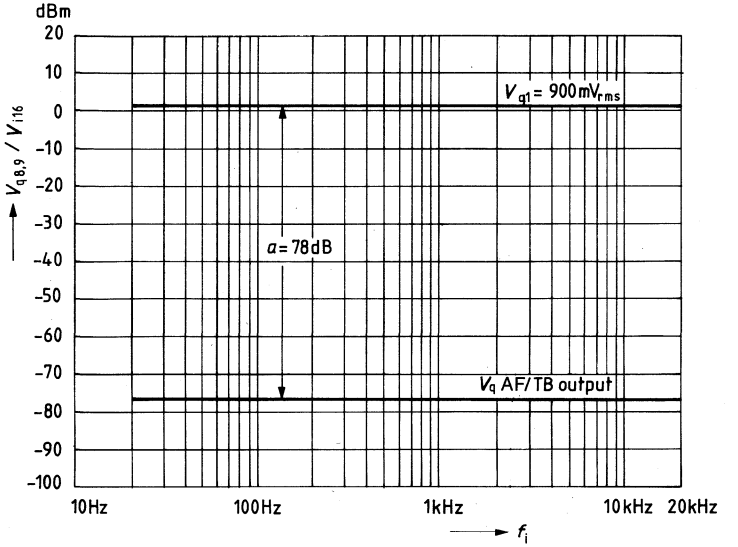
Balance versus V_7
($V_S = 12$ V; $V_{16\,rms} = 500$ mV)



Total harmonic distortion versus input frequency
($V_S = 12$ V, $V_{i\,rms} = 300$ mV)

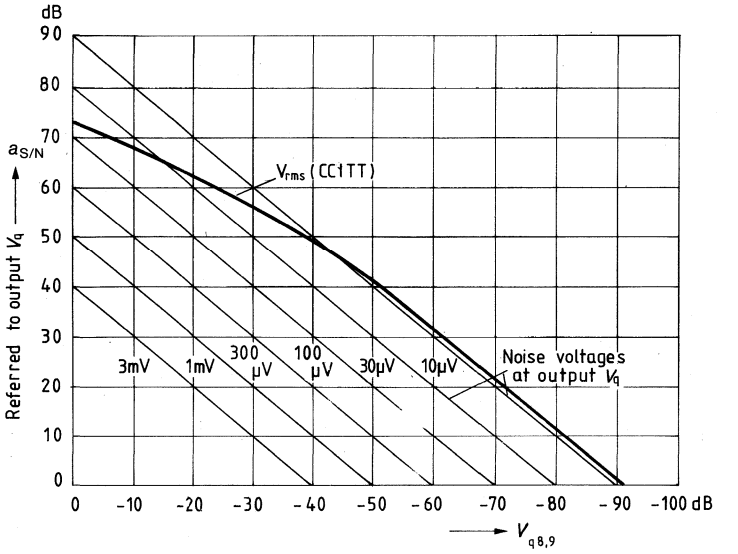


Cross-talk attenuation
Dual tone operation versus input frequency

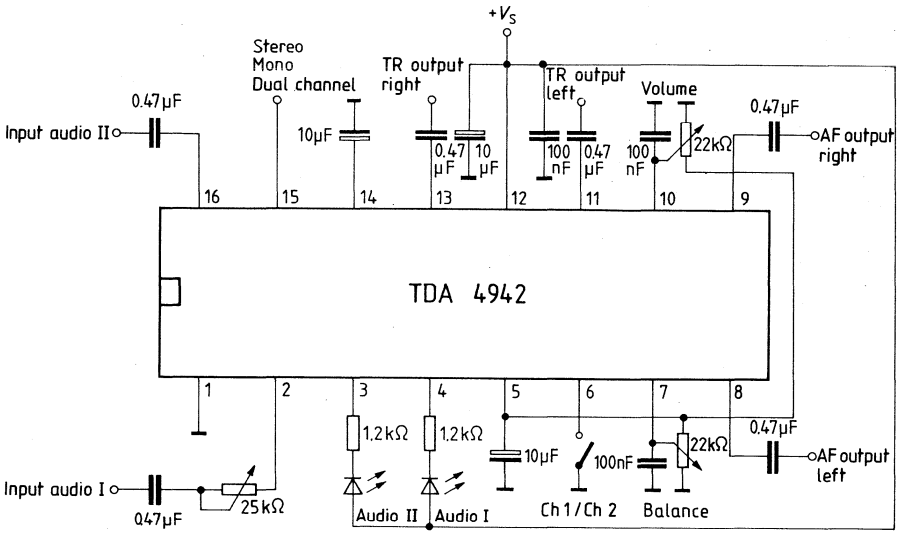


* TB = Tape recorder

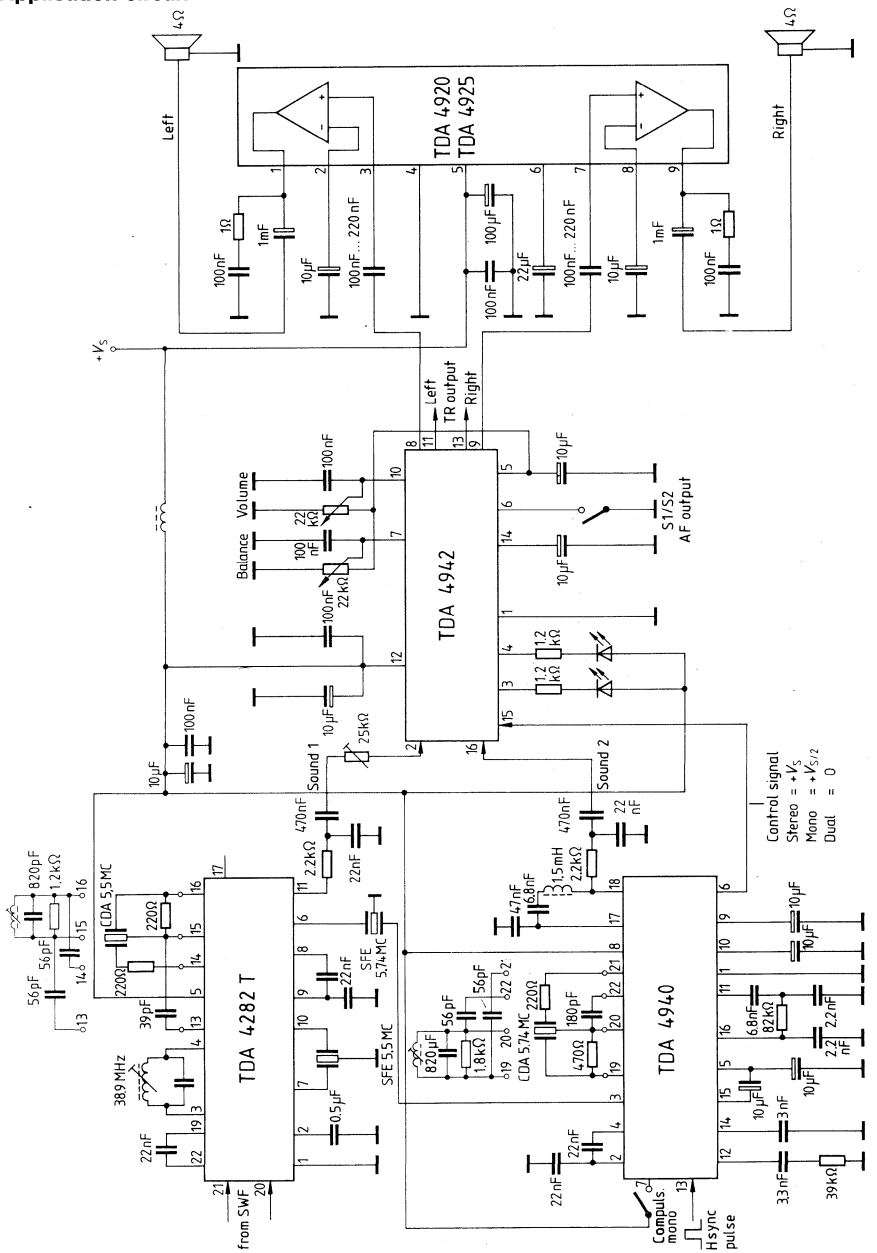
Disturbance voltage spacing versus attenuation
(V_S = 12 V; V_{irms} = 300 mV; f_i = 1 kHz)



Application circuit



Application circuit



Bipolar circuit

Type	Ordering code	Package outline
TDA 4944	Q67000-A2186	DIP 14

The integrated circuit TDA 4944 is equipped with a switchable matrix, one CCIR VCR input and output, analog switches and an LED driver. The *L-R* information is determined by the matrix switched with the tristate input. This switch input is controlled by the preceding pilot tone decoding circuit TDA 4940. By combining the stereo VCR input and output, a standard VCR recorder can be attached. The subsequent analog switch enables the selection of audio I or audio II during dual audio operation. The position of the analog switch and/or stereo or mono operation are indicated by the externally connected LEDs. The operation mode of the TDA 4944 is illustrated below in table 1. In addition, all outputs are short-circuit-resistant.

Features

- Switchable matrix
- VCR input and output according to CCIR standards
- All outputs are short-circuit resistant

Maximum ratings

Supply voltage	V_{S12}	16.5	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	90	K/W

Operating range

Supply voltage	V_{S12}	10 to 15.8	V
Frequency range (−1 dB)	$f_{i4,6,1,13}$	20 to 20,000	Hz
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics ($V_S = 12$ V; $T_{amb} = 25$ °C)

		min	typ	max	
Total current consumption (without LED)	I_{S12}		14		mA
LED driver current (each LED)	$I_{LED7,8}$	10	15		mA
Input resistance audio I	R_{i6}		15		kΩ
Input resistance audio II	R_{i4}		30		kΩ
Input current of the VCR circuit	I_2			300	µA
Input voltage audio I ($THD = 0.7\%$)	$V_{i6\,rms}$		150	600	mV
Input voltage audio II ($THD = 0.7\%$)	$V_{i4\,rms}$		300	1200	mV
Input voltage VCR (playback)	$V_{i1,13\,rms}$		0.5	2	V
Output voltage VCR ($V_{i6\,rms} = 150$ mV; $V_{i4\,rms} = 300$ mV)	$V_{q1,13\,rms}$		500		mV
AF output voltage ($V_{i6\,rms} = 150$ mV; $V_{i4\,rms} = 300$ mV)	$V_{q9,10\,rms}$		300		mV
Output resistance AF output	$R_{q9,10\,rms}$		0.2		kΩ
Output resistance VCR output	$R_{q1,13}$		0.2		kΩ
Total harmonic distortion ($V_{i4\,rms} = 1$ V; $V_{i6\,rms} = 0.5$ V)	THD			0.5	%
Channel separation	$a_{L/R}$		60		dB
Disturbance voltage spacing ($V_{i6\,rms} = 150$ mV; $V_{i4\,rms} = 300$ mV; $f_i = 20$ Hz to 20 kHz)	$a_{S+N/N}$		70		dB
Noise voltage at the AF output	$V_{n\,AF9,10}$		100		µV
Switch input audio I/audio II					
H input voltage = audio I = S1 open	$V_{H,11}$	4		V_S	V
L input voltage = audio II = S1 closed	$V_{L,11}$	0		2.8	V
Swicht input VCR P/R					
H input voltage ≙ VCR-P S2 closed	V_{H2}	8		V_S	V
L input voltage ≙ VCR-R S2 open	V_{L2}	0		5	V
Switch voltage matrix					
dual audio	V_3	0		1/6 V_S	V
mono	V_3	1/3 V_S		2/3 V_S	V
stereo	V_3	5/6 V_S		V_S	V
Input current	I_{11}		20		µA

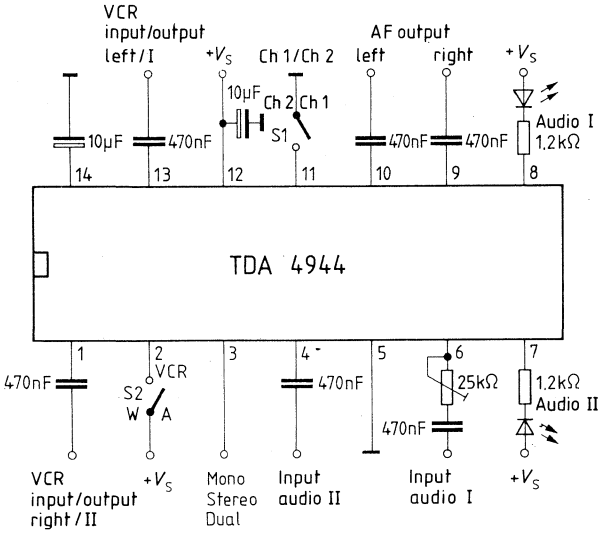
Pin configuration

Pin No.	Function
1	Combined VCR input/output, right channel II
2	VCR record/play mode switch
3	Mono, stereo or dual sound mode switch
4	Channel II demodulator input (5.75 MHz)
5	Ground
6	Channel I demodulator input (5.5 MHz, NTSC 4.5 MHz)
7	LED driver for channel II indication
8	LED driver for channel I indication
9	AF output right channel
10	AF output left channel
11	Audio channel I/channel II mode switch
12	$+V_S$
13	Combined VCR input/output left channel I
14	Decoupling capacitor

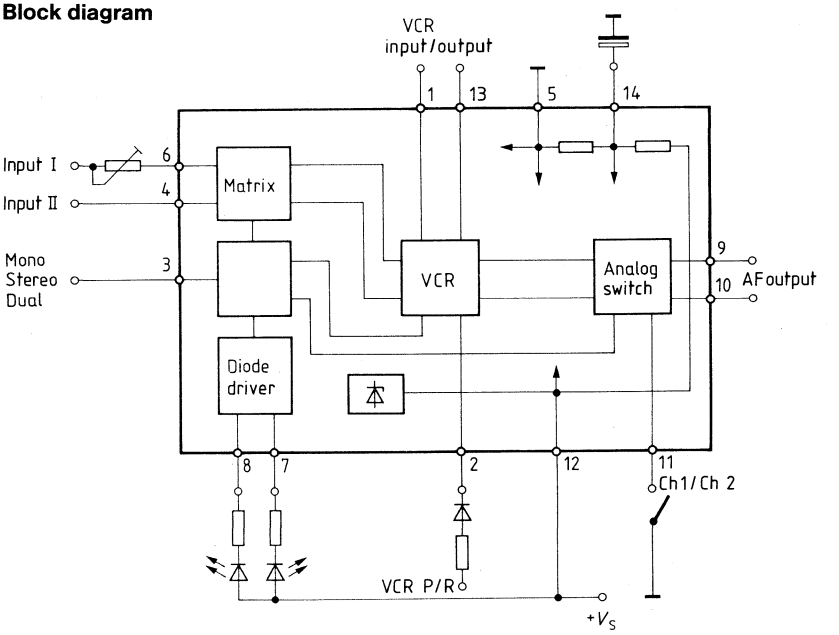
Truth table

Pin 2	Pin 3	Pin 11	Pin 7	Pin 8
VCR P/R	Tristate input	Audio I/II	LED II	LED I
V_S = Play	any	any	ON	ON
0 V = Rec	0 V = 2 tone	Open = Audio I	OFF	ON
0 V	0 V	Ground=Audio II	ON	OFF
0 V	1/2 V_S = Mono	any	OFF	OFF
0 V	V_S = Stereo	any	ON	ON

Application circuit



Block diagram



Preliminary data

Bipolar circuit

Type	Ordering code	Package outline
TDA 5400	Q67000-A2165	DIP 18
TDA 5410	Q67000-A2173	

The high gain, controlled video IF amplifier with controlled demodulator includes low impedance outputs for the positive and negative video signal, gated control as well as delayed tuner control and an AFC output.

TDA 5400: for PNP tuners
TDA 5410: for NPN tuners

Features

- High degree of integration
- Extensive control range
- High input sensitivity

Maximum ratings

Supply voltage	V_S	16.5	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	70	K/W

Operating range

Supply voltage range	V_S	10.5 . . . 15.8	V
IF-frequency range	f_{IF}	60	MHz
Ambient temperature range	T_{amb}	0 . . . 70	°C

Characteristics ($V_S = 13$ V; $T_{amb} = 25$ °C)

Current consumption	I_{13}	60	mA
Stabilized reference voltage	$V_{14/12}$	6.0	Vdc
Control current for tuner ($V_{16} = 0.5\ V_{13}$)	I_{16}	4.0	mA
Tuner AGC threshold	$V_{15/12}$	0 to 4	Vdc
Gating pulse voltage			
pos. gating pulse	V_1	+3.0	V
neg. gating pulse	V_1	−3.0	V
Input voltage at G_{max} ($V_3 = 3\ V_{pp}$)	$V_{i17/18}$	max 100	μV
AGC range	ΔG	60	dB
IF control voltage			
V_{max}	$V_{2/12}$	min 0	Vdc
V_{min}	$V_{2/12}$	max 4.0	Vdc
AFC output current	I_{q6}	±1.0	mA
AFC switching			
($V_8 = V_9$; $R = 10$ kΩ) OFF	$V_{8/12}$	max 4.0	Vdc
($V_8 = V_9$; $R = \infty$) ON	$V_{8/12}$	6.0	Vdc
AFC direction			
$di/df > 0$	$V_{5/12}$	4.0 to V_{13}	Vdc
$di/df < 0$	$V_{5/12}$	0 to 1.0	Vdc
Video output voltage (pos.) ($R_L = \infty$)	$V_{q3\,pp}$	3.0	V
Sync pulse level	$V_{3/12}$	2.0	Vdc
DC voltage ($V_2 = 4$ V; $V_{17/18} = 0$)	$V_{3/12}$	5.3	Vdc
Output current			
(to ground through R)	I_{q3}	−5.0	mA
(to plus $V_3 = 7$ V)	I_{q3}	+2.0	mA
Video output voltage (neg.) ($R_L = \infty$)	$V_{q4\,pp}$	3.0	V
Sync pulse level	$V_{4/12}$	$V_{13} - 2.0$	Vdc
DC voltage ($V_2 = 4$ V; $V_{17/18} = 0$)	$V_{4/12}$	$V_{13} - 5.3$	Vdc
Output current			
(to ground through R)	I_{q4}	−5.0	mA
(to plus $V_4 = V_{13}$)	I_{q4}	+1.0	mA

Additional application data[1])

Input impedance	$Z_{17/18}$	1.8/2	kΩ/pF
Output impedance	$Z_{10/11}$	6.6/2	kΩ/pF
AFC input impedance	$Z_{8/9}$	20	kΩ
Output resistance	R_3	150	Ω
Output resistance	R_4	150	Ω
Residual IF (basic frequency)	V_3; V_4	10	mV
Video bandwidth (−3 dB)	B_{video}	6.0	MHz
Intermodulation ratio with reference to f_{FT} (1.07 MHz)	a	45	dB

1) not measured

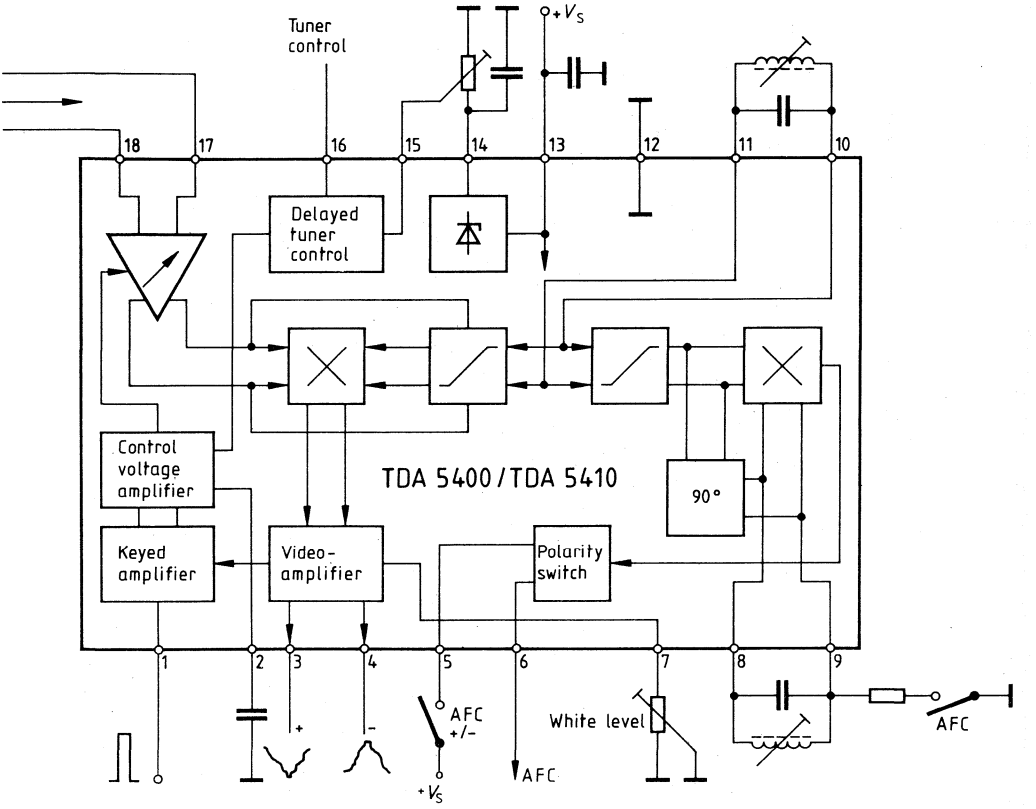
Circuit description

The integrated circuit is comprised of a 4-stage controlled AM amplifier, a limiter and mixer for synchronous demodulation of the video signals as well as an FM demodulator to generate positive or negative AFC voltages. In addition, an amplifier for both the positive and negative video output signal is included. The positive video signal together with the positive flyback pulse are used for gated control. The delayed tuner AGC is generated by a threshold amplifier driven by the control voltage.

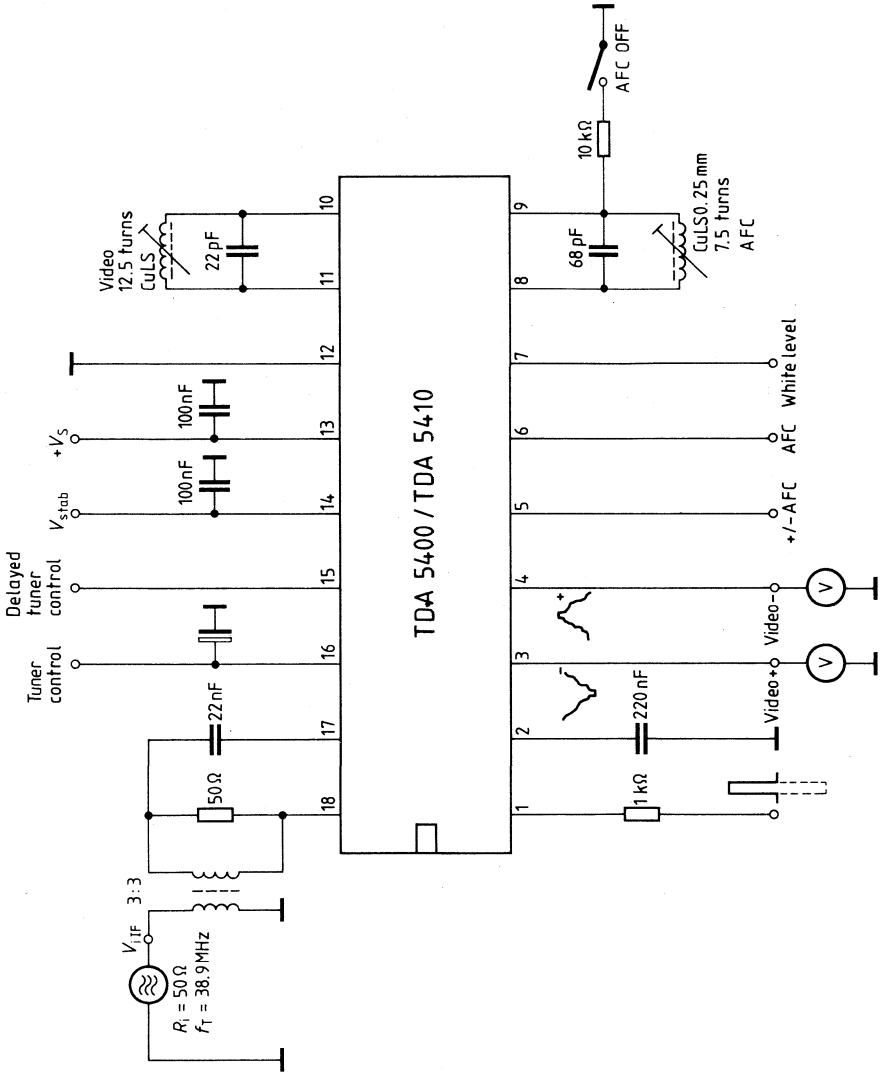
Pin configuration

Pin No.	Function
1	Gating pulse
2	Time constant AGC
3	Positive video output
4	Negative video output
5	AFC polarity switch
6	AFC output
7	White level adjustment
8	AFC circuit
9	AFC circuit
10	Tank circuit
11	Tank circuit
12	Ground
13	Supply voltage
14	Reference voltage
15	Tuner AGC
16	Delayed AGC output
17	Video IF input
18	Video IF input

Block diagram



Measurement circuit



Preliminary data **Bipolar circuit**

Type	Ordering code	Package outline
TDA 5430	Q67000-A2202	DIP 18

The controlled AM broadband amplifier includes a synchronous demodulator, video amplifier and an FM demodulator to generate the AFC voltage (negative S-curve) as well as the control voltage for the IF amplifier and PNP tuner. The AFC section is supplied by a separate supply voltage.

Features

- High degree of integration
- Extensive control range
- High input sensitivity

Maximum ratings

Supply voltage	V_{S1}	16.5	V
	V_{S2}	33	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	70	K/W

Operating range

Supply voltage	V_{S1}	10.5 to 15.8	V
	V_{S2}	30 to 32	V
IF frequency range	f_{IF}	15 to 60	MHz
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics ($V_{S1} = 13$ V; $T_{amb} = 25$ °C)

		min	typ	max	
Current consumption	I_{13}		60		mA
Stabilized reference voltage	$V_{14/12}$		6.0		Vdc
Control current for tuner ($V_{16} = 0.5\ V_{13}$)	I_{16}		4.0		mA
Tuner AGC threshold	$V_{15/12}$	0		4	Vdc
Gating pulse voltage					
pos. gating pulse	V_1		+3.0		V
neg. gating pulse	V_1		−3.0		V
Input voltage at G_{max} ($V_3 = 3\ V_{pp}$)	$V_{i17/18}$			100	µV
AGC range	ΔG		60		dB
IF control voltage G_{max}	$V_{2/12}$	0			Vdc
G_{min}	$V_{2/12}$			4.0	Vdc
AFC output current (di/df < 0)	I_{q6}		±1.0		mA
AFC switching					
OFF ($V_8 = V_9; R = 10$ kΩ)	$V_{q8/12}$	0		4.0	Vdc
ON ($V_8 = V_9; R = \infty$)	$V_{i8/12}$		6.0		Vdc
AFC supply voltage	$V_{5/12}$	30		32	Vdc
AFC current consumption	I_5		4.0		mA
Video output voltage (pos.) ($R_L = \infty$)	$V_{q3\,pp}$		3.0		V
Sync pulse level	$V_{3/12}$		2.0		Vdc
DC voltage ($V_2 = 4$ V; $V_{17/18} = 0$)	$V_{3/12}$		5.3		V
Output current					
to ground through R	I_{q3}		−5.0		mA
to plus $V_3 = 7$ V	I_{q3}		+2.0		mA
Video output voltage (neg.) ($R_L = \infty$)	$V_{q4\,pp}$		3.0		V
Sync pulse level	$V_{4/12}$		$V_{13}-2.0$		Vdc
DC voltage ($V_2 = 4$ V; $V_{17/18} = 0$ V)	$V_{4/12}$		$V_{13}-5.3$		Vdc
Output current					
to ground through R	I_{q4}		−5.0		mA
to plus $V_4 = V_{13}$	I_{q4}		+1.0		mA
Additional application data					
Input impedance	$Z_{i17/18}$		1.8/2		kΩ/pF
Output impedance	$Z_{q10/11}$		6.6/2		kΩ/pF
AFC-input impedance	$Z_{i8/9}$		20		kΩ
Output resistance	R_{q3}		150		Ω
Output resistance	R_{q4}		150		Ω
Residual IF (basic frequency)	$V_3; V_4$		10		mV
Video bandwidth (−3 dB)	B_{video}		6.0		MHz
Intermodulation ratio with reference to f_{FT} (1.07 MHz)	a		45		dB

1) not measured

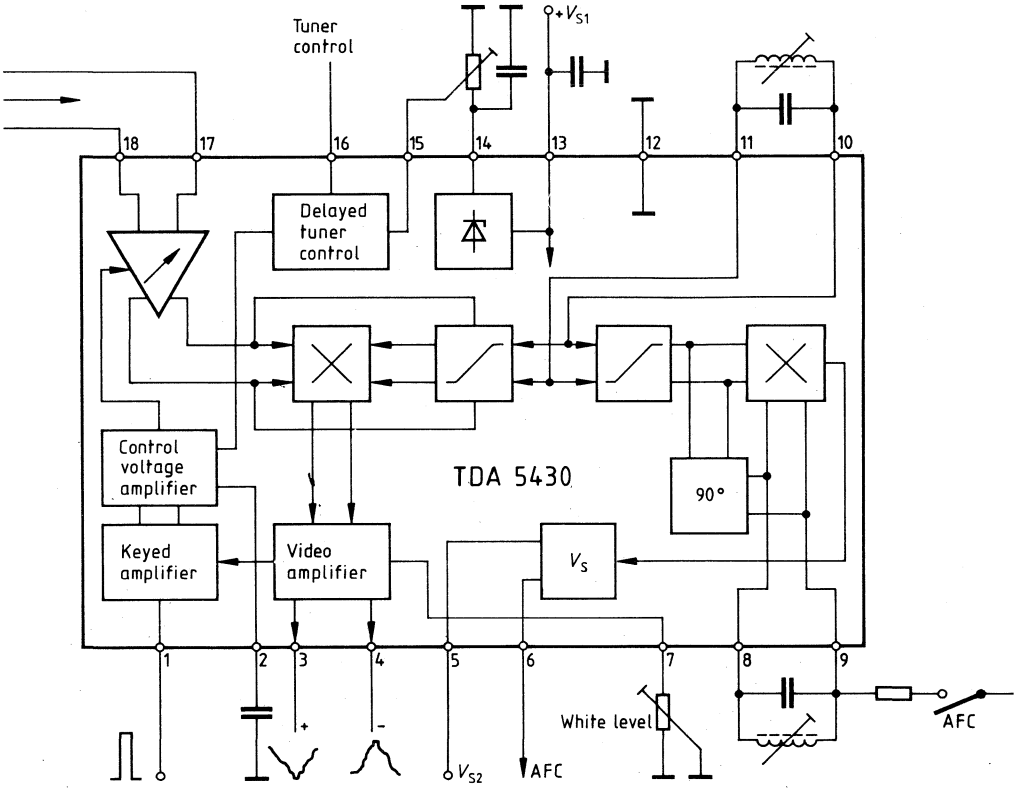
Circuit description

The integrated circuit is comprised of a 4-stage controlled AM amplifier, a limiter and mixer for synchronous demodulation of the video signals as well as an FM demodulator to generate the AFC voltage (negative S-curve). Furthermore, the component includes a video amplifier for both the positive and negative video signal. The AFC section is supplied by a separate operating voltage (maximum tuning voltage). This voltage is activated by mechanical switching to provide a simple AFC coupling. Both the positive video signal and the positive flyback pulse are used for gated control.

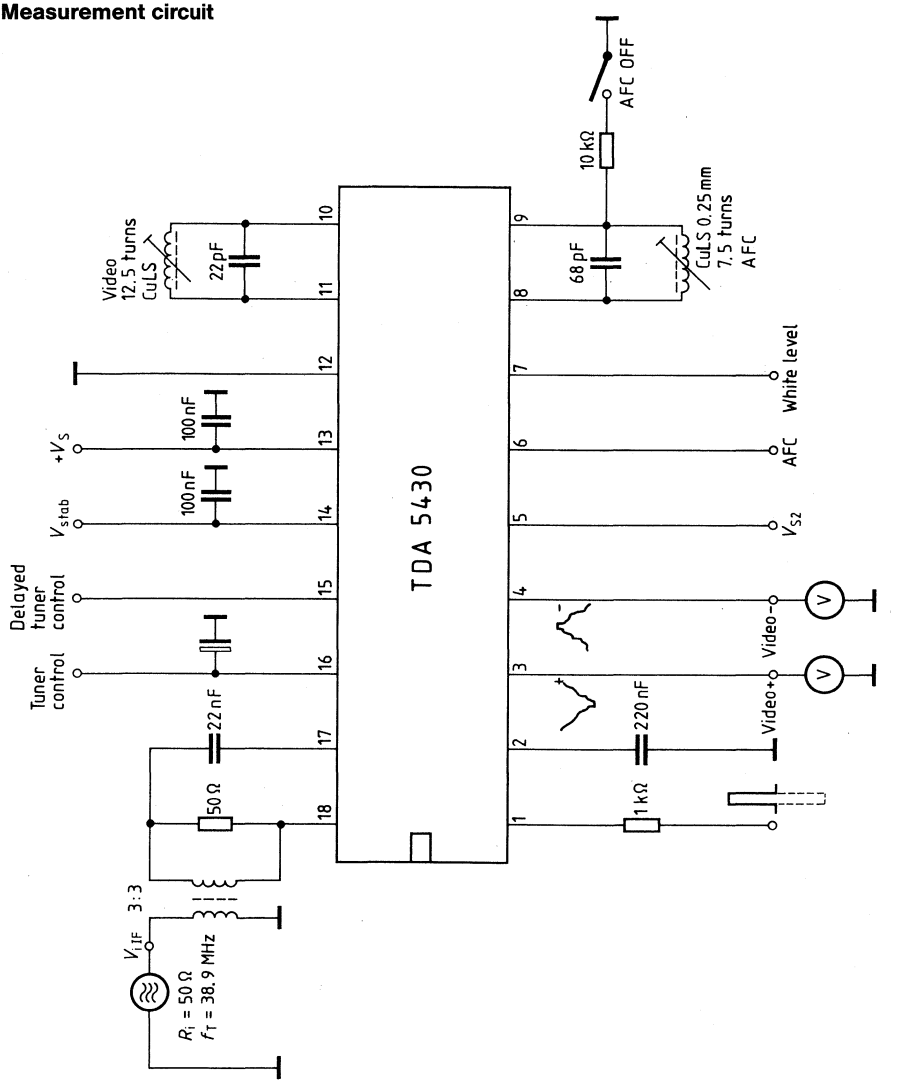
Pin designation

Pin No.	Function
1	Gating pulse
2	Time constant AGC
3	Positive video output
4	Negative video output
5	AFC supply voltage V_{S2}
6	AFC output
7	White level adjustment
8	AFC circuit
9	AFC circuit
10	Tank circuit
11	Tank circuit
12	Ground
13	Supply voltage $+V_{S1}$
14	Reference voltage
15	Tuner AGC
16	Delayed tuner AGC output
17	Video IF input
18	Video IF input

Block diagram



Measurement circuit



Bipolar circuit

Type	Ordering code	Package outline
TDA 5500	Q67000-A1377	DIP 16

The TDA 5500 is modulated after the TBA 1440 G. It contains – like the TBA 1440 G – a highly amplifying video IF amplifier, a controlled demodulator and two low-ohmic video outputs with positive and negative signals as well as a complete, gated control, and delayed tuner control.

The connection of pin 10 differs from the TBA 1440 G. While pin 10, included in the TBA 1440 G, adjusts the sync pulse level, the same pin is used as standard VCR connection in the TDA 5500. Switchover from VCR recording to playback is performed via pin 4.

Features

- Standard VCR connection
- Internal VCR switchover
- Gated control
- Positive and negative video output

Maximum ratings

Supply voltage	V_{13}	15[1])	V
Voltages	V_4	7	V
	V_5	15	V
Ohmic resistance between pin 8 and 9	$R_{8\text{-}9}$	$\leqq 20$	Ω
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	90	K/W

Operating range

Supply voltage range	V_{13}	10.5 to 15	V
Ambient temperature range	T_{amb}	−25 to 60	°C

1) intermittently 16.5 V

Characteristics ($V_{13} = 13$ V; $T_{amb} = 25$ °C; all data measured with respect to ground, unless otherwise stated)

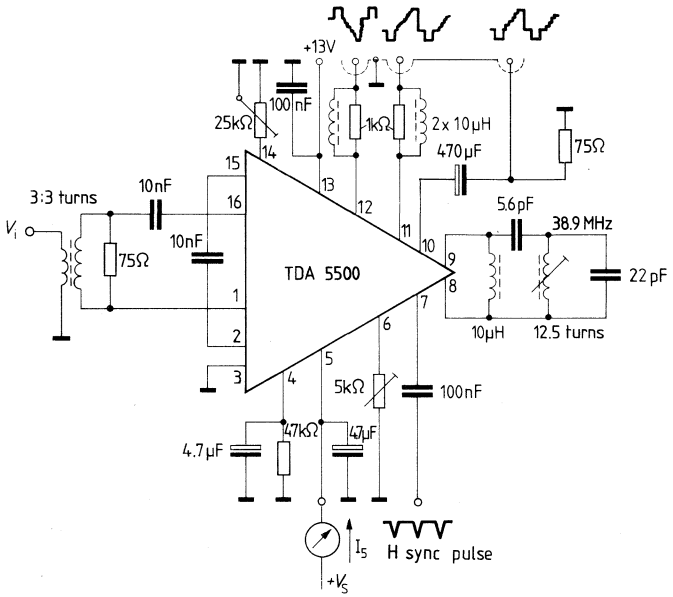
		min	typ	max	
Current consumption	I_{13}		55		mA
DC voltage at output 11 ($V_i = 0$)					
$R_{14\text{-}3} = \infty$	V_{11}		4.5		V
$R_{14\text{-}3} = 0$	V_{11}		7.5		V
DC voltage at output 12 ($V_i = 0$)					
$R_{14\text{-}3} = \infty$	V_{12}		1.5		V
$R_{14\text{-}3} = 0$	V_{12}		3		V
DC voltage at output 10 ($V_i = 0$)					
$R_{14\text{-}3} = \infty$	V_{10}		5.5		V
$R_{14\text{-}3} = 0$	V_{10}		8		V
Video amplification	$\frac{V_{11}}{V_{10}} = \frac{V_{12}}{V_{10}}$		3		
White level deviation	$\Delta V_{11}/V_{13}$		100		mV/V
	$\Delta V_{12}/V_{13}$		25		mV/V
AGC threshold = sync level	$V_{11\,sync}$		1.9		V
Sync pulse level with async or without gating pulses (peak level control)	$V_{11\,sync}$		1.5		V
Control current for tuner prestage ($V_5 \geqq 2$ V)	I_5	10	15		mA
Gating pulse voltage	$-V_7$	2		5	V
IF control voltage max. gain	V_4	0		0.5	V
min. gain	V_4	2		4	V
Voltage range VCR recording	V_4	0		4	V
VCR playback	V_4	4		6.5	V
Output current to ground	I_{11}; I_{12}			5	mA
to plus	I_{11}; I_{12}			−1	mA
Input impedance at max gain	$Z_{i1\text{-}16}$		1.8/2		kΩ/pF
at min gain	$Z_{i1\text{-}16}$		1.9/0		kΩ/pF
Output impedance	$Z_{q\,8\text{-}9}$		2/2.5		kΩ/pF
Output resistance VCR recording	R_{q10}		75		Ω
Input resistance VCR playback	R_{i10}		75		Ω
Input voltage[1]) for $V_{11} = 2$ V_{pp} (at $G_{V\,max}$)	V_i		180	250	µV
AGC range	ΔG		55		dB
Intermodulation ratio (1.07 MHz) with reference to color carrier[2])	a		45		dB

1) According to test circuit: V_1 = rms sync pulse level at 60 Ω

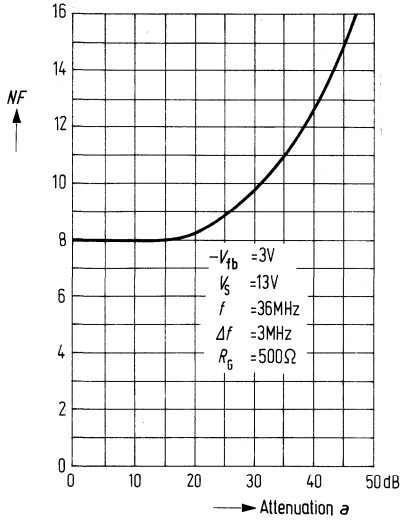
2) Test level $a_{CC} = -3$ dB

$a_{SC} = -20$ dB referred to picture carrier

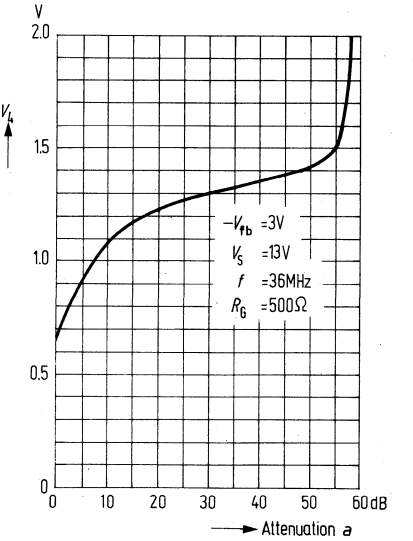
Test circuit



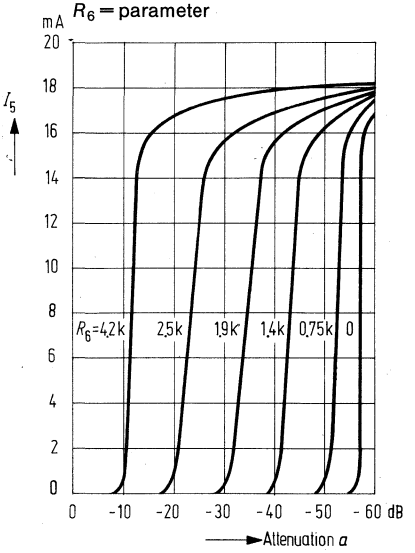
Noise figure versus attenuation
(measured at video frequency)
$V_S = 13$ V, $f = 36$ MHz, $\Delta f = 3$ MHz,
$R_G = 500\ \Omega$, $-V_{fb} = 3$ V



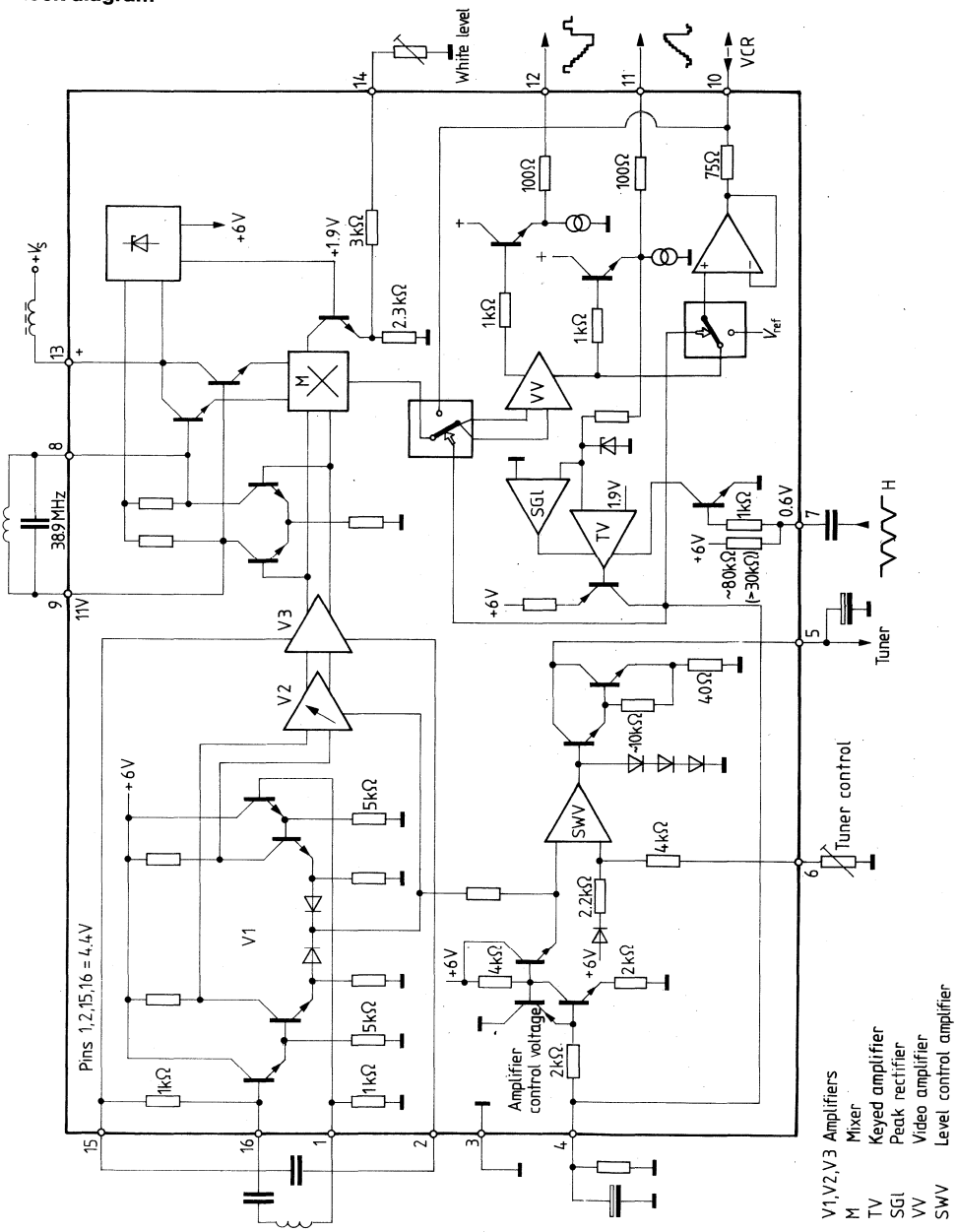
Control voltage versus attenuation
$-V_{fb} = 3$ V, $V_S = 13$ V, $f = 36$ MHz,
$R_G = 500\ \Omega$



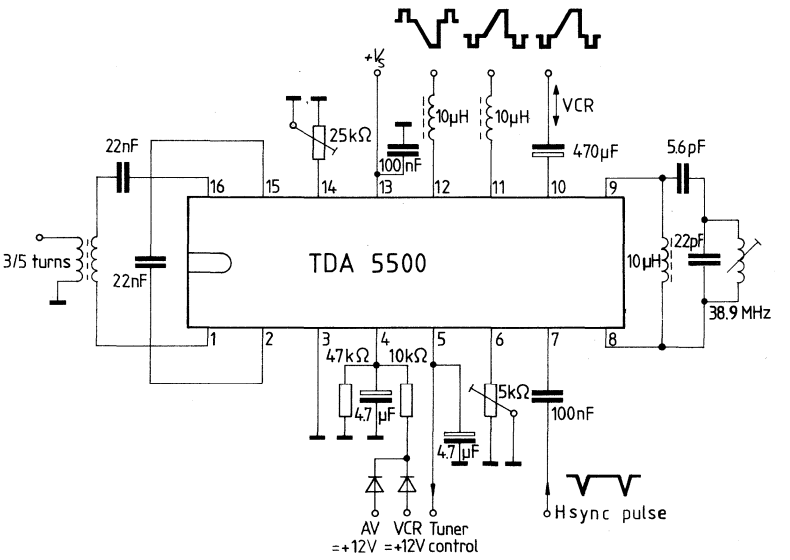
Tuner control current versus attenuation
R_6 = parameter



Block diagram



Application circuit



Preliminary data **Bipolar circuit**

Type	Ordering code	Package outline
TDA 5510	Q67000-A2196	DIP 16

The TDA 5510 includes a controlled AM broadband amplifier equipped with a synchronous demodulator, a high gain controllable video IF amplifier and a VCR input/output. In addition, a generation circuit provides the control voltage for the IF amplifier and the PNP tuner.

Features

- Standard VCR connection
- Internal VCR switchover
- Gated control
- Positive and negative video output

Maximum ratings

Supply voltage	V_S	16.5	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	70	K/W

Operating voltage

Supply voltage range	V_S	10.5 to 15.8	V
IF frequency range	f_{IF}	50 to 60	MHz
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics ($V_S = 13$ V; $T_{amb} = 25$ °C)

		min	typ	max	
Current consumption	I_{11}		60		mA
Stabilized reference voltage	$V_{12/10}$		6.0		Vdc
Control current for tuner ($V_{14} = 0.5\ V_{11}$)	I_{14}		4.0		mA
Tuner AGC threshold	$V_{13/10}$			4.0	Vdc
Gating pulse voltage					
pos. gating pulse	V_1		+3.0		V
neg. gating pulse	V_1		−3.0		V
Input voltage at G_{max} ($V_{3\,pp} = 3$ V)	$V_{15/16}$			100	μV
AGC range	ΔG		60		dB
IF control voltage					
G_{max}	$V_{2/10}$	0			Vdc
G_{min}	$V_{2/10}$			4.0	Vdc
VCR switchover	$V_{2/10}$	8.0		V_{11}	Vdc
Video output voltage (pos.) ($R_L = \infty$)	$V_{3\,pp}$		3.0		V
Sync pulse level	$V_{3/10}$		2.0		Vdc
DC voltage ($V_2 = 4$ V; $V_{15/16} = 0$)	$V_{3/10}$		5.3		Vdc
Output current					
(to ground through R)	$I_{q\,3}$		−5.0		mA
(to plus $V_3 = 7$ V)	$I_{q\,3}$		+2.0		mA
Video output voltage (neg.) ($R_L = \infty$)	$V_{q\,4\,pp}$		3.0		V
Sync pulse level	$V_{q\,4/10}$		V_{11}−2.0		Vdc
DC voltage ($V_2 = 4$ V; $V_{15/16} = 0$)	$V_{q\,4/10}$		V_{11}−5.3		Vdc
Output current					
(to ground through R)	$I_{q\,4}$		−5.0		mA
(to plus $V_4 = V_{11}$)	$I_{q\,4}$		+1.0		mA
VCR output voltage (neg.)					
VCR recording ($R_L = \infty$)	$V_{q\,5\,pp}$		2.0		V
Sync pulse level					
VCR recording	$V_{5/10}$		V_{11}−1.6		Vdc
DC voltage ($V_2 = 4$ V; $V_{15/16} = 0$)					
VCR recording	$V_{5/10}$		V_{11}−3.8		Vdc
DC voltage ($V_2 \geq 8$ V)					
VCR playback	$V_{5/10}$		V_{11}−0.9		Vdc
Output current					
(to ground through R)	$I_{q\,5}$		−5.0		mA
(to plus $V_5 = V_{11}$)	$I_{q\,5}$		+1.0		mA
Video amplifier					
VCR playback					
($V = V_3/V_6$; $V_{6\,pp} = 1$ V)	G		3.0		

Additional application data[1])

Input impedance	$Z_{i15/16}$	1.8/2	kΩ/pF
Output impedance	$Z_{q\,8/9}$	6.6/2	kΩ/pF
Output resistance	$R_{q\,3}$	150	Ω
Output resistance	$R_{q\,4}$	150	Ω
Output resistance	$R_{q\,5}$	150	Ω
Residual IF(basic frequency)	$V_3; V_4$	10	mV
Video bandwidth (−3 dB)			
VCR recording	B_{video}	6.0	MHz
VCR playback V_6	B_{video}	10.0	MHz
Intermodulation ratio with reference to f_{FT} (1.07 MHz)	a	45	dB

Circuit description

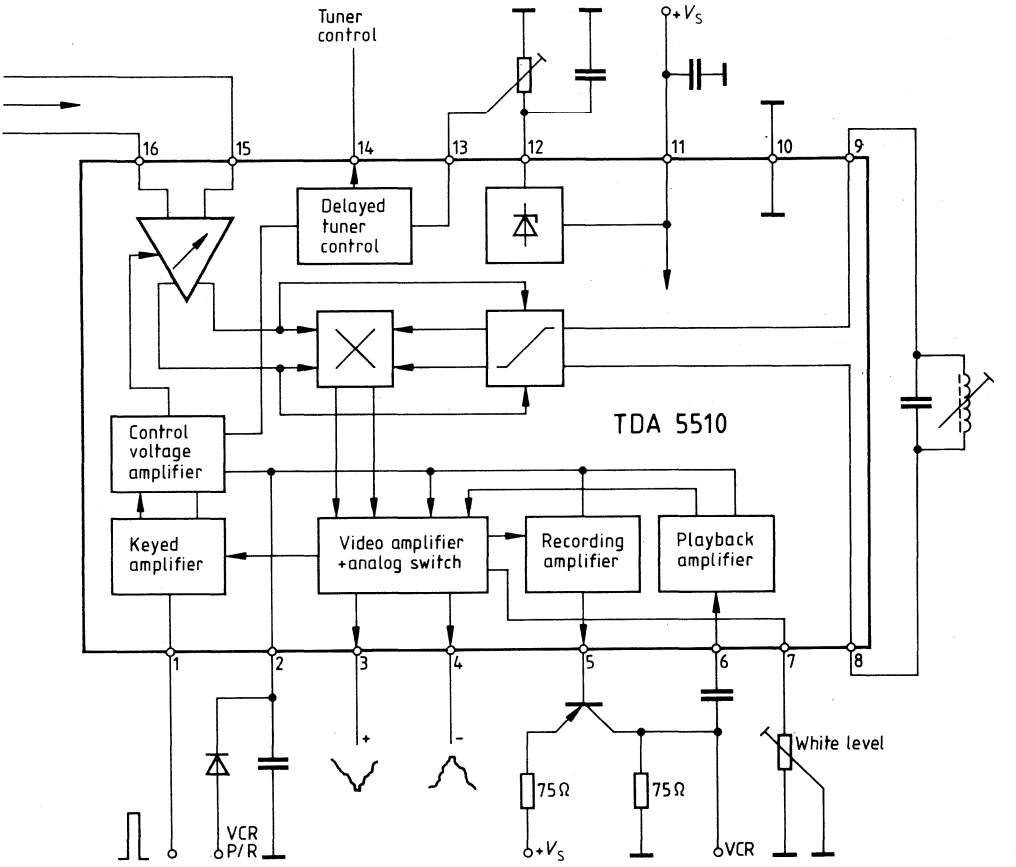
The integrated circuit is comprised of a 4-stage controllable AM amplifier, a limiter and mixer for synchronous demodulation of the video signals as well as an amplifier for both the positive and negative video output signal. The positive video signal as well as the positive flyback pulse are used for gated control. In addition, the component includes a standard VCR connection via an external transistor. The delayed tuner AGC is generated by a threshold amplifier driven by the control voltage.

Pin configuration

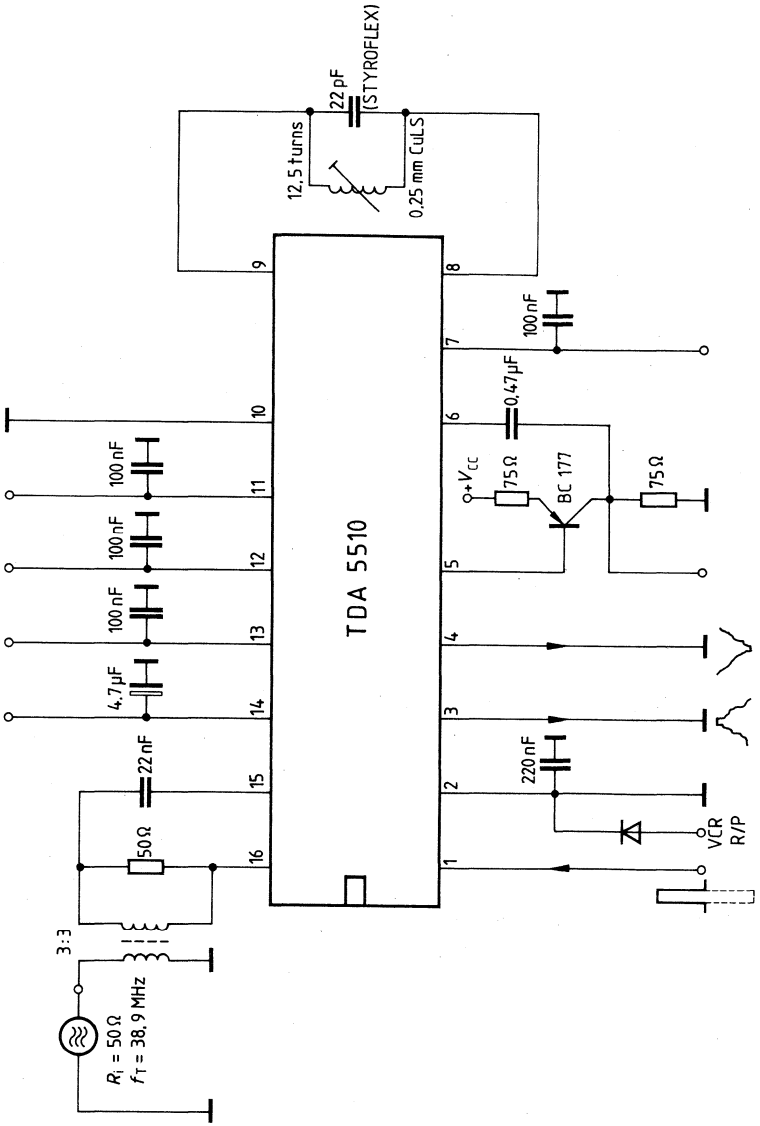
Pin No.	Function
1	Gating pulse
2	Time constant AGC; switchover VCR recording/playback
3	Positive video output
4	Negative video output
5	VCR output
6	VCR input
7	White level adjustment
8	Tank circuit
9	Tank circuit
10	Ground
11	Supply voltage
12	Reference voltage
13	Tuner AGC
14	Delayed tuner AGC output
15	Video IF input
16	Video IF input

1) not measured

Block diagram



Measurement circuits



Preliminary data **Bipolar circuit**

Type	Ordering code	Package outline
TDA 5620	Q67000-A2214	DIP 18

The TDA 5620 has been designed as a synchronous demodulator for use in PAL color TV receivers. The chroma signal received at the input is subsequently amplified and demodulated to provide +(R-Y) and +(B-Y) output signals for further processing by the video processor.

Features

- Economic design
- Few external components
- Individualized functions to ensure flexible structure

Maximum ratings

Supply voltage	V_{18}	0 to 14.4	V
Supply current	I_{18}	55	mA
Power dissipation	P_V	800	mW
Input voltage	V_{i1}	0 to 12	V
Output voltage	V_{q4}	0 to V_{18}	V
Input voltage (preliminary)	V_{i7}	−3 to V_{18}	V
Input voltage	$V_{i8/11}$	0 to 7	V
Output voltage	$V_{q12/13}$	0 to V_{18}	V
Voltage	$V_{15/16}$	0 to 8	V
Input voltage	V_{i17}	−4 to 4	V
Current	$I_{2/3}$	−10 to 5	mA
Output current	I_{q4}	−20	mA
Current	$I_{5/6}$	−3 to 3	mA
Output current	$I_{q12/13}$	−1 to 5	mA
Output current	I_{q14}	−10 to 0.3	mA
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	70	K/W

Operating range

Supply voltage (preliminary)	V_S	9.6 to 14.4	V
Ambient temperature range	T_{amb}	−20 to 70	°C

Characteristics ($V_S = 12$ V; $T_{amb} = 25$ °C)

		Test circuit	min	typ	max	
Supply current	I_{S18}	1	28	37.5	47	mA
Input voltage	V_{i1}	1	5.1	5.7	6.3	V
Output voltage	V_{q4}	1	7.6	8.5	9.4	V
Voltage	$V_{5/6}$	1	6.2	7.7	9.2	V
Input voltage	$V_{i8/11}$	1	2.2	2.5	2.8	V
Output voltage	$V_{q12/13}$	1	9.5	10.3	11.1	V
Voltage	V_{14}	1	8.7	9.5	10.7	V
Voltage	$V_{15/16}$	1	2.7	3.3	3.9	V
Voltage	V_2	1	4.3	4.7	5.3	V
Gating pulse at pin 17						
Burst output voltage ($v_{Bi1\,pp} = 0.1$ V)	$v_{Bq4\,pp}$	2	0.45	0.75	1	V
Chroma control (referred to $v_{Bq4\,pp}$ at $v_{Bi1} = 0.1$ V) ($v_{Bi1\,pp} = 0.2$ V)	A_{CC1}	2	−1	0	1	dB
Chroma control (referred to $v_{Bq4\,pp}$ at $v_{Bi1} = 0.1$ V) ($v_{Bi1\,pp} = 10$ mV)	A_{CC2}	2	−5	−2	1	dB
Output voltage R-Y Standard color bar ($v_{Bi1\,pp} = 0.1$ V)	$v_{q12\,pp}$	2	1.0	1.4	1.8	V
Output voltage B-Y Standard color bar ($v_{Bi1\,pp} = 0.1$ V)	$v_{q13\,pp}$	2	1.0	1.4	1.8	V
Output voltage variation Standard color bar ($v_{Bi1\,pp} = 0.1$ V) ($V_S = 12$ V ± 20%)	$\Delta q_{q12/13\,pp}$	2	±0.15	±0.35	±0.55	V
Output voltage variation Standard color bar ($v_{Bi1\,pp} = 0.1$ V) ($T_{amb} = -20$ to 70 °C)	$\Delta q_{q12/13\,pp}$	2	±0.05	±0.2	±0.35	V
Demodulator output residual carrier without input signal	$v_{q12\,pp}$	2			0.2	V
Demodulator output residual carrier without input signal	$v_{q13\,pp}$	2			0.2	V
Residual signal[1])	v_{q12}	2			10	mV
Residual signal[1])	v_{q13}	2			10	mV
Color killer level (referred to $v_{Bi1\,pp} = 0.1$ V)	v_{K1}	2	−38	−30	−25	dB
Residual signal[1])	$v_{OFF\,pp}$	2			10	mV
Difference output voltage (B-Y)[3])	$v_{q13\,pp}$	3	0.8	1.1	1.5	V
Ratio of output voltage[3])	v_{q13}/v_{q12}	3	0.85	1	1.15	

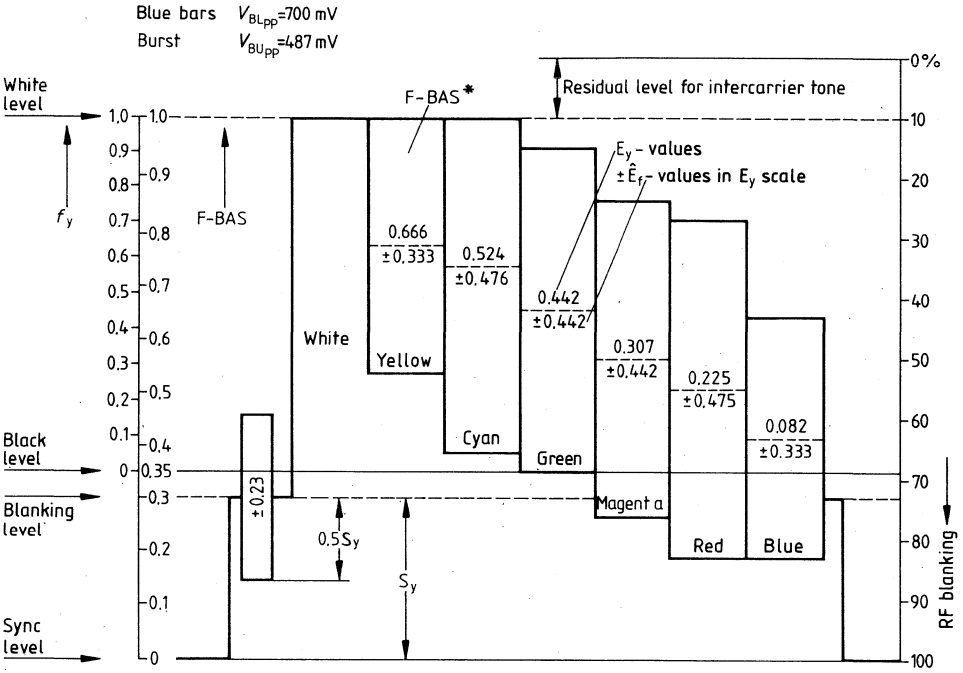
For footnotes refer to page 566 . . . 568

Characteristics ($V_S = 12$ V; $T_{amb} = 25$ °C)

		Test circuit	min	typ	max	
Free run frequency after adjustment; pin 5-6 short pin 8 without signal ($f_{center} = 4{,}433{,}658$ Hz)	f_0	3			±250	Hz
Frequency variation pin 5-6 short ($V_S = 12$ V ±20%)	Δf_{01}	3			±80	Hz
Frequency variation pin 5-6 short ($T_{amb} = -20$ to 70 °C)	Δf_{02}	3			±200	Hz
Supply voltage of OSC start	V_S	3			8	V
VCO control sensitivity ($v_{Bi\,8\,pp} = 0.7$ V) Voltage measurement at pin 5-6 at 100 Hz Burst frequency variation	β	3	1.0	1.8	2.6	Hz/mV
Phase detector sensitivity ($v_{Bi\,8\,pp} = 0.7$ V) Voltage measurement at pin 5-6 during phase variation by means of 100 Hz burst frequency variation	μ	3	18	25	45	mV/degrees
Capture range ($v_{Bi\,8\,pp} = 0.7$ V) Measurement at different burst frequencies	f_P	3	0.8			kHz
Phase deviation ($v_{Bi\,8\,pp} = 0.7$ V) Variation of the phase by means of burst frequency variation 100 Hz	$\Delta\Phi$	3	0	0.03	0.05	degrees/Hz
Input resistance ($f = 4.43$ MHz) ($v_{Bi\,1\,pp} = 100$ mV)	R_{i1}	4	2.0	2.8	3.6	kΩ
Input capacitance ($f = 4.43$ MHz) ($v_{Bi\,1\,pp} = 100$ mV)	C_{i1}	4			10	pF
Delay time of the H-blanking[4] measured between pin 7 and pin 13	t_F	2			1.7	µs

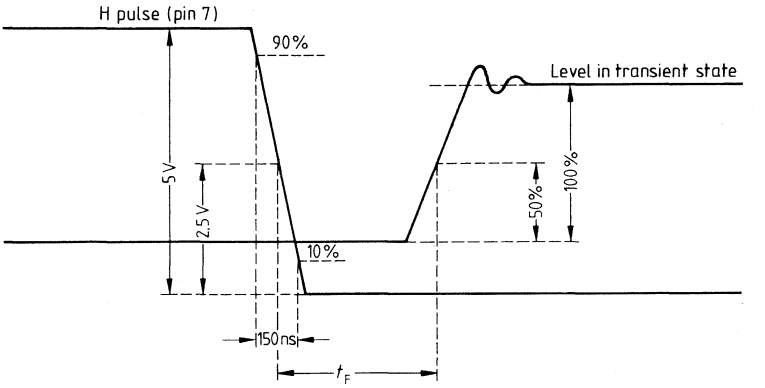
1) Reduce burst input signal, until color killer responds
2) Standard operating demodulator residual voltage with output transistor switched off by the emitter follower circuit.
3) Refer to test circuit 3, page 567
4) Refer to pulse diagram, page 568
$v_{Ri\,pp}$ = Demodulator input voltage 700 mV – rainbow signal
$v_{Bi\,1}$ = Burst input voltage at pin 1
$v_{Bi\,8}$ = Burst input voltage at pin 8

Standard color bar at input F-BAS of the test circuit 3



*) F BAS ≙ composed video signal input

Pulse diagram



Circuit description

The major functions of the TDA 5620 are illustrated in the block diagram on page 569. The chroma signal at pin 1 is forwarded to the controlled chroma amplifier. Subsequent to the chroma amplifier, a driver stage is included for the delay line. U and V components are generated in the internal matrix stages (U and V matrix). By selecting this particular design, the ultrasound delay line can be used by both the SECAM and PAL signals. The low-pass filters for the carrier suppression of the synchronous demodulators are connected at pins 12 and 13.

The reference oscillator operates at 4.4 MHz. The 90° reference for the V-demodulator is generated internally, while the phase position can be adjusted by an external capacitance (pin 16).

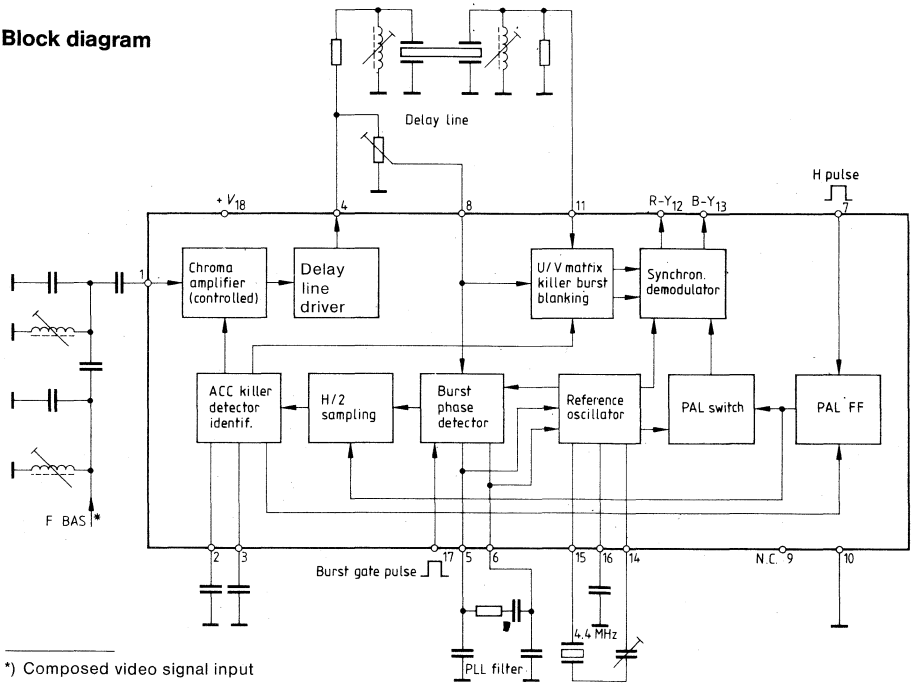
The separated burst of the non-delayed chroma signal component (pin 8) serves as information source for the burst phase synchronization process as well as the chroma control voltage gain and color killer functions.

Separate inputs forward the required auxiliary pulses. The burst gate pulse is present at pin 15, while the H-blanking pulse is forwarded to pin 7. The +(R−Y) and +(B−Y) signals are applied as output signals. The (G−Y) matrix is included in the video processor.

Pin configuration

Pin No.	Function
1	Composed video signal input
2	ACC killer detector clamping capacitor
3	ACC killer detector clamping capacitor
4	Delay line output driver
5	Burst phase detector (PLL-filter connection)
6	Burst phase detector (PLL-filter connection)
7	H-pulse input
8	Input U/V matrix (undelayed)
9	N.C.
10	Ground
11	Input U/V matrix (delayed)
12	Output R-Y
13	Output B-Y
14	Reference oscillator (crystal connection)
15	Reference oscillator (crystal connection)
16	Phase correction (oscillator)
17	Input burst gate pulse
18	Supply voltage

Block diagram



*) Composed video signal input

Test and measurement circuit 1

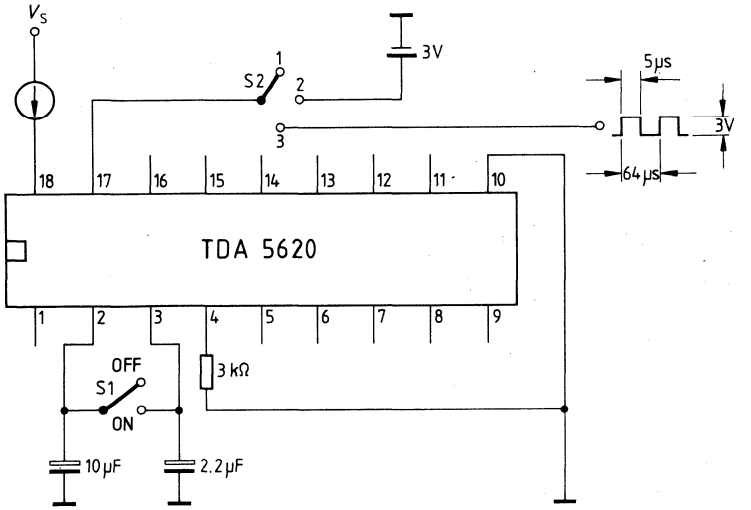


Table 1:

F	S1	S2
1	ON	1
2	ON	1
3	OFF	1
4	ON	2
5	ON	2
6	ON	1
7	ON	1
8	ON	1
9	ON	1
10	ON	2
11	ON	1
12	ON	1
13	OFF	3

Test and measurement circuit 2

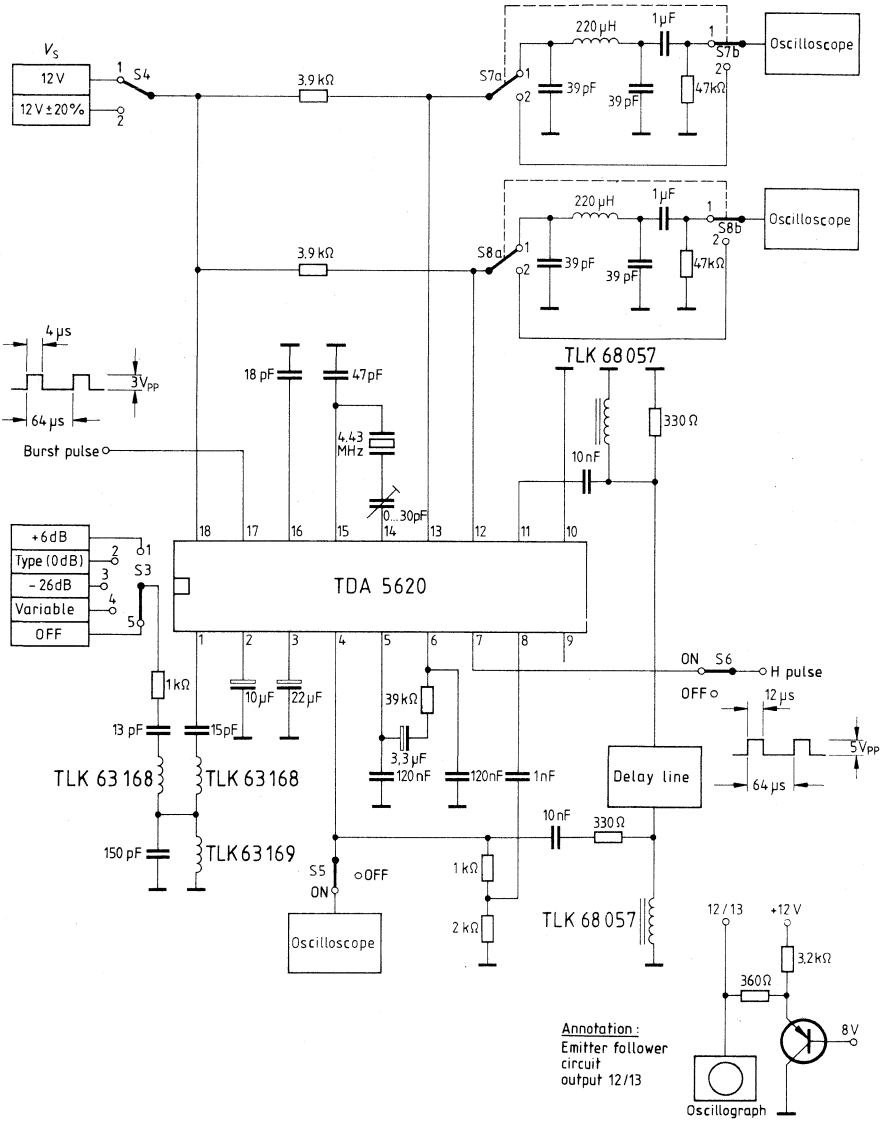


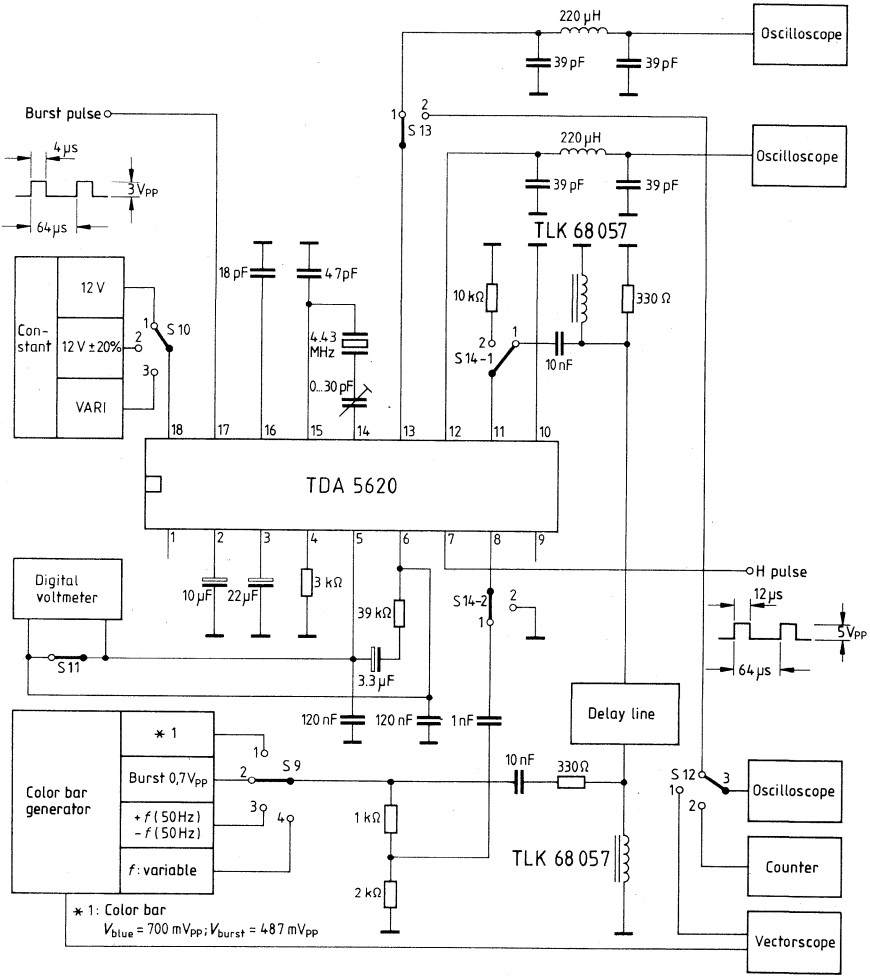
Table 2 (to test and measurement circuit 2)

F	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	42
S3	2	1	3	2	2	2	2	2	2	5	5	4	4	4	2	2
S4	1	1	1	1	1	2	2	1	1	1	1	1	1	1	1	1
S5	on	on	on	off	off	off	off	off	off	off	off	off	off	off	off	off
S6	on	on	on	on	on	on	on	on	on	on	on	off	off	on	on	on
S7 a b	1	1	1	1	1	1	1	1	1	2	2	1	1	1	2	1
S8 a b	1	1	1	1	1	1	1	1	1	2	2	1	1	1	2	1

Table 3 (to test and measurement circuit 3)

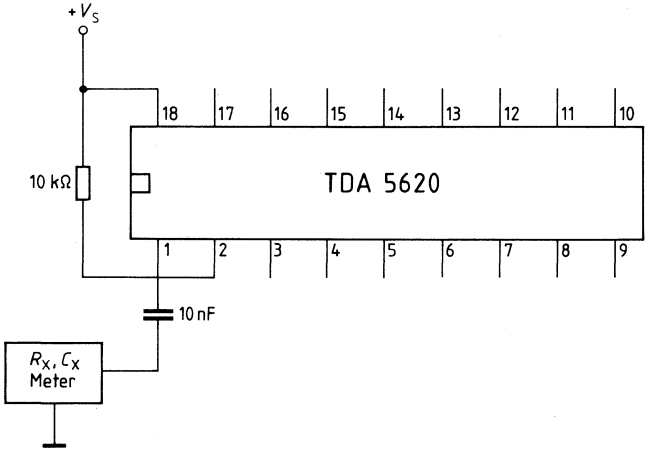
F	30	31	32	33	34	35	36	37	38	39
	1	1	2	2	2	2	3	3	4	3
	1	1	1	2	1	3	1	1	1	1
	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	OFF	OFF
	—	—	2	2	2	1	2	3	1	3
	1	1	2	2	2	2	2	2	2	2
	1	1	2	2	2	2	2	1	1	1

Test and measurement circuit 3

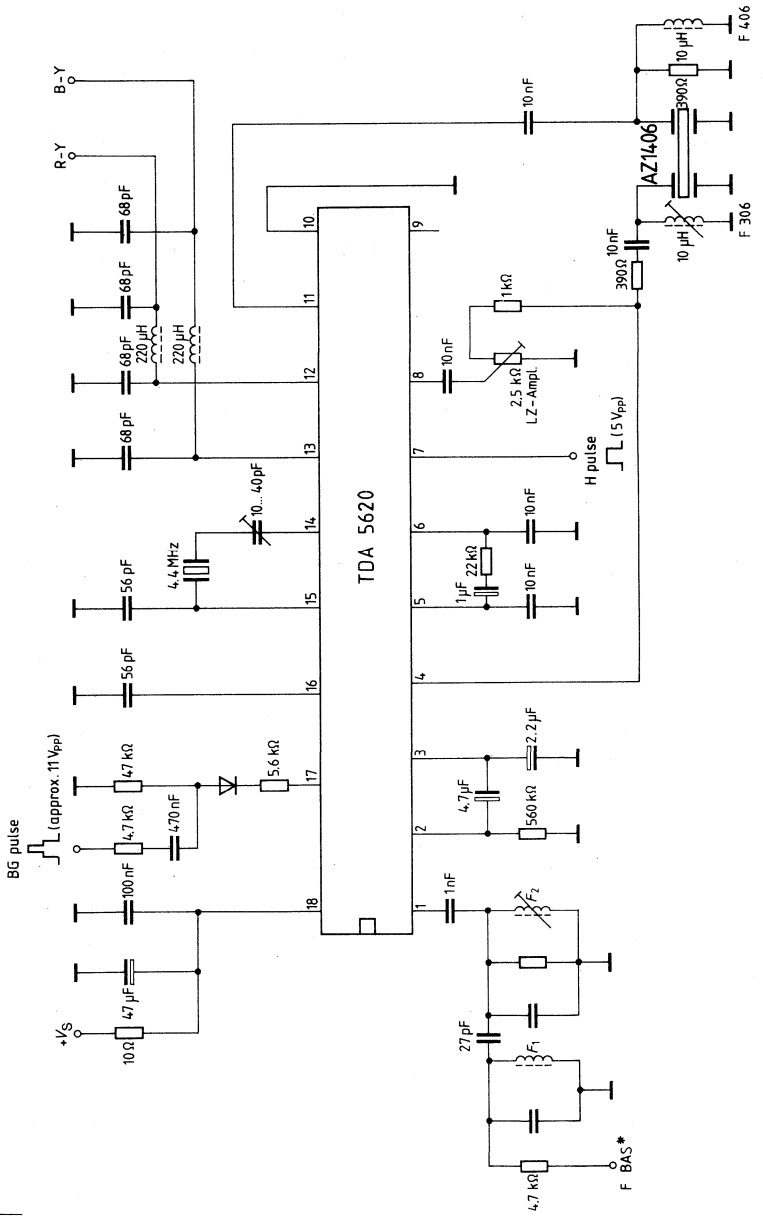


Test and measurement circuit 4

With the exception of pin 1, test circuit 4 is identical to test circuit 2



Application circuit



*) Composed video signal input

Preliminary data **Bipolar circuit**

Type	Ordering code	Package outline
TDA 5630	Q67000-A2215	DIP 24

The TDA 5630 has been designed as a SECAM color decoder and system changeover switch for color TV receivers equipped with automatic standard or SECAM standard switching. The component generates +(R-Y) and +(B-Y) output signals for further processing by the video processor.

Features

- Automatic switchover for multistandard reception
- Economic design
- Few external components
- Individualized functions to ensure flexible structure

Maximum ratings

Supply voltage	V_{24}	0 to 14.4	V
Supply current	I_{24}	52	mA
Power dissipation	P_V	760	mW
Voltages	V_4	−4 to 4	V
	V_5	0 to 7.5	V
	V_8	0 to 10	V
	V_{10}	0 to 8	V
	$V_{11/12/13}$	0 to V_{24}	V
	V_{14}	0 to 8	V
	V_{16}	0 to 10	V
	V_{18}	−3 to V_{24}	V
	V_{19}	0 to 7.5	V
	$V_{21/22/23}$	0 to 8	V
Currents	$I_{1/2}$	−0.5 to 10	mA
	I_3	−10 to 3	mA
	I_7	−5 to 0.5	mA
	$I_{9/15}$	−1 to 1	mA
	$I_{11/13}$	−1 to 5	mA
	I_{17}	−5 to 0.5	mA
	I_{20}	−20 to 0	mA
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	65	K/W

Operating range

Supply voltage range	V_S	9.6 to 14.4	V
Ambient teperature range	T_{amb}	−20 to 70	°C

Characteristics ($V_S = 12$ V; $T_{amb} = 25$ °C)

		Switch position	Test circuit	min	type	max	
Supply current	I_S	2/3	1	20	29	37	mA
Voltages	$V_{1/2}$	2/3	1	4.9	5.7	6.4	V
	$V_{5/19}$	2/3	1	1.8	2.4	3.0	V
	$V_{7/17}$	2/3	1	10.6	11.2	11.8	V
	$V_{8/16}$	2/3	1	4.7	5.4	6.1	V
	$V_{9/15}$	2/3	1	6.3	7.2	8.0	V
	$V_{10/14}$	2/3	1	2.5	3.3	4.0	V
	$V_{11/13/20}$	2/3	1	6.8	7.9	9.0	V
	V_{21}	2/3	1	2.6	3.3	4.0	V
	V_{22}	2/3	1	2.3	3.0	3.7	V
	$V_{9/11/13/15}$	2/1	1	11.7	11.9	V_S	V
	V_{12}	2/2	1	0.85	1.10	1.30	V
	V_{12}	1/2	1	0	0.1	0.2	V
	V_{12}	3/2	1	0	0.1	0.2	V
Limiter output voltage pin 20 Standard color bar signal (100 mV) measured pin 20 S3:3; S4:1; S5:1; S6:2	$v_{q\,20\,pp}$		2	1.7	2.2	2.7	V
Limiter output voltage pin 20 Standard color bar signal (−30 dB) measured pin 20 S3:3; S4:1; S5:1; S6:2	$v_{q\,20\,pp}$		2	0.6	1.4	2.4	V
Gain PAL amplifier Sine signal 4.43 MHz (300 mV_{PP}) output voltage pin 20 at pin 21 input signal S3:1; S4:1; S5:2; S6:2	G_{PAL}		2	0.95	1.0	1.3	fold
SECAM permutator discriminator (B-Y) Standard color bar signal S3:2; S4:3; S5:1; S6:2	$v_{q\,11\,pp}$		2	0.6	1.0	1.3	V
SECAM switch discriminator (R-Y) Standard color bar signal S3:2; S4:2; S5:1; S6:2	$v_{q\,13\,pp}$		2	0.7	1.2	1.6	V
SECAM switch discriminator (B-Y) Standard color bar signal (−16 dB) S3:2; S4:3; S5:1; S6:2	$v_{q\,11\,pp}$		2	0.6	1.0	1.3	V
SECAM switch discriminator (R-Y) Standard color bar signal (−16 dB) S3:2; S4:2; S5:1; S6:2	$v_{q\,13\,pp}$		2	0.7	1.2	1.6	V
Color killer tolerance Attenutation of the input signal at color killer operation S3:3; S4:3; S5:1; S6:2	dP		2	−34	−27	−20	dB

Characteristics ($V_S = 12$ V; $T_{amb} = 25$ °C)

		Test circuit	min	typ	max	
System discriminator SECAM signal weak input Standard color bar signal (—40 dB) S3:2; S4:3; S5:1; S6:2	V_{i12}	2	0.9	1.05	1.2	V
System discriminator SECAM signal small input Standard color bar signal (—18 dB) S3:2; S4:3; S5:1; S6:2	V_{i12}	2	0	0.05	0.2	V
System discriminator PAL signal Voltage of pin 1 against pin 2 at the PAL signal input and 100 mV_{PP} burst signal S3:2; S4:3; S5:1; S6:1	$V_{1\text{-}2}$	2			±0.1	V
Permutator crosstalk Standard color bar signal The ratio of output voltage at pin 13 against 1 H delayed S7:2; S4:2; S3:2; S5:1; S6:2	a	2		—62	—50	dB
Permutator crosstalk Standard color bar signal The ratio of output voltage at pin 11 against 1 H delayed S7:2; S4:2; S7:3; S4:3; S3:2; S5:1; S6:2	a	2		—60	—50	dB
PAL-SECAM switching circuit crosstalk Standard color bar signal Leakage of PAL signal at SECAM switch S3:3; S4:1; S5:2; S6:2	a	2		—33	—30	dB
PAL-SECAM switching circuit crosstalk Standard color bar signal (—26 dB) Leakage of SECAM signal when switching PAL/SECAM S3:1; S4:1; S5:1; S6:1	a	2		—53	—45	dB
Minimum operating voltage for SECAM cross switch FF	V_{i18}		0.70	0.80	0.95	V
Burst gate minimum operating voltage	V_{i4}		0.65	0.77	0.90	V

Annotation: S_7 in position 2 for test 12, 13
S_7 in position 1 for the other tests

Circuit description

The chroma signal is received at the input (pin 23) via the cloche filter. The input limit amplifier is followed by the signal switch, which receives both the SECAM chroma signal and the PAL chroma signal generated by the PAL decoder. This switch is controlled by the system identification component (automatic standard switchover). According to the standard used, either the SECAM or the PAL signal is switched by the buffer stage to the delay line. The signals for D_B lines (blue) as well as for the D_R lines (red) are forwarded to the SECAM cross switch, which in turn distributes the signals to the respective discriminator. Control is effected through the included flipflop component.

Subsequent to the demodulation process the external *RC* links activate the video deemphasis mode. At the same time, a standard depending switch-over of the dc level is performed on the output levels. As with the PAL decoder, +(R-Y) and +(B-Y) signals are generated as output signals.

Only H-identification is used for identification purposes. Toward this end, a burstgate pulse separates from the signal the so-called SECAM bursts, which correspond to the respective zero frequencies of the carriers for red and blue lines. After separation, they are forwarded by the burstgate pulse to the evaluation circuit. This circuit operates with a high quality resonant circuit. Its resonance frequency is adjusted to the zero frequency for D_B lines. As a result, the amplitude of the burst signals differ widely, clearly identifying the D_B and D_R lines. By comparing the H/2 signal of the flipflop, its correct switching mode is established.

For the purpose of norm recognition, the burst signals are gated and the blanking values are stored by means of external capacitances (pins 1 and 2). Only with the SECAM signal a noticeable voltage difference becomes apparent between pin 1 and 2, since PAL and NTSC signals or noise interference do not generate the same effect. Therefore this singular occurrence enables a clear norm recognition.

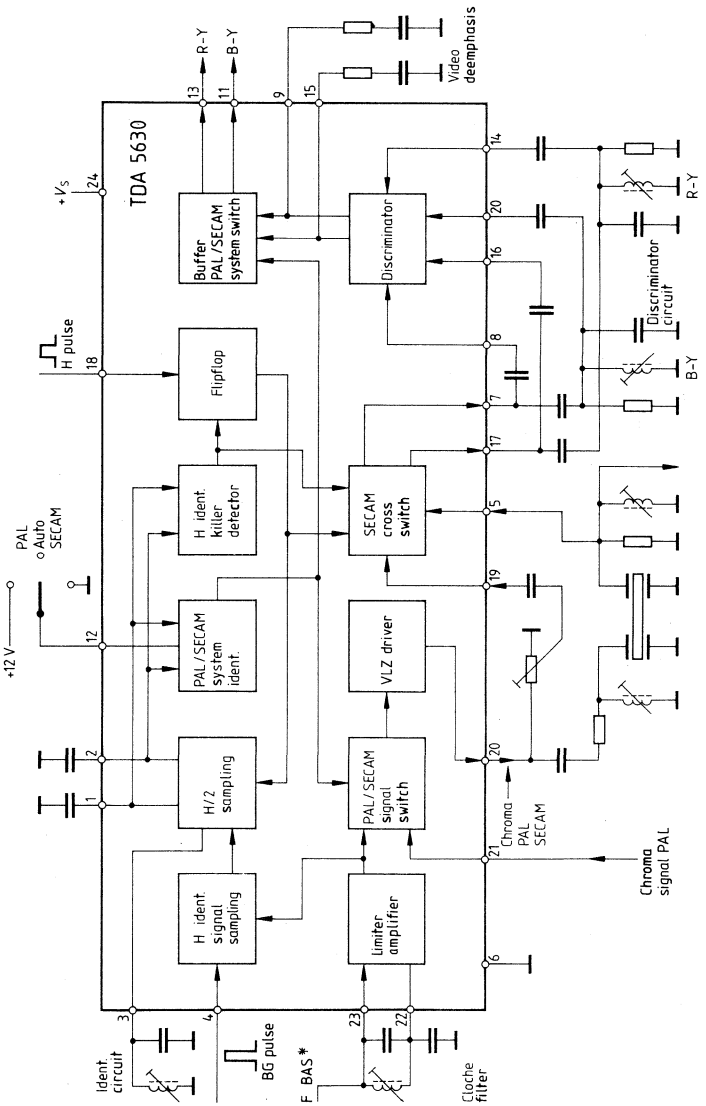
Since the voltage difference decreases progressively during weak or noisy SECAM signals, this effect can be used as information for the color killer.

The burstgate pulses are forwarded via pin 4, while the H-blanking pulses are wired to pin 18.

Pin configuration

Pin No.	Function
1	TP H/2 sampling
2	Tp H/2 sampling
3	Color carrier circuit
4	Burst gate input
5	Line switch – input delayed
6	Ground
7	SECAM cross switch – output B-Y
8	Discriminator circuitry
9	Video deemphasis
10	Discriminator circuitry
11	B-Y output
12	PAL – SECAM switchover
13	R-Y output
14	Discriminator circuitry
15	Video deemphasis
16	Discriminator circuitry
17	SECAM cross switch – output R-Y
18	H-pulse input
19	Line switch – input undelayed
20	Chroma switch – output (PAL – SECAM)
21	Chroma input (PAL)
22	Composed video signal input
23	Composed video signal input
24	Supply voltage

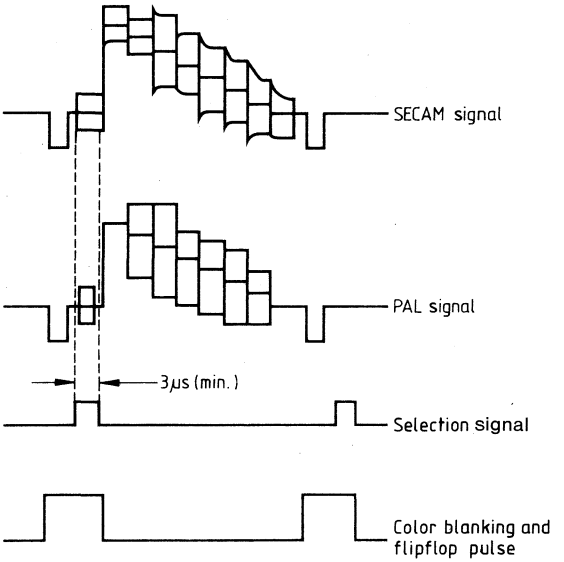
Block diagram



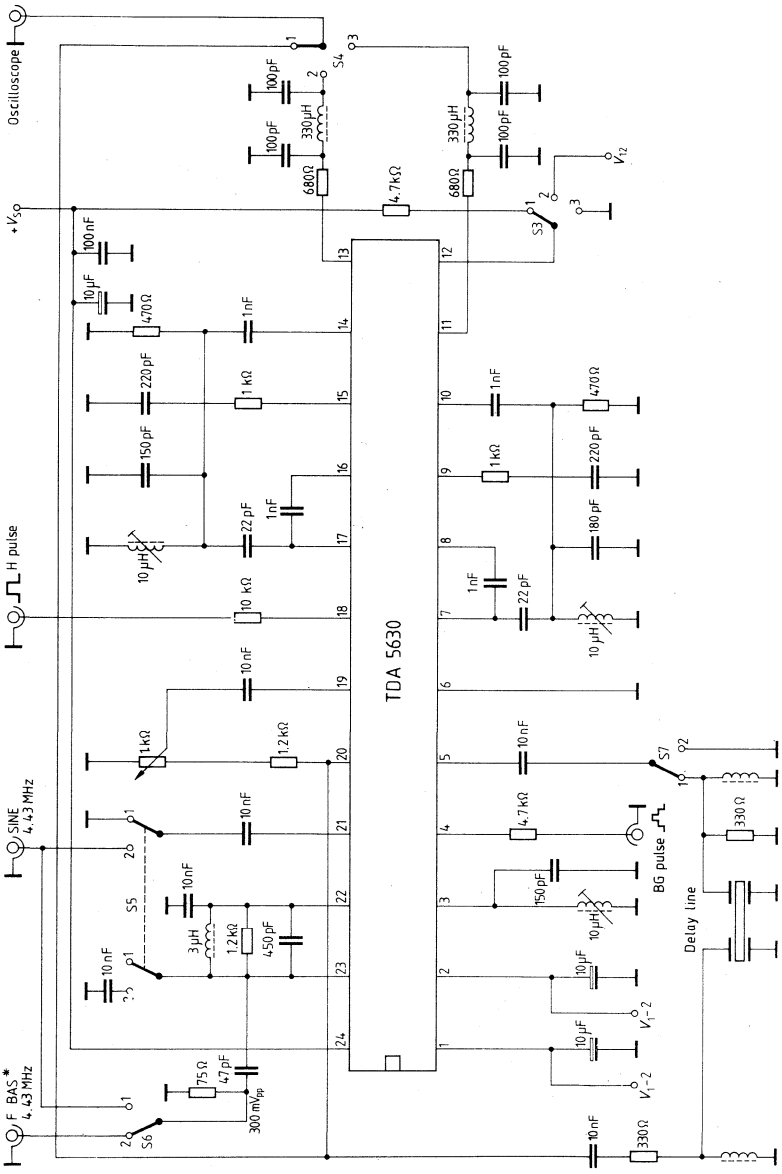
*) Composed video signal input

Pulse diagram

System selection pulse against FF gate pulse

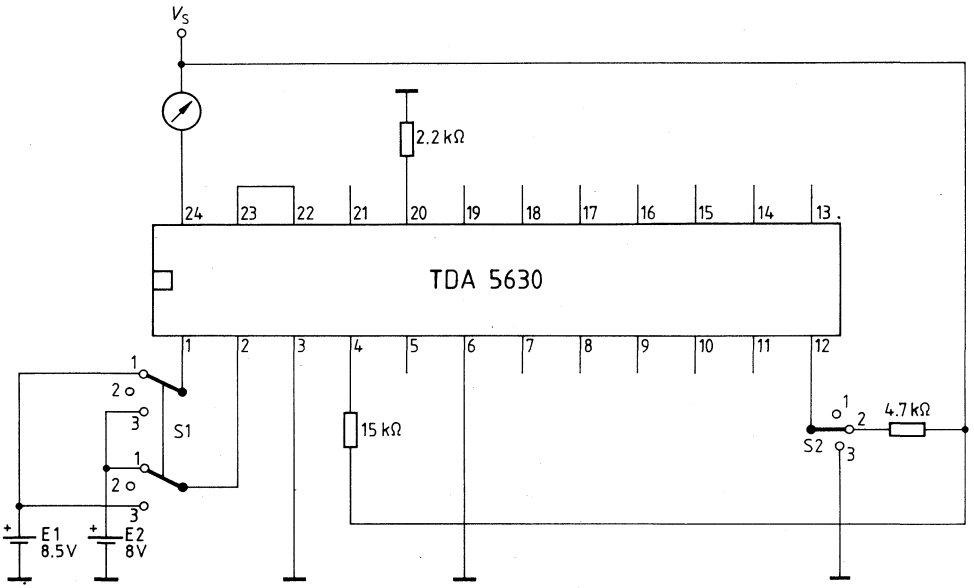


Test circuit

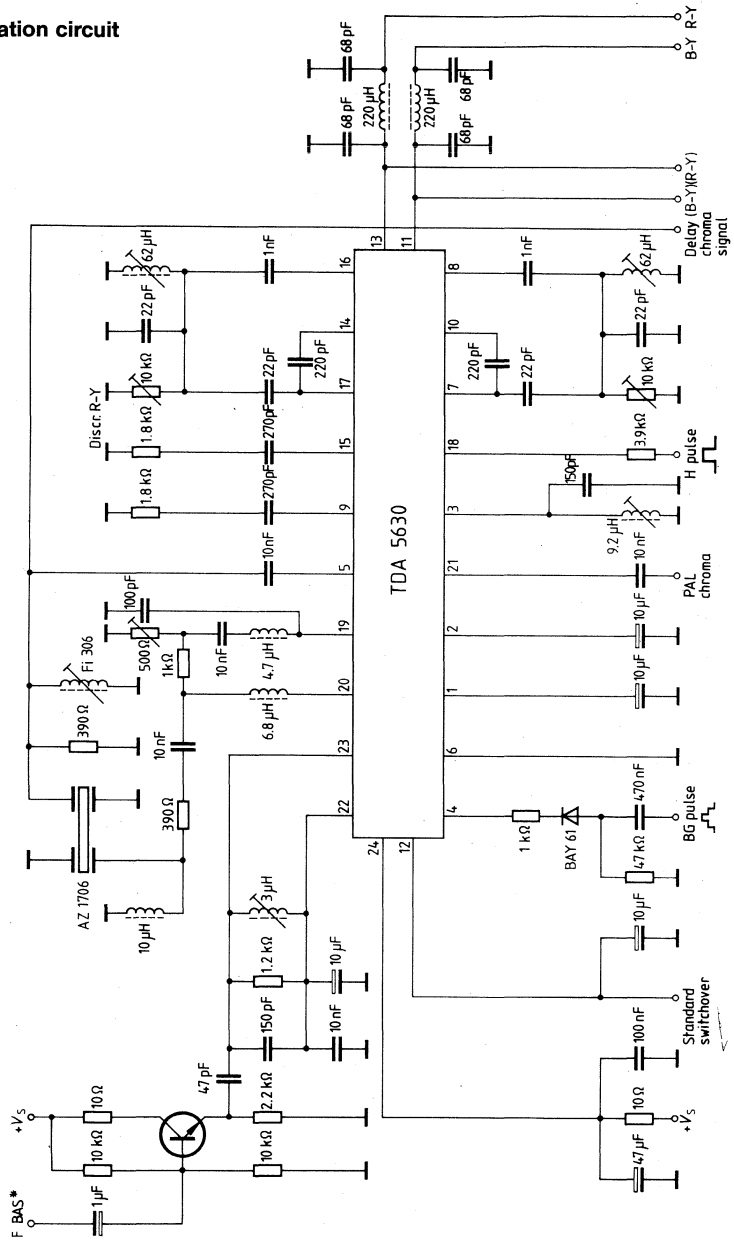


*) Composed video signal input

Test circuit 1



Application circuit



*) Composed video signal input

Preliminary data **Bipolar circuit**

Type	Ordering code	Package outline
TDA 5800	Q67000-A1777	DIP 22

The TDA 5800 contains a 4 stage broadband amplifier with controllable gain, a limiter, a synchronous demodulator for AM, an FM-demodulator for generating the AFC voltage, and an AGC generator for the IF amplifier and tuner.

An external PNP transistor is required for a VCR connection according to the IEC standard.

Features

- Suitable for standard VCR connection
- Switchable AFC
- Fast regulation
- Positive and negative video output

Maximum ratings

Supply voltage	V_S	16.5	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	70	K/W

Operating range

Supply voltage range	V_S	10 to 15.8	V
IF frequency range	f_{IF}	0.1 to 60	MHz
Ambient temperature range	T_{amb}	0 to 70	°C

■ Not for new design

Characteristics ($V_S = 13$ V; $T_{amb} = 25$ °C)

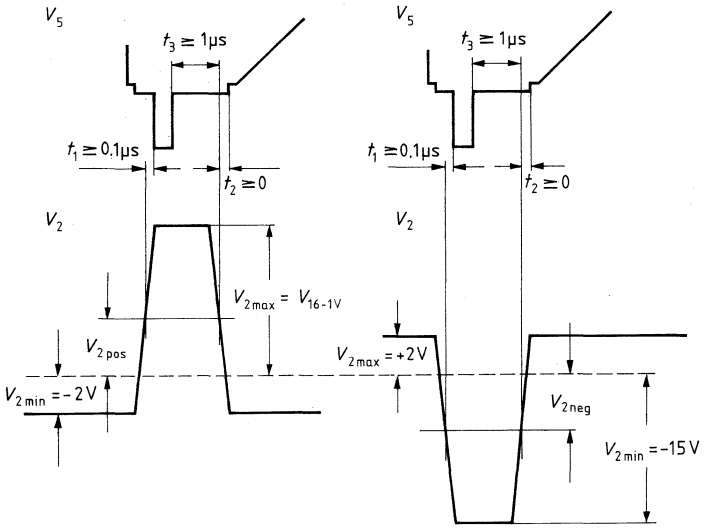
		min	typ	max	
Current consumption	I_{16}		60		mA
Stab. reference voltage	$V_{14/1}$		6.0		Vdc
Tuner control current	I_{17}	3.0	4.0		mA
Tuner AGC threshold	$V_{18/1}$	0		5.0	Vdc
Gating pulse voltage	$V_{2\,pos}$	−2.0	3.0	$V_{16}-1$	V
	$V_{2\,neg}$	−15.0	−3.0	2.0	V
Input voltage at G_{max} ($V_{5\,pp} = 3$ V)	$V_{22/21}$			100	μV
AGC range	ΔG		60		dB
IF control voltage for G_{max}	$V_{3/1}$	0			Vdc
IF control voltage for G_{min}	$V_{3/1}$			5.0	Vdc
IF control voltage for VCR switchover	$V_{3/1}$	8.0		V_{16}	Vdc
AFC output current	I_9		±1.0		mA
AFC switch off OUT ($V_{11} = V_{12}$; $R = 10$ kΩ)	$V_{11/1}$	0		4.0	Vdc
AFC switch off ON ($V_{11} = R_{12}$; $R = \infty$)	$V_{11/1}$		5.3		Vdc
AFC characteristics ($di/df > 0$)	$V_{15/1}$	3.0		V_{16}	Vdc
AFC characteristics ($di/df < 0$)	$V_{15/1}$	0		1.0	Vdc
Video output voltage pos. ($R_L = \infty$)	$V_{q\,5}$		3.0		Vdc
Sync pulse level	$V_{5/1}$		2.0		Vdc
DC voltage ($V_3 = 5$ V; $V_{22/21} = 0$)	$V_{5/1}$		5.3		Vdc
Output current to ground across R	$I_{q\,5}$		−5.0		mA
Output current (to +)	$I_{q\,5}$		2.0		mA
Output resistance	$R_{q\,5}$		150		Ω
Video output voltage neg. ($R_L = \infty$)	$V_{q\,6\,pp}$		3.0		V
Sync pulse level	$V_{6/1\,pp}$		$V_{16}-2$		V
DC voltage ($V_3 = 5$ V; $V_{22/21} = 0$)	$V_{6/1\,pp}$		$V_{16}-5.3$		V
Output current to ground across R	$I_{q\,6}$		−5.0		mA
Output current (to +)	$I_{q\,6}$		1.0		mA
Video amplifier VCR recording ($V = V_5/V_8$; $V_{8\,pp} = 1$ V)	G		3.0		

Additional application data
(not measured)

Input impedance	$Z_{i\,22/21}$		1.8/2		kΩ/pF
Output impedance	$Z_{q\,10/13}$		6.6/2		kΩ/pF
AFC input impedance	$Z_{i\,11/12}$		20		kΩ
Output resistance	$R_{q\,6}$		150		Ω
Output resistance	$R_{q\,7}$		150		Ω
Residual IF (basic frequency)	V_5; V_6		10		mV
Video bandwidth (−3 dB) VCR recording	B_{video}		6.0		MHz
Video bandwidth (VCR recording $V_{8\,pp} = 1$ V)	B_{video}		10.0		MHz
Intermodulation ratio with reference to f_{FT} (1.07 MHz)	a		45		dB

■ Not for new design

Pulse diagram

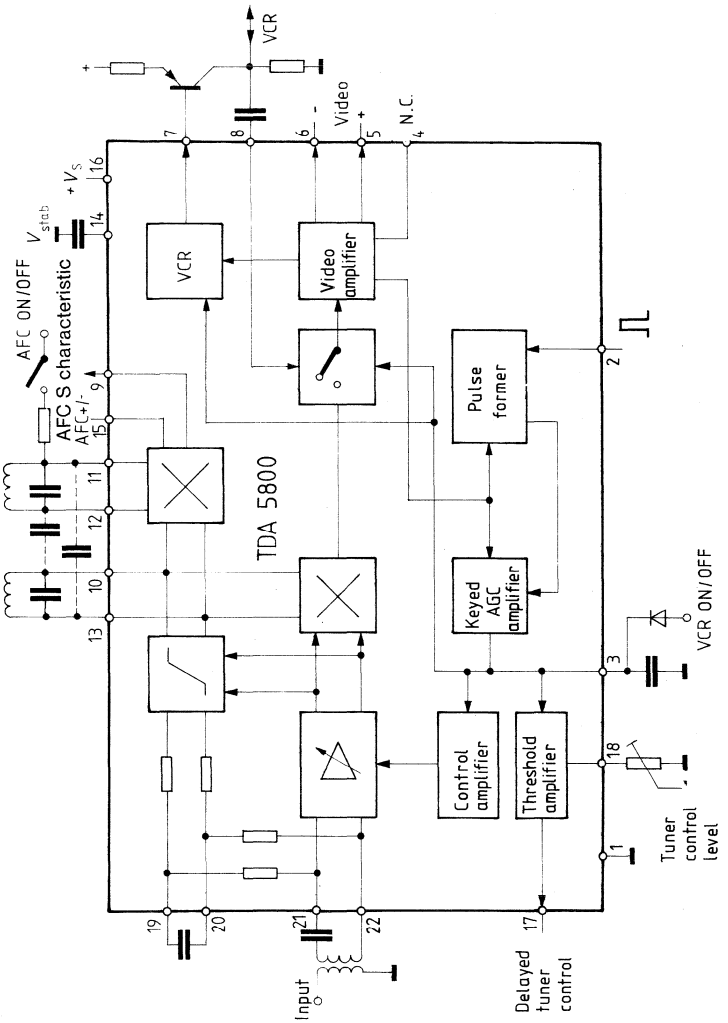


pos. gating pulse

neg. gating pulse

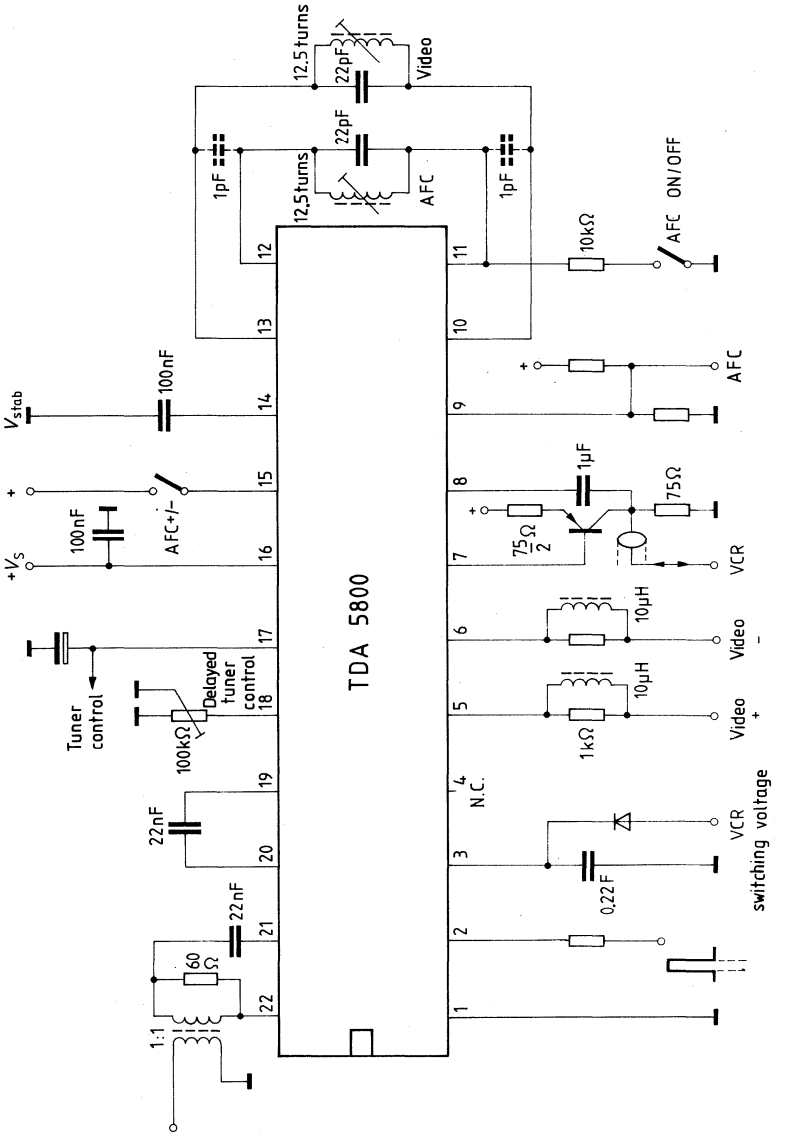
■ Not for new design

Block diagram and measurement circuit



■ Not for new design

Application circuit



■ Not for new design

Bipolar circuit

Type	Ordering code	Package outline
TDA 5820	Q67000-A1776	DIP 22

The TDA 5820 contains a 4 stage broadband amplifier with controllable gain, a limiter, a synchronous demodulator for AM, a phase-switchable FM-demodulator for generating the AFC-voltage, and an AGC generator for the IF-amplifier and tuner. The video amplifier is switchable for positive or negative modulation. Sync-pulse keyed AGC is used for negative modulation, black level keyed AGC with positive modulation.

Features

- Switchable to accomodate German and French standards
- Switchable AFC
- Fast regulation
- Positive and negative video outputs

Maximum ratings

Supply voltage	V_S	16.5	V
Junction temperature	T_j	150	°C
Storage temperature	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	70	K/W

Operating range

Supply voltage range	V_S	10 to 15.8	V
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics ($V_S = 13$ V; $T_{amb} = 25$ °C)

		min	typ	max	
Current consumption	I_{16}	38	60	90	mA
Stab. reference voltage	$V_{14/1}$	5.7	6.0	6.65	Vdc
Tuner control current ($V_{17} = 0.5\ V_{16}$)	V_{17}	3.0	4.0	6.2	mA
Tuner AGC threshold	$V_{18/1}$	0		5.0	Vdc
Gating pulse voltage (see pulse diagram)	$V_{2\,pos}$	−2.0	3.0	$V_{16}-1$	V
	$V_{2\,neg}$	−15.0	−3.0	2.0	V
Input voltage at G_{max} ($V_{5\,pp} = 3$ V)	$V_{22/21}$			100	µV
AGC range	ΔG		60		dB
IF control voltage for max. gain	$V_{3/1}$	0			Vdc
IF control voltage for min. gain	$V_{3/1}$			5.0	Vdc
IF control voltage for video switch off	$V_{3/1}$	8.0		V_{16}	Vdc
AFC output current	I_9		±1.0		mA
AFC switch off OUT ($V_{11} = V_{12}$; $R = 10$ kΩ)	$V_{11/1}$	0		4.0	Vdc
AFC switch off ON ($V_{11} = V_{12}$; $R = \infty$)	$V_{11/1}$		5.3		Vdc
AFC characteristics (di/df > 0)	$V_{15/1}$	4.0		V_{16}	Vdc
AFC characteristics (di/df < 0)	$V_{15/1}$	0		1.0	Vdc
Standard switchover neg. modul. (G-standard)	$V_{7/1}$	4.0		V_{16}	Vdc
Standard switchover pos. modul. (L-standard)	$V_{7/1}$	0		1.0	Vdc
Video output voltage pos. ($R_L = \infty$)	$V_{q\,5\,pp}$	2.3	3.0	3.5	V
Sync pulse level neg. modul.	$V_{5/1}$	1.25	2.0	2.5	Vdc
Black level for pos. modulation DC voltage ($V_3 = 5$ V)	$V_{5/1}$	2.15	2.9	3.65	Vdc
($V_{22/21} = 0$ neg. modulation) DC voltage ($V_3 = 5$ V)	$V_{5/1}$	4.0	5.3	6.6	Vdc
($V_{22/21} = 0$ pos. modulation)	$V_{5/1}$	1.5	2.0	2.8	Vdc
Output current (to ground across R)	$I_{q\,5}$		−5.0		mA
Output current (to +, $V_S = 6$ V)	$I_{q\,5}$	+0.9	2.0	+2.7	mA
Sync pulse level/max. White level (residual carrier ≦ 6% pos. modulation)	V_5		6.0	9.0	%
Video output voltage neg. ($R_L = \infty$)	$V_{q\,6\,pp}$	2.3	3.0	3.5	V
Sync pulse level neg. modulation	$V_{6/1}$	$V_{16}-3.4$	$V_{16}-2.0$	$V_{16}-0.4$	Vdc
Black level for pos. modulation DC voltage ($V_3 = 5$ V)	$V_{6/1}$	$V_{16}-4.5$	$V_{16}-2.9$	$V_{16}-1.5$	Vdc
($V_{22/21} = 0$ neg. modulation) DC voltage ($V_3 = 5$ V)	$V_{6/1}$	$V_{16}-7.2$	$V_{16}-5.3$	$V_{16}-3.4$	Vdc
($V_{22/21} = 0$ pos. modulation)	$V_{6/1}$	$V_{16}-3.6$	$V_{16}-2.0$	$V_{16}-0.6$	Vdc
Output current (to ground across R)	$I_{q\,6}$		−5.0		mA
Output current (to +, $V_6 = 12.3$ V)	$I_{q\,6}$	+0.5	1.0	+1.6	mA

Additional application data[1])

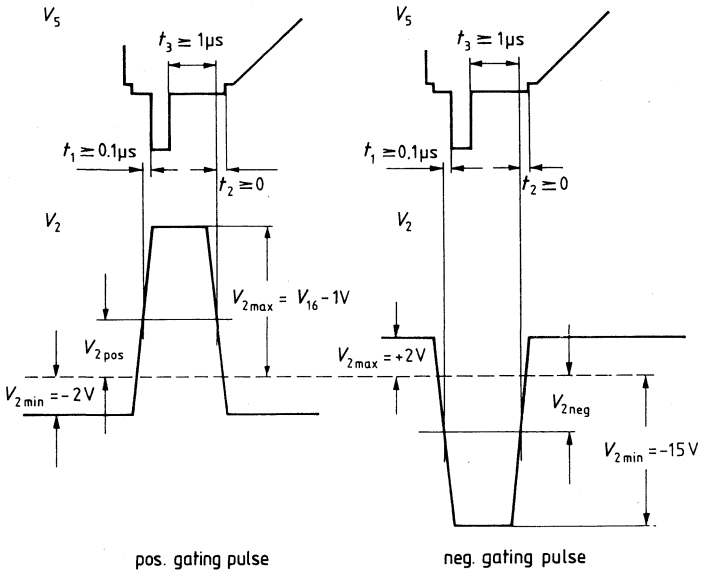
		min	typ	max	
Input impedance	$Z_{22/21}$		1.8/2		kΩ/pF
Output impedance	$Z_{10/13}$		6.6/2		kΩ/pF
AFC input impedance	$Z_{11/12}$		20		kΩ
Output resistance	R_{q5}		150		Ω
Output resistance	R_{q6}		150		Ω
IF frequency range	f_{IF}	0.1		60	MHz
Residual IF (basic frequency)	V_5; V_6		10		mV
Video bandwidth (−3 dB)	B_{video}		6.0		MHz
Intermodulation ratio referred to f_{FT} (1.07 MHz)	a		45		dB

Pin configuration

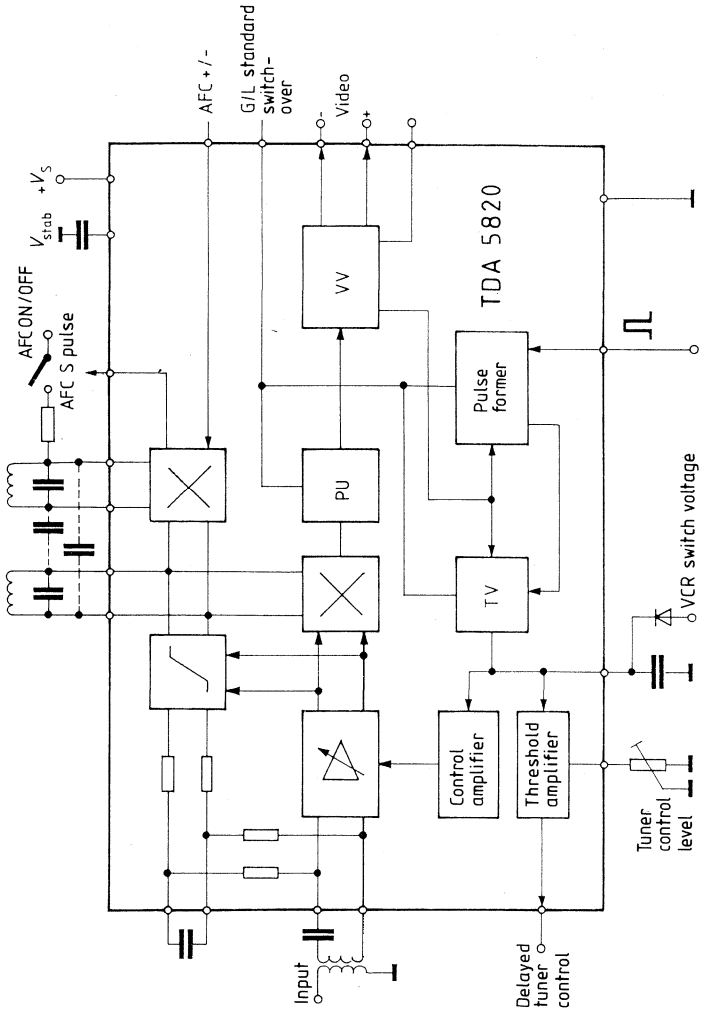
Pin No.	Function
1	Ground
2	Gating pulse
3	Time constant for control voltage/ programming VCR recording playback
4	White level adjustment
5	Video output, positive
6	Video output, negative
7	G/L standard switchover
8	Ground
9	AFC output
10	Tank circuit
11	AFC tank circuit
12	AFC tank circuit
13	Tank circuit
14	Stab. reference voltage
15	Programmable AFC polarity
16	Supply voltage +
17	Delayed tuner control
18	Tuner AGC threshold
19	Operating point adjustment
20	Operating point adjustment
21	Video IF input
22	Video IF input

1) not measured

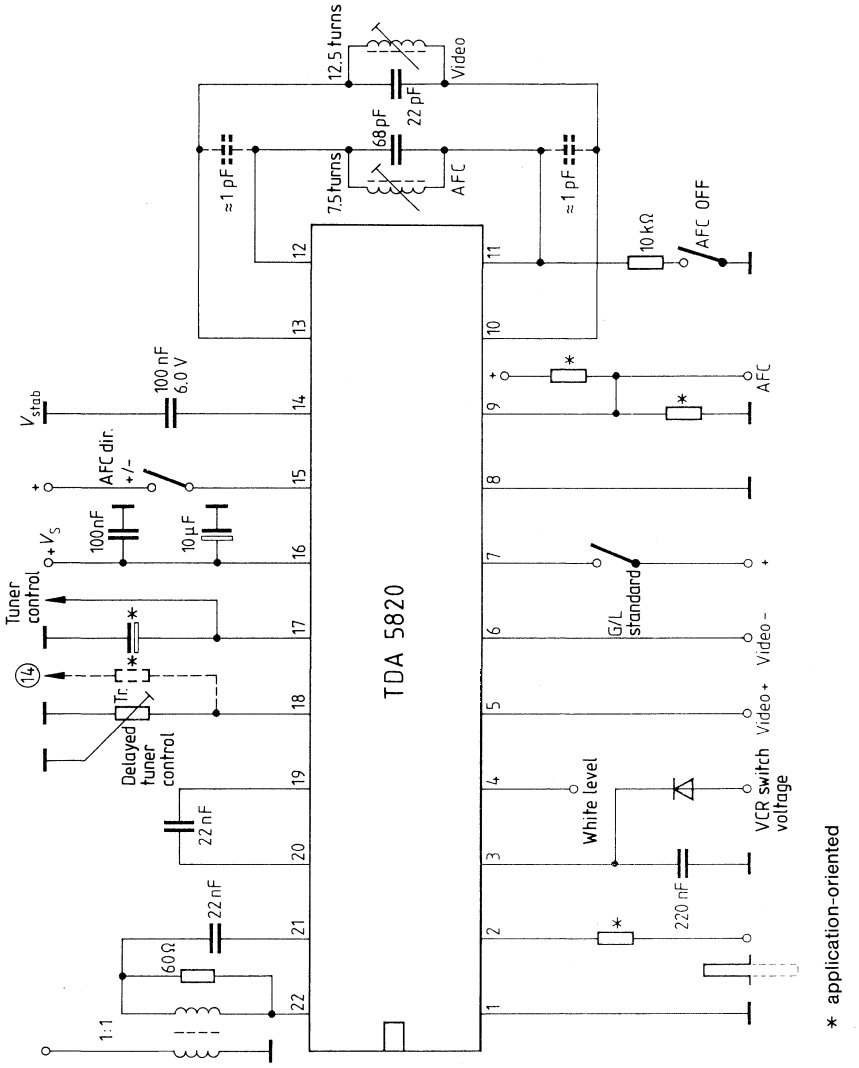
Pulse diagram



Block diagram and measurement circuit



Application circuit



Bipolar circuit

Type	Ordering code	Package outline
TDA 5850	Q67000-A1775	DIP 8

The TDA 5850 is a switchable video amplifier with connections for the French and IEC VCR standards.

Features

- Standard connection for VCR (CCIR) and Peri TV sets
- Input clamping
- Positive and negative video outputs

Maximum ratings

Supply voltage	V_S	16.5	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	70	K/W

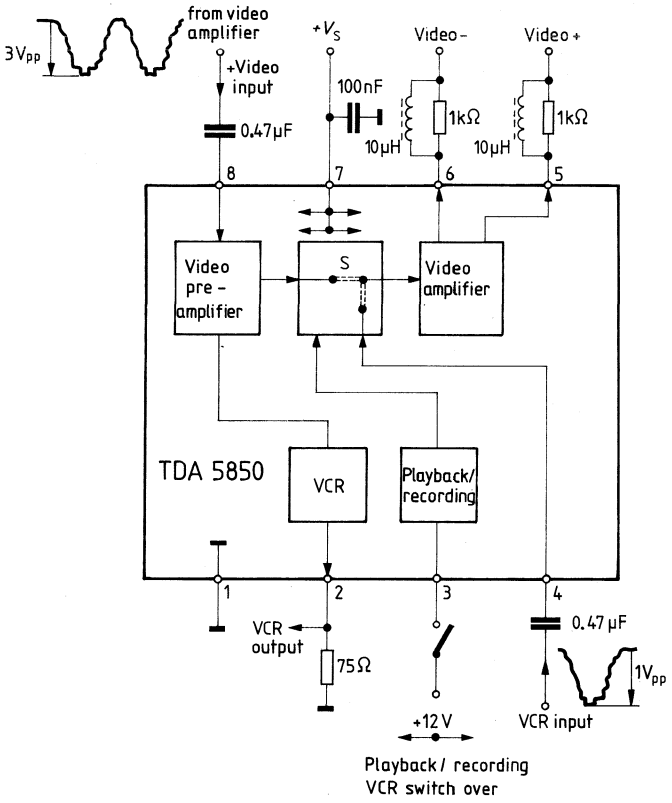
Operating range

Supply voltage range	V_S	10 to 15.8	V
Video bandwidth	B_{video}	6	MHz
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics ($V_S = 13$ V; $T_{amb} = 25$ °C)

		min	typ	max	
Current consumption (pin 2 open)	I_7		23.0		mA
Switch input VCR recording	$V_{3/1}$	0		1.2	Vdc
Switch input VCR playback	$V_{3/1}$	3.0		V_7	Vdc
Switch input $V_{3/1} = 15$ V	I_3			1.0	mA
Video output voltage pos. ($V_3 = 1.2$ V; $V_{8\,pp} = 3$ V)	$V_{5\,pp}$		3.0		V
Video output voltage pos. ($V_3 \geq 3$ V; $V_4 = 1$ V_{pp})	$V_{5\,pp}$		3.0		V
Sync pulse level	$V_{5/1}$		2.0		Vdc
Output current (to ground)	I_5		−5.0		mA
Output current (to +)	I_5		2.0		mA
Output resistance	R_5		150		Ω
Video output voltage neg. ($V_3 = 1.2$ V; $V_8 = 3$ V_{pp})	$V_{6\,pp}$		3.0		V
Video output voltage neg. ($V_3 \geq 3$ V; $V_4 = 1$ V_{pp})	$V_{6\,pp}$		3.0		V
Sync pulse level	$V_{6/1}$		$V_7 - 2$		Vdc
Output current (to ground)	I_6		−5.0		mA
Output current (to +)	I_6		1.0		mA
Output resistance	R_6		150		Ω
Video output voltage pos. ($V_{8\,pp} = 3$ V; $R_{2/1} = 75$ Ω)	$V_{2\,pp}$		1.0		V
Sync pulse level ($R_{2/1} = 75$ Ω)	$V_{2/1}$		1.0		Vdc
Output current (to ground)	I_2		−30.0		mA
Output current (to +)	I_2		2.0		mA
Output resistance	R_2		75		Ω
Video input current ($V_{8\,pp} = 3$ V)	I_8			40	µA
Video input current ($V_{4\,pp} = 1$ V)	I_4			20	µA
Video gain ($V_{8\,pp} = 3$ V; $R_{2/1} = 75$ Ω)	$G_{2/8}$		1/3		
Video gain ($V_{8\,pp} = 3$ V; $V_3 = 1.2$ V)	$G_{5/8}$		1		
Video gain ($V_{8\,pp} = 3$ V; $V_3 = 1.2$ V)	$G_{6/8}$		−1		
Video gain ($V_{4\,pp} = 1$ V; $V_3 \geq 3$ V)	$G_{5/4}$		3		
Video gain ($V_{4\,pp} = 1$ V; $V_3 \geq 3$ V)	$G_{6/4}$		−3		
Video bandwidth (−3 dB)	B_{video}	6.0			MHz
Cross talk rejection referred to $V_{5\,pp} = 3$ V ($f = 50$ Hz . . 6.0 MHz; $V_3 = 1.2$ V; $V_{4\,pp} = 1$ V)	a		50		dB

Block diagram, test circuit and application circuit



Video IF IC with Synchronous Demodulator

TDA 6000
TDA 6010

Preliminary data

Bipolar circuit

Type	Ordering code	Package outline
TDA 6000	Q67000-A2203	DIP 16
TDA 6010	Q67000-A2227	

The controlled AM broadband amplifier includes a PLL synchronous demodulator, a video amplifier as well as a control voltage generation for the IF amplifier and tuner.

TDA 6000: for PNP tuner
TDA 6010: for NPN tuner

Features

- Ideal synchronous demodulation
- Large control range
- High input sensitivity
- Very low luma-chroma crosstalk
- Positive and negative video signal
- Extremely low differential phase and gain errors
- Ideal chroma processing

Maximum ratings

Supply voltage	V_S	16.5	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	70	K/W

Operating range

Supply voltage range	V_S	10.5 to 15.8	V
IF frequency	f_{IF}	60	MHz
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics ($V_S = 13$ V; $T_{amb} = 25$ °C)

		min	typ	max	
Current consumption	I_{11}		70		mA
Stab. reference voltage	V_{12}		6.0		Vdc
Control current for tuner ($V_{14} = 0.5\ V_{11}$)	I_{14}		4.0		mA
Tuner AGC threshold	$V_{13/1}$	0		4.0	Vdc
Gating pulse voltage					
pos. gating pulse	V_1		+3.0		V
neg. gating pulse	V_1		−3.0		V
Input voltage at G_{max} ($V_{3\,pp} = 3$ V)	$V_{i15/16}$			100	µV
AGC range	V		60		dB
Video output voltage (pos.) ($R_L = \infty$)	$V_{q\,3\,pp}$		3.0		V
Sync pulse level	$V_{q\,3}$		2.0		Vdc
DC voltage ($V_2 = 4$ V; $V_{15/16} = 0$)	$V_{3/1}$		5.3		Vdc
Output current					
to ground across R	$I_{q\,3}$		−5.0		mA
to plus $V_3 = 7$ V	$I_{q\,3}$		+2.0		mA
Video output voltage (neg.) ($R_L = \infty$)	$V_{q\,4\,pp}$		3.0		V
Sync pulse level	$V_{4/10}$		V_{11}−2.0		Vdc
DC voltage ($V_2 = 4$ V; $V_{15/16} = 0$ V)	$V_{4/10}$		V_{11}−5.3		Vdc
Output current					
to ground across R	$I_{q\,4}$		−5.0		mA
to plus $V_4 = V_{11}$	$I_{q\,4}$		+1.0		mA
IF control voltage G_{max}	$V_{2/10}$	0			Vdc
G_{min}	$V_{2/10}$			4.0	Vdc

Additional application data

Input impedance	$Z_{i15/16}$		1.8/2		kΩ/pF
Output impedance	$Z_{q\,8/9}$		6.6/2		kΩ/pF
Output resistance	$R_{q\,3}$		150		Ω
Output resistance	$R_{q\,4}$		150		Ω
Residual IF (basic frequency)	$V_3; V_4$		10		mV
Video bandwidth (−3 dB)	B_{video}		6.0		MHz
Intermodulation ratio with reference to f_{FT} (1.07 MHz)	a		45		dB

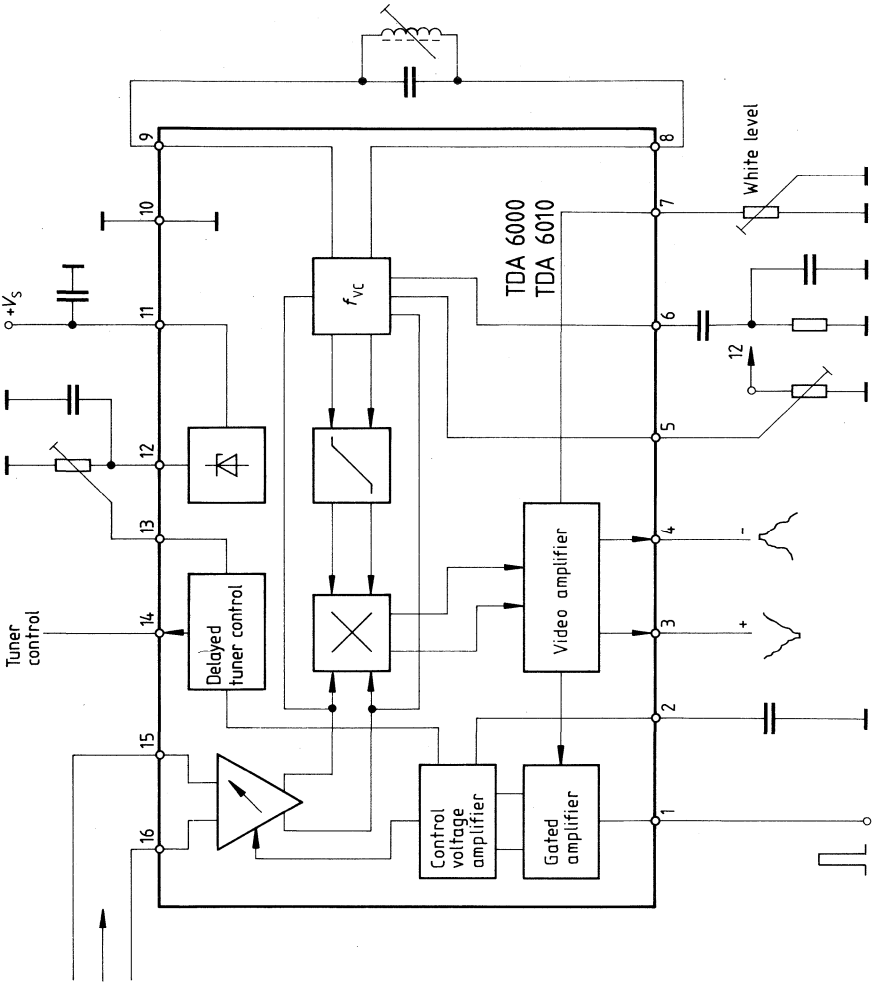
Circuit description

This integrated circuit consists of a 4-stage controlled gain AM amplifier and a PLL circuit for video carrier regeneration. The synchronous demodulator features very low intermodulation distortion between video IF and color carrier (1.1 MHz or 920 kHz beat). Also included are a mixer for the synchronous demodulation of the video signals and an amplifier for the positive and negative video output signal. The positive signal is used for gate control of the AGC amplifier. The delayed tuner AGC is derived from the control voltage via a threshold amplifier.

Pin configuration

Pin No.	Function
1	Gating pulse
2	Time constant AGC
3	Positive video output
4	Negative video output
5	Offset adjustment
6	PLL time constant
7	White level adjustment
8	Tank circuit
9	Tank circuit
10	Ground
11	Supply voltage
12	Reference voltage
13	AGC threshold
14	Tuner control
15	Video IF input
16	Video IF input

Block diagram



Preliminary data **Bipolar circuit**

Type	Ordering code	Package outline
TUA 2000	Q67000-A1764-C702	DIP 16

The TUA 2000 is a monlithic integrated circuit and suitable as a tuner for the VHF range up to 400 MHz, e.g. for TV tuners.

RF section

- Few external components
- Stable oscillator frequency and amplitude with very low interference radiation
- Optimal rejection of oscillator and input frequencies at the IF output due to a decoupled active ring mixer circuit
- High interference voltage resistance
- High-impedance mixer input, for symmetrical and unsymmetrical connections
- IF post-amplifier

IF section

- Optimal crosstalk rejection
- Large signal-modulation range
- Low noise figure with wide minimum over large load-impedance range

Maximum ratings

Supply voltage range ($V_3 \leqq V_S$)	V_S	−0.3 to 16.5	V
Reference voltage ($V_S \geqq V_3$)	V_3	−0.3 to 7.9	V
Voltage at pin 1, 2 ($V_3 \leqq V_{1,2}$)	$V_{1,2}$	−0.3 to 16.5	V
Voltage at pin 8,9 ($V_3 \leqq V_{8,9}$)	$V_{8,9}$	−0.3 to 16.5	V
Voltage at pin 14	V_{14}	−0.3 to 16.5	V
AC voltage at pin 4, 5, 6, 11, 12, 13, 15	V_{rms}	0 to 0.5	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	80	K/W

Only the specified external circuitry may be applied to pins 4, 5, 6, 11, 12, 13, 15

Operating range

Supply voltage range	V_S	9 to 15	V
Reference voltage range	V_3	7.2 to 7.8	V
Input frequency range – mixer section	$f_{M\,12/13}$	10 to 400	MHz
Input frequency range of the UHF – IF amplifier frequency range	$f_{UHF\,11}$	10 to 400	MHz
Input frequency range of the SAW amplifier	$f_{IF\,15}$	10 to 400	MHz
Oscillator amplifier range depending on the oscillator circuitry at pin 4, 5	$f_{OSC\,4,5}$	10 to 400	MHz
Voltage at pin 1, 2, 8, 9	$V_{1,2,8,9}$	9 to 15	V
Output frequency range of the mixer/UHF	$f_{IF\,M/UHF\,8/9}$	10 to 400	MHz
Output frequency range of the SAW amplifier	$f_{IF\,1,2}$	10 to 400	MHz
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics ($V_S = 12V^*$); $V_3 = 7.5$ V; $T_{amb} = 25$ °C)

		min	typ	max	
Total current consumption $I_{14} = 0$; $V_3 = 7.2$ V; $V_S = 9$-15 V	$I_{10,1,2,8,9,3}$	35			mA
$I_{14} = 0$; $V_3 = 7.8$ V; $V_S = 9$-15 V		42		72	mA
Current consumption at pin 3 $I_{14} = 0$; $V_3 = 7.2$-7.8 V	I_3	17		31	mA
Output characteristic $V_{8,9} = 9$-15 V; $V_3 = 7{,}8$ V	$\Delta I_{8,9}$			100	µA
Output characteristic $V_{1,2} = 9$-15 V; $V_3 = 7.8$ V	$\Delta I_{1,2}$			200	µA
UHF switching voltage $V_{I(u)} = -25$ dBm $V_0 \geqq -5$ dBm; $f_{IF} = 38.9$ MHz	$V_{14\,UHF}$	7		16	V
VHF switching voltage $V_{I(u)}{}^*) = -25$ dBm $V_0 \leqq -30$ dBm; $f_{IF} = 38.9$ MHz	$V_{14\,VHF}$	0		3	V
Mixer gain Bd I; $V_{I(RF)} = -40$ dBm; $f_{RF} = 60$ MHz; $f_{IF} = 36.15$ MHz; $R_{G\,12/13} = 100\ \Omega$; refer to response characteristic	G_{60}	23	27	31	dB
Mixer gain Bd III; $V_{I(RF)}{}^*) = -40$ dBm; $f_{IF} = 36.15$ MHz; $R_{G\,12/13} = 100\ \Omega$; refer to response characteristic	G_{220}	23	27	31	dB
Mixer noise Bd I, white noise $R_{G\,12/13} = 100\ \Omega$; refer to response characteristic	NF_{60}			13	dB
Mixer noise Bd III; white noise $R_{G\,12/13} = 100\ \Omega$; refer to response characteristic	NF_{220}			14	dB
Gain UHF input $V_{I(u)}{}^*) = -40$ dBm; $V_{14} = 12$ V; $f_{RFU} = f_{IF} = 36.15$ MHz; $R_{G\,11} = 200\ \Omega$; refer to response characteristic	G_{UHF}	36	38	40	dB

*) $V_{I(u)}$, $V_{I(RF)}$ } Input voltage if the generator is terminated with a load resistor of 50 Ω

Characteristics ($V_S = 12\,V^*$); $V_3 = 7.5$ V; $T_{amb} = 25$ °C)

		min	typ	max	
Noise figure UHF input $V_{14} = 12$ V; white noise $R_{G11} = 200\ \Omega$; refer to response characteristic	NF_{UHF}			7	dB
Oscillator turn-on drift $V_{tun} = 28$ V; $t = 0 - 500$ ms; Bd II; $f_{OSC} = 216$ MHz	f_{OSC}	−10		−250	kHz
Oscillator turn-on drift $V_{tun} = 28$ V; $t = 0 - 10$ s; Bd II; $f_{OSC} = 216$ MHz	f_{OSC}	−10		−450	kHz
Additional application data					
Differential input resistance[1])	$R_{12/13}$		3		kΩ
Differential input capacitance[1])	$C_{12/13}$		2.7		pF
IF input resistance[1])	R_{15}		2		kΩ
IF input capacitance[1])	C_{15}		3.9		pF
UHF input resistance[1])	R_{11}		2.2		kΩ
UHF input capacitance[1])	C_{11}		3.4		pF
Interference voltage resistance Bd I $m_N = 1\%$; $m_{int} = 80\%$; $\Delta f_{int} = 10$ MHz; $f_{mod} = 1$ kHz; $f_N = 65$ MHz	$V_{int\,12/13\,rms}$		140		mV
Interference voltage resistance Bd II $m_N = 1\%$; $m_{int} = 80\%$; $\Delta f_{int} = 10$ MHz; $f_{mod} = 1$ kHz; $f_N = 220$ MHz	$V_{int\,12/13\,rms}$		100		mV

1) Measured S parameter values converted to Y parameter

*) Unless otherwise specified under test conditions

Circuit description

The TUA 2000 contains a symmetrical mixer input, as well as a multiplicative mixer. The oscillator amplitude is regulated. All oscillator operating currents and voltages are stabilized, so that the oscillator's amplitude and frequency are largely independent of temperature and operating voltage changes.

The IF amplifier has been provided with a high impedance input.

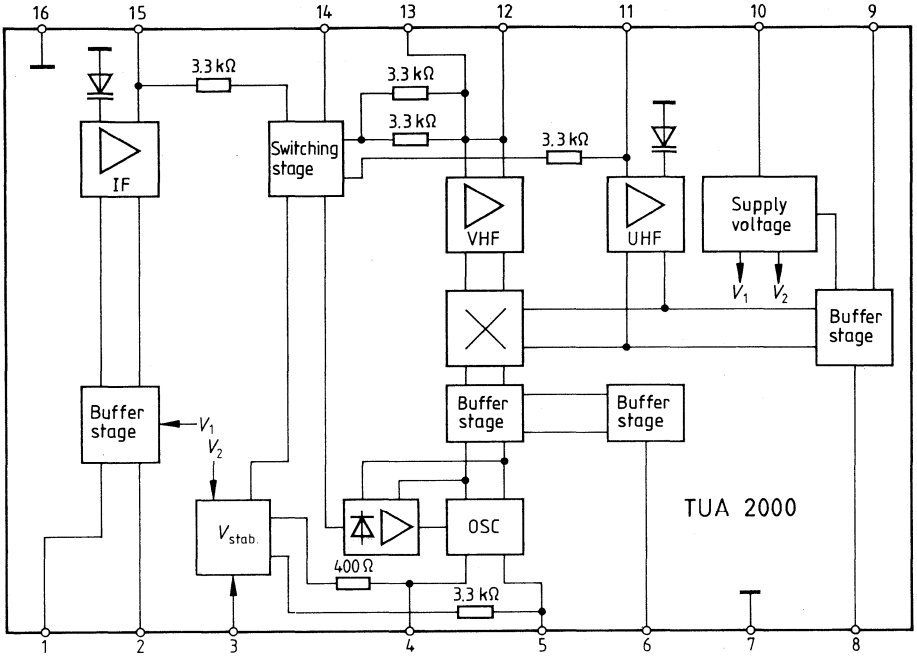
The output has two open collector connections.

During UHF operation, oscillator and mixer are switched off and the UHF IF input coupling stage is activated.

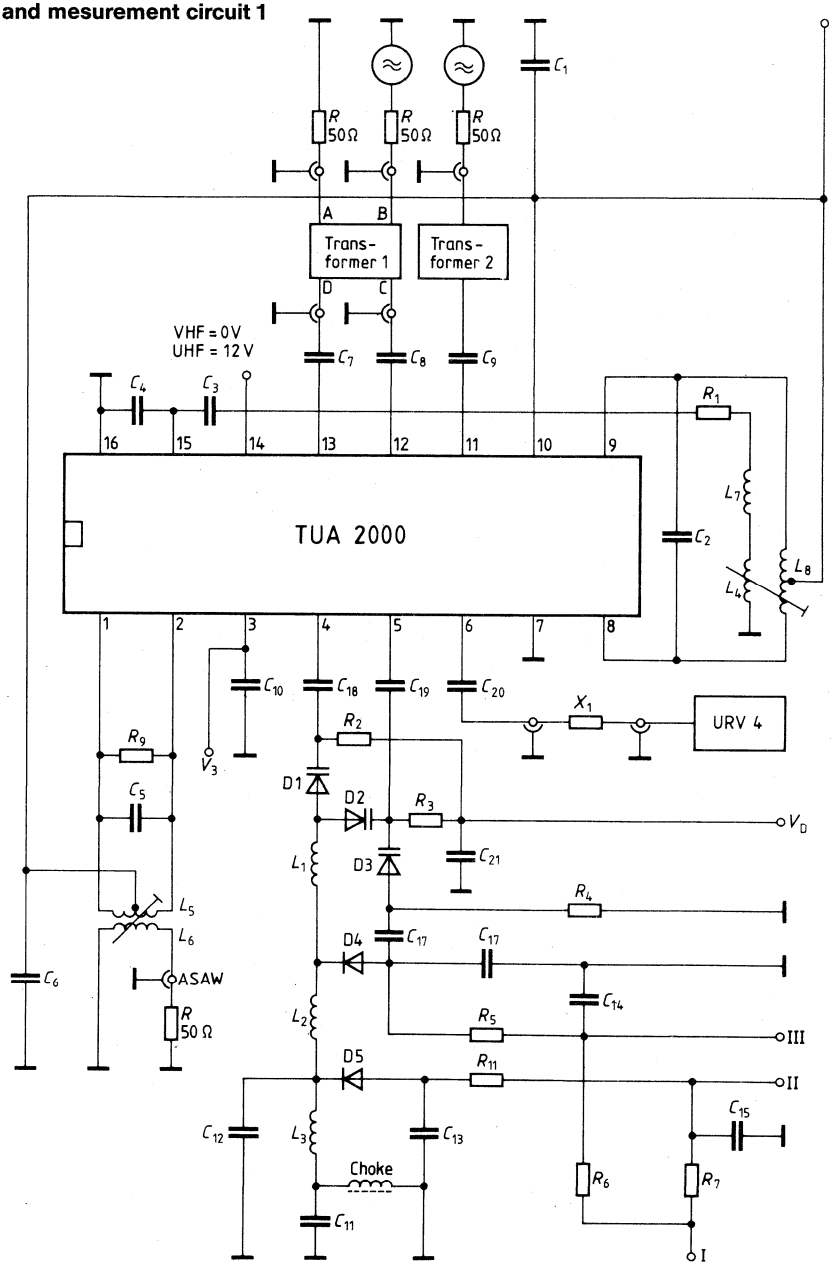
Pin configuration

Pin No.	Function
1	"Open collector" output of the IF SAW driver
2	"Open collector" output of the IF SAW driver
3	Input for external reference voltage
4	Low-ohmic collector output, coupling point to the high reference point
5	High-ohmic base input of a parallel resonant circuit
6	Oscillator signal output for counter connection
7	Ground
8	"Open collector" output of the mixer
9	"Open collector" output of the mixer
10	Supply voltage
11	Asymmetrical IF signal input for the UHF-IF signal
12	Mixer high impedance differential input
13	Mixer high impedance differential input
14	Switching voltage input for the VHF-UHF switch-selection
15	Asymmetrical signal input of the IF SAW amplifier
16	Ground

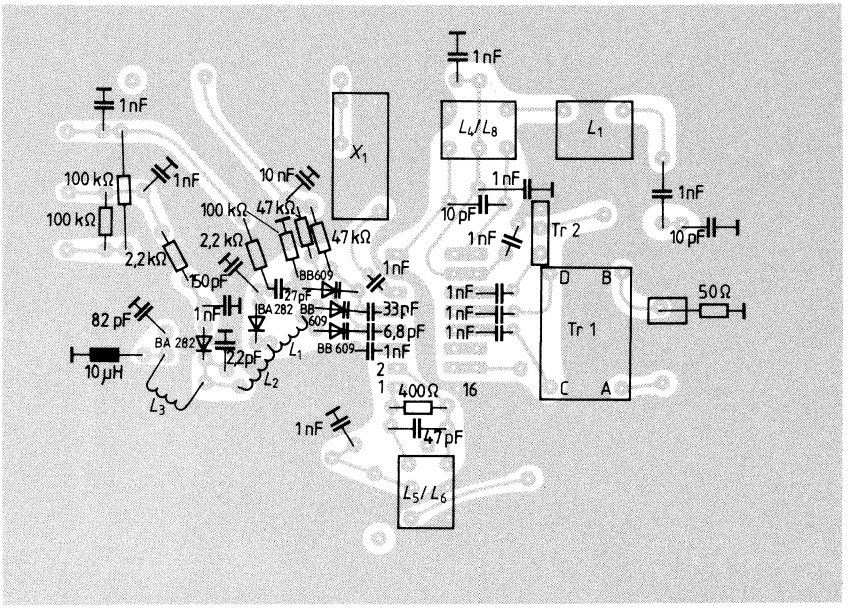
Block diagram



Test and mesurement circuit 1



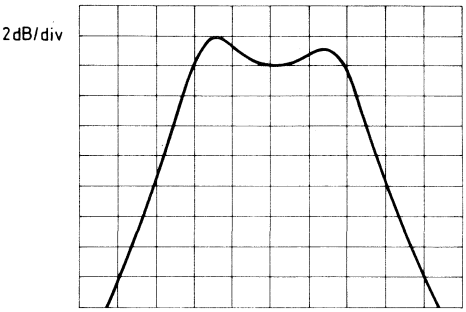
Plug-in location plan



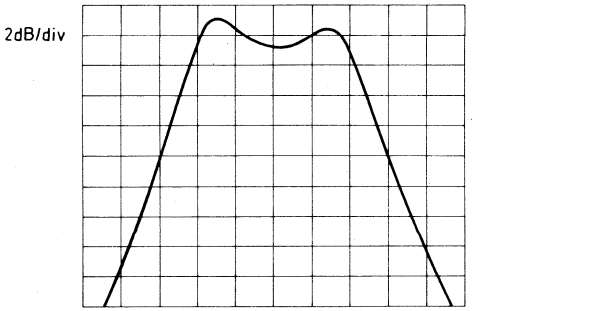
PCB layout of test and measurement circuit 1

Notes on test and measurement circuit 1

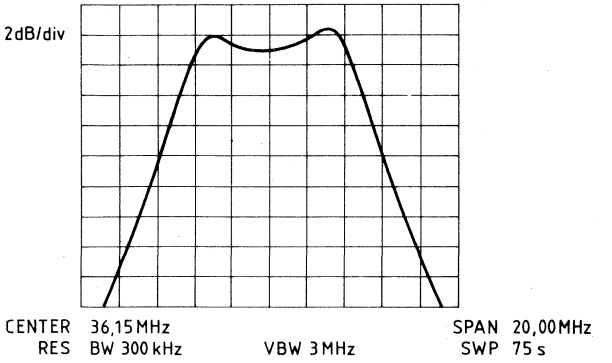
Response of passband curve for operation in VHF band I
$f_{RF} = 60$ MHz ± 10 MHz; $V_{14} = 0$ V; $V_{I(RF)} = -40$ dBm; ref. level $= -10$ dBm
gain test point $f_{RF} = 60$ MHz; $f_{IF} = 36.15$ MHz



Response of passband curve for operation in VHF band III
$f_{RF} = 220$ MHz ± 10 MHz; $V_{14} = 0$ V; $V_{I(RF)} = -40$ dBm; ref. level $= -10$ dBm
gain test point $f_{RF} = 220$ MHz; $f_{IF} = 36.15$ MHz



Response of passband curve for operation in VHF IF position
$f_{RFU} = 36.15$ MHz ± 10 MHz; $V_{14} = 12$ V; $V_{I(RF)} = -40$ dBm; ref. level = 0 dBm
gain test point $f_{RFU} = f_{IF} = 36.15$ MHz



Explanations to diagrams

2 dB/div	= 2 dB/division on Y axis
Center 36.15 MHz	= center frequency of display at IF = 36.15 MHz
RES BW 300 kHz	= resolution bandwidth of spectrum analyzer is 300 kHz in its IF section
VBW 3 MHz	= video bandwidth in IF section of spectrum analyzer is 3 MHz
SPAN 20.00 MHz	= overall display range of diagram is 20 MHz, i.e. 2 MHz/division on X axis
SWP 75 sec	= sweep time on X axis is 75 s
Ref. level	= reference level is uppermost horizontal line of diagram

Notes on test and measurement circuit 1

On path pin 4 – C18 – D1 – D2 – C19 – pin 5 ensure minimal lead inductance for the suppression of parasitic series resonance outside of the oscillator's useful band.

Transformer Tr 1:

Tr 1 = ANZ ac = HH-109 30 to 500 MHz
C = 0°; R_{gC} = 50 Ω
D = 180°; R_{gD} = 50 Ω

Transformer Tr 2:

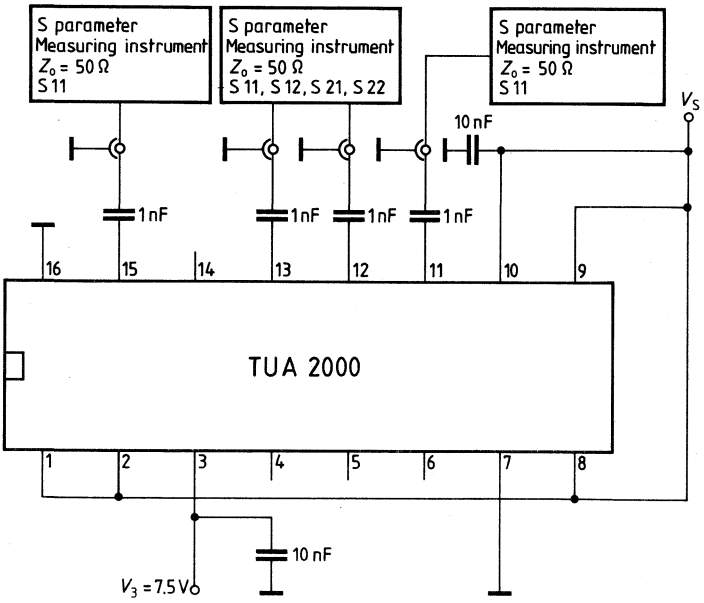
50/200 Ω unbalanced
3 turns bifilar on core material
B62152-A7-X1

Attenuator: X1 = 6 dB

Bd I 58 to 85 MHz
Bd II 110 to 216 MHz
Bd III 200 to 400 MHz

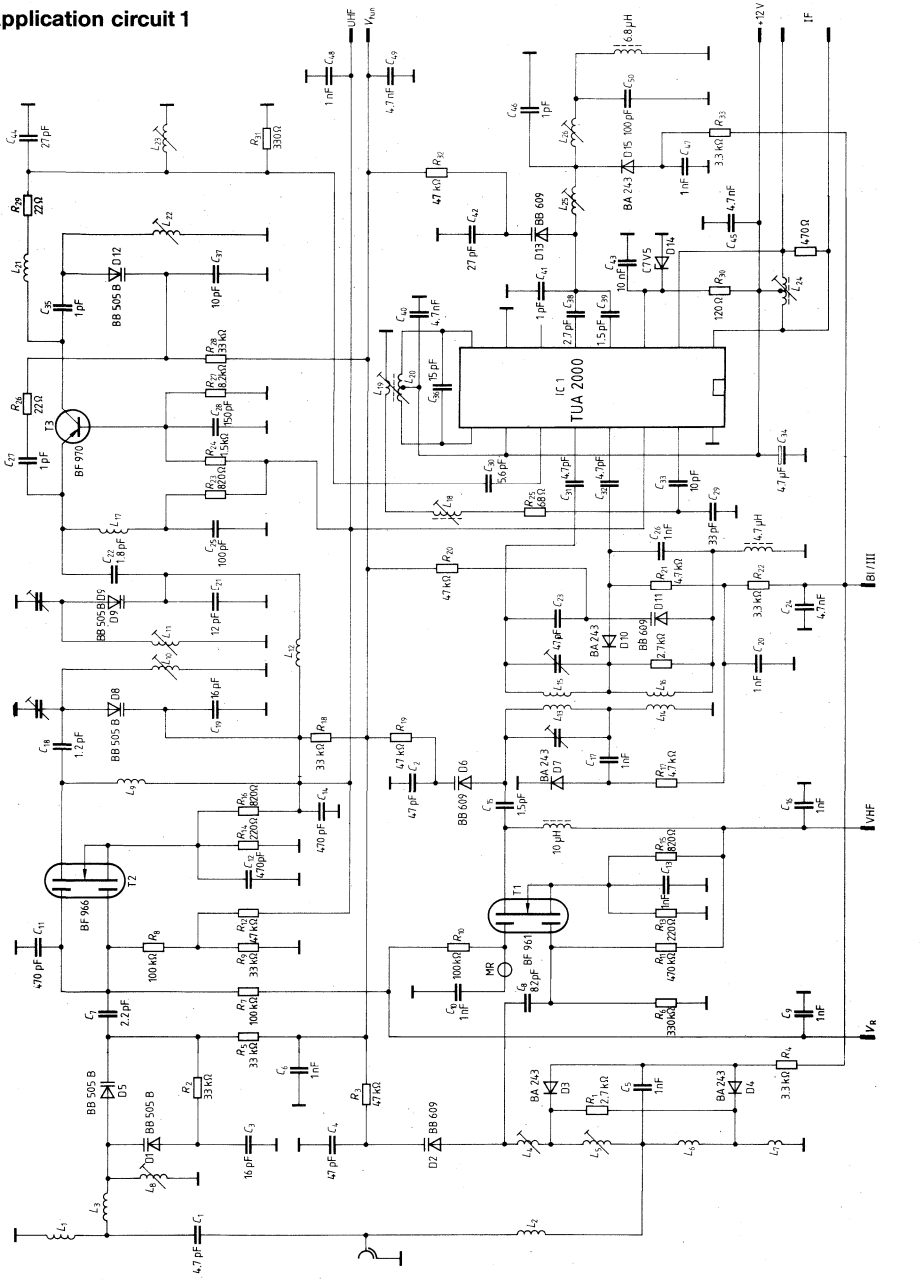
	I	II	III
Band I	−12 V	X	X
Band II	−12 V	+12 V	X
Band III	−12 V	+12 V	+12 V

Test and mesurement circuit 2

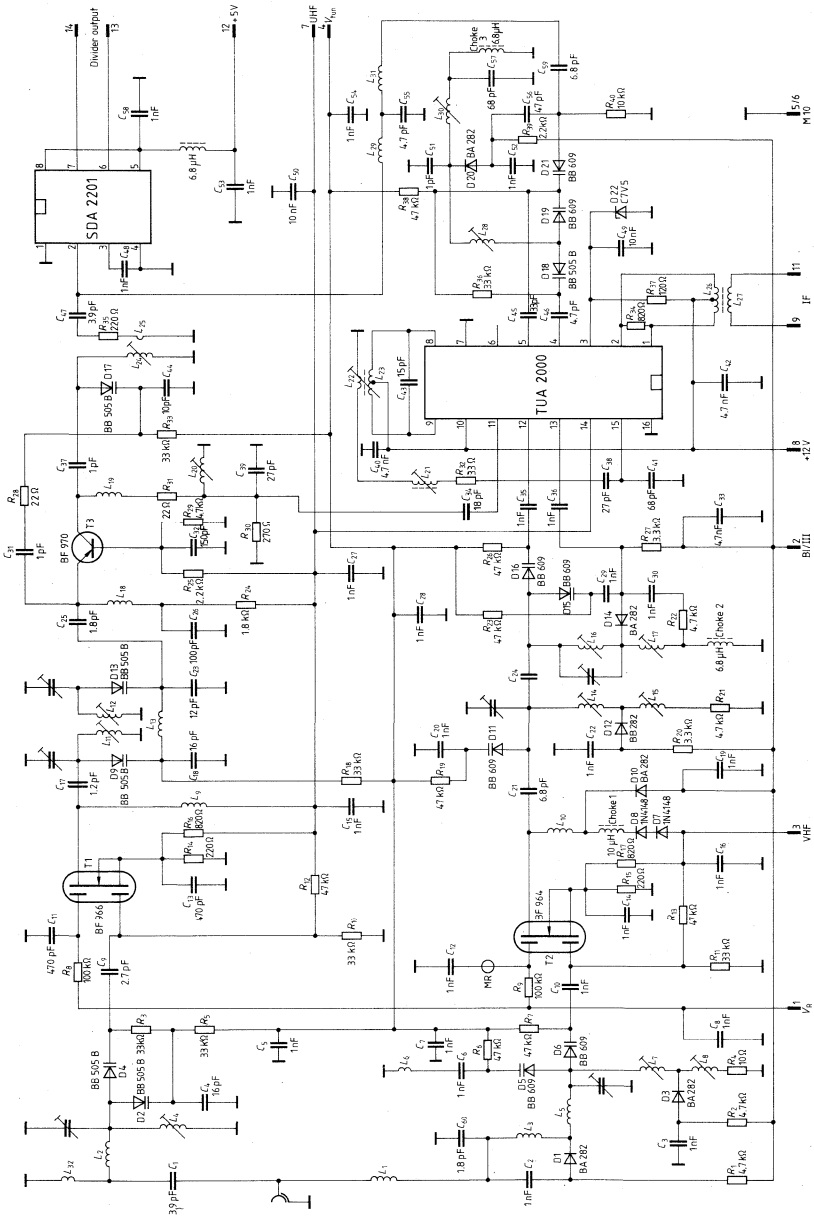


For the determination of the input admittance values of pins 11, 12, 13, 15

Application circuit 1



Application circuit 2



Preliminary data **Bipolar circuit**

Type	Ordering code	Package outline
TUA 2000-2	Q67000-A1764-C705	DIP 16

The TUA 2000-2 is a monlithic integrated circuit and suitable as a tuner for the VHF range up to 400 MHz, e.g. for TV tuners.

RF section

- Few external components
- Stable oscillator frequency and amplitude with very low interference radiation
- Optimal rejection of oscillator and input frequencies at the IF output due to a decoupled active ring mixer circuit
- High interference voltage resistance
- High-impedance mixer input, for symmetrical and asymmetrical connections
- IF post-amplifier for the UHF IF signal

IF section

- Optimal crosstalk suppression
- Large signal-modulation range
- Low noise figure with wide minimum over large load-impedance range

Maximum ratings

Supply voltage range ($V_3 \leqq V_S$)	V_S	−0.3 to 16.5	V
Reference voltage ($V_S \geqq V_3$)	V_3	−0.3 to 7.9	V
Voltage at pin 1, 2 ($V_3 \leqq V_{1,2}$)	$V_{1,2}$	−0.3 to 16.5	V
Voltage at pin 8,9 ($V_3 \leqq V_{8,9}$)	$V_{8,9}$	−0.3 to 16.5	V
Voltage at pin 14	V_{14}	−0.3 to 16.5	V
AC voltage at pin 4, 5, 6, 11, 12, 13, 15	V_{rms}	0 to 0.5	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	80	K/W

Only the sepcified external circuitry may be applied to pins 4, 5, 6, 11, 12, 13, 15.

Operating range

Supply voltage range	V_S	9 to 15	V
Reference voltage range	V_3	7.2 to 7.8	V
Input frequency range – mixer section	$f_{M\,12/13}$	10 to 400	MHz
Input frequency range of the UHF – IF amplifier frequency range	$f_{UHF\,11}$	10 to 400	MHz
Input frequency range of the SAW amplifier	$f_{IF\,15}$	10 to 400	MHz
Oscillator amplifier range depending on the oscillator circuitry at pin 4, 5	$f_{OSC\,4,5}$	10 to 400	MHz
Voltage at pin 1, 2, 8, 9	$V_{1,2,8,9}$	9 to 15	V
Output frequency range of the mixer/UHF	$f_{IF\,M/UHF\,8/9}$	10 to 400	MHz
Output frequency range of the SAW amplifier	$f_{IF\,1,2}$	10 to 400	MHz
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics ($V_S = 12V^*$); $V_3 = 7.5$ V; $T_{amb} = 25$ °C)

		min	typ	max	
Total current consumption $I_{14} = 0$; $V_3 = 7.2$ V; $V_S = 9\text{-}15$ V	$I_{10,1,2,8,9,3}$	35			mA
$I_{14} = 0$; $V_3 = 7.8$; $V_S = 9\text{-}15$ V		42		72	mA
Current consumption at pin 3 $I_{14} = 0$; $V_3 = 7.2\text{-}7.8$ V	I_3	17		31	mA
Output characteristic $V_{8,9} = 9\text{-}15$ V; $V_3 = 7.8$ V	$\Delta I_{8,9}$			100	µA
Output characteristic $V_{1,2} = 9\text{-}15$ V; $V_3 = 7.8$ V	$\Delta I_{1,2}$			200	µA
UHF switching voltage $V_{I(u)} = -25$ dBm $V_0 \geqq -5$ dBm; $f_{IF} = 38.9$ MHz	$V_{14\,UHF}$	7		16	V
VHF switching voltage $V_{I(u)}{}^*) = -25$ dBm $V_0 \leqq -30$ dBm; $f_{IF} = 38.9$ MHz	$V_{14\,VHF}$	0		3	V
Mixer gain Bd I; $V_{I(RF)} = -40$ dBm; $f_{RF} = 60$ MHz; $f_{IF} = 36.15$ MHz; $R_{G12/13} = 100\ \Omega$; refer to response characteristic	G_{60}	23	27	31	dB
Mixer gain Bd III; $V_{I(RF)}{}^*) = -40$ dBm; $f_{IF} = 36.15$ MHz; $R_{G12/13} = 100\ \Omega$; refer to response characteristic	G_{220}	23	27	31	dB
Mixer noise Bd I, white noise $R_{G12/13} = 100\ \Omega$; refer to response characteristic	NF_{60}			13	dB
Mixer noise Bd III; white noise $R_{G12/13} = 100\ \Omega$; refer to response characteristic	NF_{220}			14	dB
Gain UHF input $V_{I(u)}{}^*) = -40$ dBm; $V_{14} = 12$ V; $f_{RFU} = f_{IF} = 36.15$ MHz; $R_{G11} = 200\ \Omega$; refer to response characteristic	G_{UHF}	31	35	39	dB

*) $V_{I(u)}$, $V_{I(RF)}$ } Input voltage if the generator is terminated with a load resistor of 50 Ω

Characteristics ($V_S = 12V^*$); $V_3 = 7.5$ V; $T_{amb} = 25$ °C)

		min	typ	max	
Noise figure UHF input $V_{14} = 12$ V; white noise $R_{G11} = 200\ \Omega$; refer to response characteristic	NF_{UHF}			7	dB
Oscillator turn-on drift $V_{tun} = 28$ V; $t = 0 - 500$ ms; Bd II; $f_{OSC} = 216$ MHz	f_{OSC}	−10		−250	kHz
Oscillator turn-on drift $V_{tun} = 28$ V; $t = 0 - 10$ s; Bd II; $f_{OSC} = 216$ MHz	f_{OSC}	−10		−450	kHz

Additional application data

Differential input resistance[1])	$R_{12/13}$		3		kΩ
Differential input capacitance[1])	$C_{12/13}$		2.7		pF
IF input resistance[1])	R_{15}		2		kΩ
IF input capacitance[1])	C_{15}		3.9		pF
UHF input resistance[1])	R_{11}		2.2		kΩ
UHF input capacitance[1])	C_{11}		3.4		pF
Interference voltage resistance Bd I $m_N = 1\%$; $m_{int} = 80\%$; $f_{int} = f_N \pm 10$ MHz $f_{mod} = 1$ kHz; $f_N = 65$ MHz	$V_{int12/13}$		140		mV_{rms}
Interference voltage resistance Bd II $m_N = 1\%$; $m_{int} = 80\%$; $f_{int} = f_N \pm 10$ MHz $f_{mod} = 1$ kHz; $f_N = 220$ MHz	$V_{int12/13}$		100		mV_{rms}

1) Measured S parameter values converted to Y parameter

*) Unless otherwise specified under test conditions

Circuit description

The TUA 2002-2 contains a symmetrical mixer input, as well as a multiplicative mixer. The oscillator amplitude is regulated. All oscillator operating currents and voltages are stabilized, so that the oscillator's amplitude and frequency are largely independent of temperature and operating voltage changes.

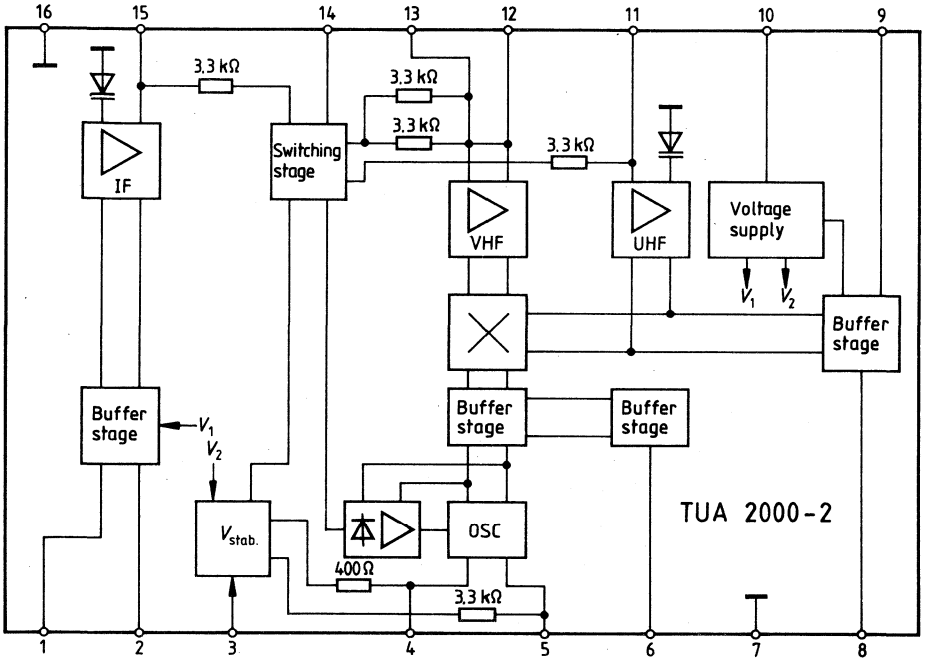
The IF amplifier has been provided with a high impedance input.

The output has two open collector connections.

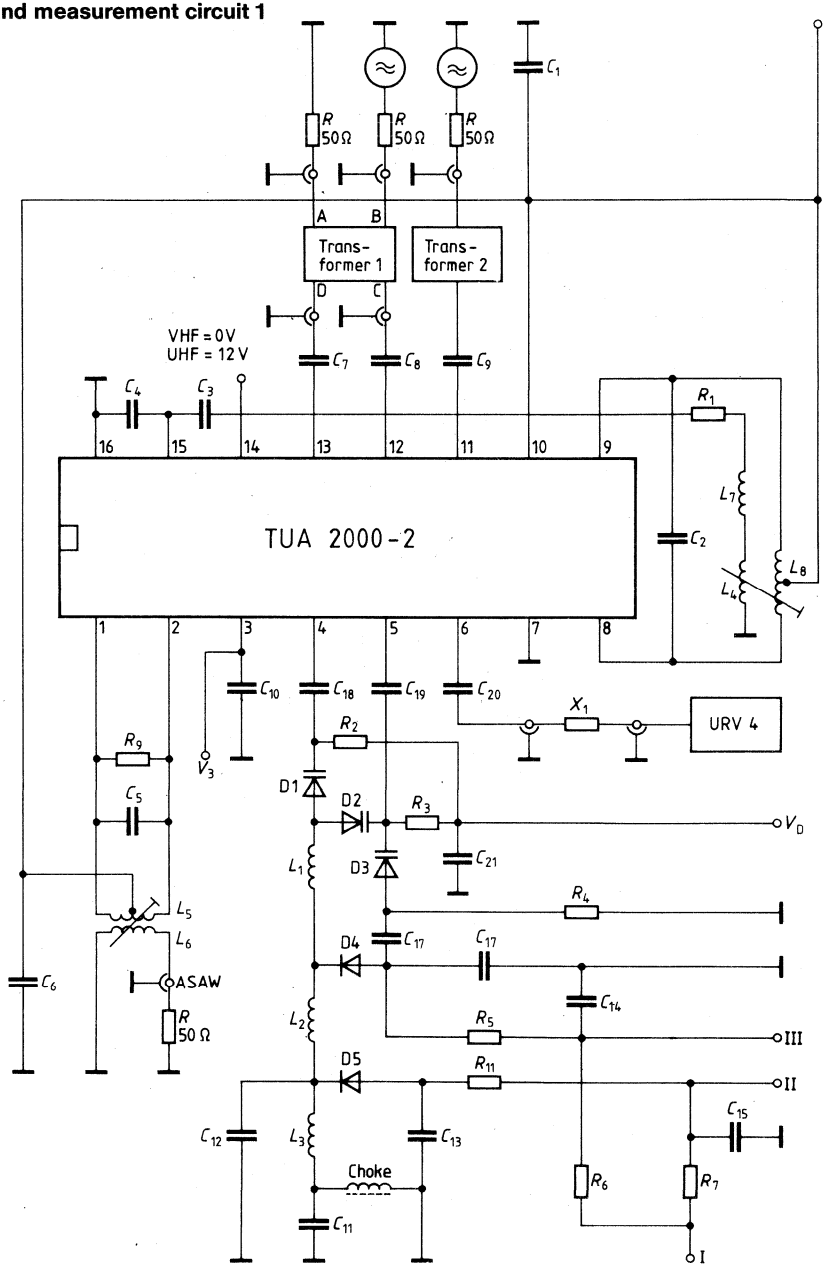
During UHF operation, oscillator and mixer are switched off and the UHF IF input coupling stage is activated.

Pin No.	Function
1	"Open collector" output of the IF SAW driver
2	"Open collector" output of the IF SAW driver
3	Input for external reference voltage
4	Low-ohmic collector output to the high reference point of a parallel resonant circuit
5	High-ohmic base input to the high reference point of a parallel resonant circuit
6	Oscillator signal output for counter connection
7	Ground
8	"Open collector" output of the mixer
9	"Open collector" output of the mixer
10	Supply voltage
11	Asymmetrical IF signal input for the UHF-IF signal
12	Mixer high impedance differential input
13	Mixer high impedance differential input
14	Switching voltage input for the VHF-UHF switch selection
15	Asymmetrical signal input of the IF SAW amplifier
16	Ground

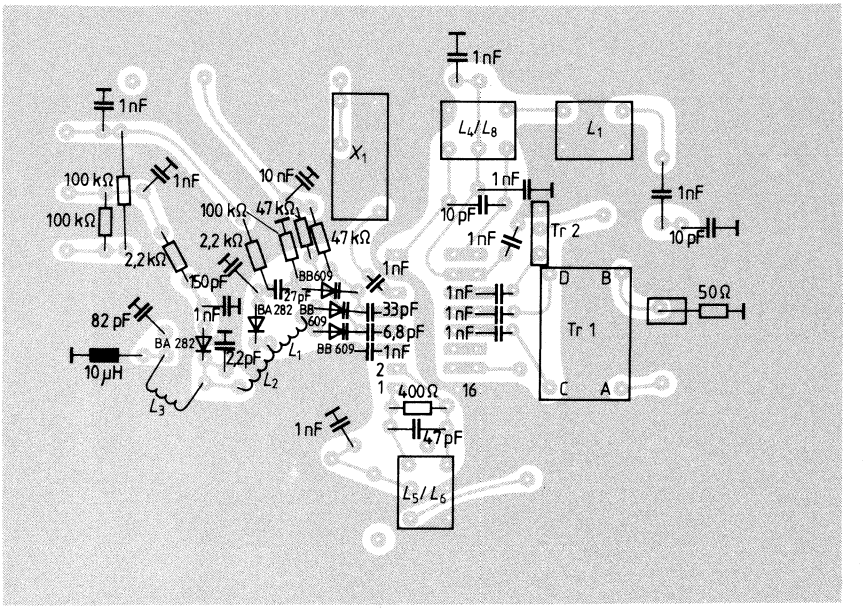
Block diagram



Test and measurement circuit 1



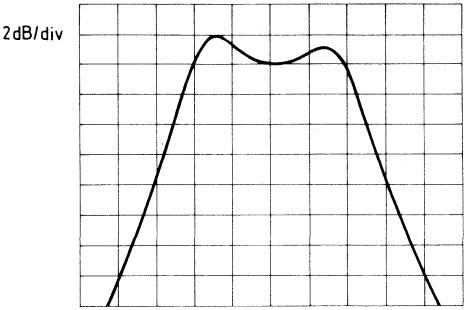
Plug-in location plan



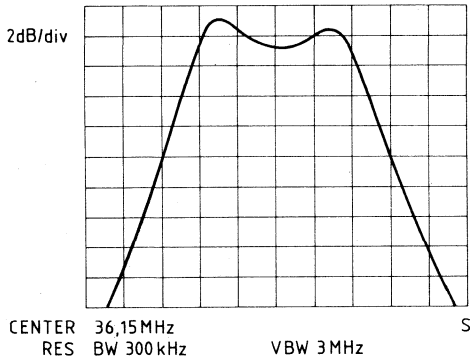
PCB layout of test and measurement circuit 1

Notes on test and measurement circuit 1

Response of passband curve for operation in VHF band I
$f_{RF} = 60$ MHz ± 10 MHz; $V_{14} = 0$ V; $V_{I(RF)} = -40$ dBm; ref. level = −10 dBm
gain test point $f_{RF} = 60$ MHz; $f_{IF} = 36.15$ MHz



Response of passband curve for operation in VHF band III
$f_{RF} = 220$ MHz ± 10 MHz; $V_{14} = 0$ V; $V_{I(RF)} = -40$ dBm; ref. level = −10 dBm
gain test point $f_{RF} = 220$ MHz; $f_{IF} = 36.15$ MHz



Response of passband curve for operation in VHF IF position
f_{RFU} = 36.15 MHz ± 10 MHz; V_{14} = 12 V; $V_{I(RF)}$ = −40 dBm; ref. level = 0 dBm
gain test point $f_{RFU} = f_{IF}$ = 36.15 MHz

Explanations to diagrams

2 dB/div	= 2 dB/division on Y axis
Center 36.15 MHz	= center frequency of display at IF = 36.15 MHz
RES BW 300 kHz	= resolution bandwidth of spectrum analyzer is 300 kHz in its IF section
VBW 3 MHz	= video bandwidth in IF section of spectrum analyzer is 3 MHz
SPAN 20.00 MHz	= overall display range of diagram is 20 MHz, i.e. 2 MHz/division on X axis
SWP 75 sec	= sweep time on X axis is 75 s
Ref. level	= reference level is uppermost horizontal line of diagram

To test and measurement circuit 1

On path pin 4 – C18 – D1 – D2 – C19 – pin 5 ensure minimal lead inductance for the suppression of parasitic series resonance outside of the oscillator's useful band.

Transformer Tr 1:

Tr 1 = ANZ ac = HH-109 30 to 500 MHz
C = 0°; R_{gC} = 50 Ω
D = 180°; R_{gD} = 50 Ω

Transformer Tr 2:

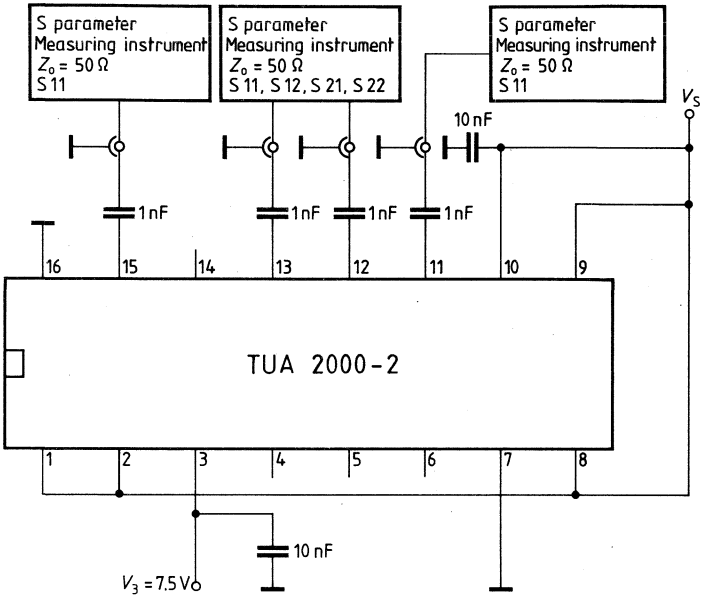
50/200 Ω unbalanced
3 turns bifilar on core material
B62152-A7-X1

Attenuator: X1 = 6 dB

Bd I 58 to 85 MHz
Bd II 110 to 216 MHz
Bd III 200 to 400 MHz

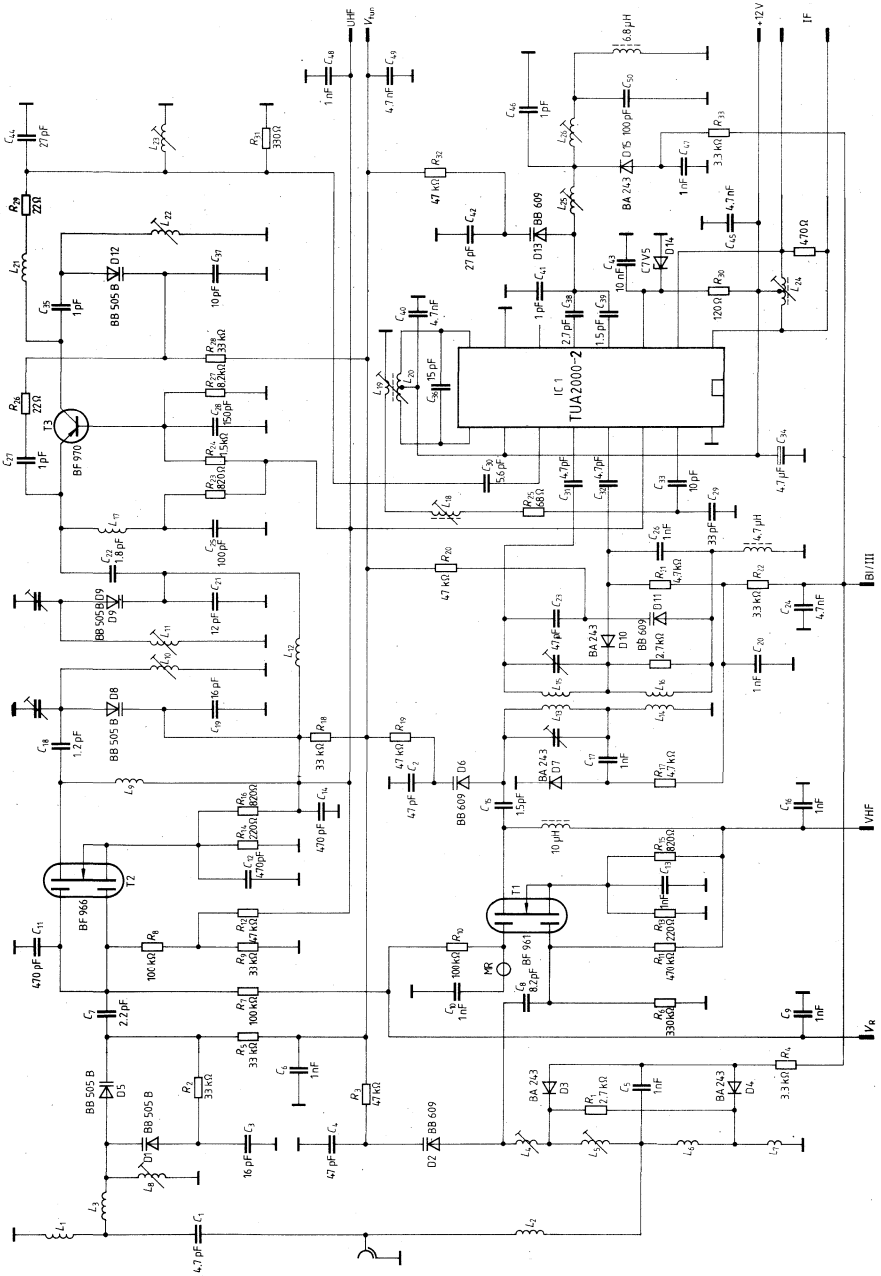
	I	II	III
Band I	−12 V	X	X
Band II	−12 V	+12 V	X
Band III	−12 V	+12 V	+12 V

Test and measurement circuit 2

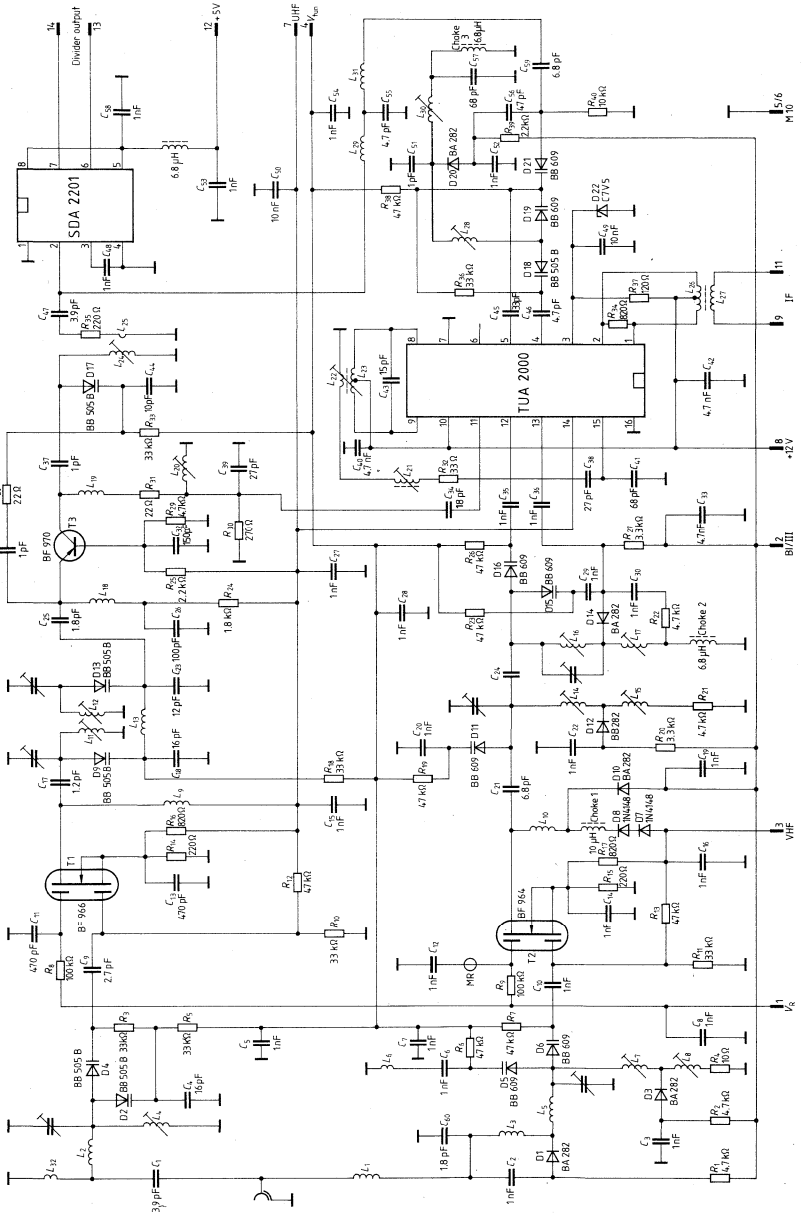


For the determination of the input admittance values of pins 11, 12, 13, 15

Application circuit 1



Application circuit 2



Bipolar circuit

Type	Ordering code	Package outline
UAA 170	Q67000-A940	DIP 16

IC for driving 16 light emitting diodes. Depending on the input voltage, the individual LEDs are driven within one row in form of a light spot. The UAA 170 provides a linear relation between control voltage and the driven LED.

By using an appropriate circuitry, the brightness of the LEDs can be varied and the crossing over of the light spot can be set between "smooth" and "abrupt". By connecting two ICs in parallel, up to 30 LEDs can be driven.

Maximum ratings

Supply voltage	V_S	18	V
Input voltages	V_{11}, V_{12}, V_{13}	6	V
Load current	I_{14}	5	mA
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	90	K/W

Operating range

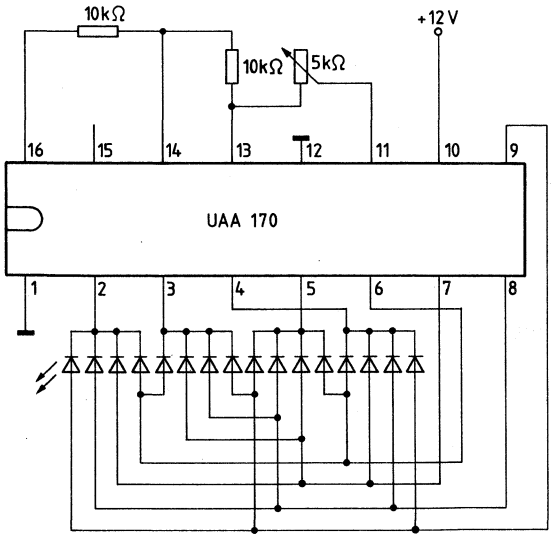
Supply voltage range (LED red)[1]	V_S	11 to 18	V
Ambient temperature range	T_{amb}	−25 to 85	°C

1) The lower limit only applies to a forward voltage of the LEDs of approx. 1.5 V (red LEDs); the lower limit increases with higher forward voltage

Characteristics ($V_S = 12$ V; $T_{amb} = 25$ °C)

		min	typ	max	
Current consumption ($I_{14} = 0$; $I_{16} = 0$)	I_S	2	4	10	mA
Control input current	I_{11}	−2			µA
Reference input current	I_{12}, I_{13}	−2			µA
Voltage difference	$\Delta V_{12/13}$	1.4		6	V
Voltage difference for smooth light transition	$\Delta V_{12/13}$	1.4			V
Voltage difference for abrupt light transition	$\Delta V_{12/13}$	4			V
Voltage difference	$\Delta V_{12/13}$	4			V
Stabilized voltage $I_{14} = 300$ µA	V_{14}		5	6	V
$I_{14} = 5$ mA	V_{14}	4.5			V
Reference input voltage	$V_{ref\,max}$	1.4		6	V
	$V_{ref\,min}$	0		4.6	V
Tolerance of forward voltages of LEDs, mutually	ΔV_D			0.5	V
Output current for LEDs	ΣI_D		25		mA

Test circuit



Scale display with light emitting diodes

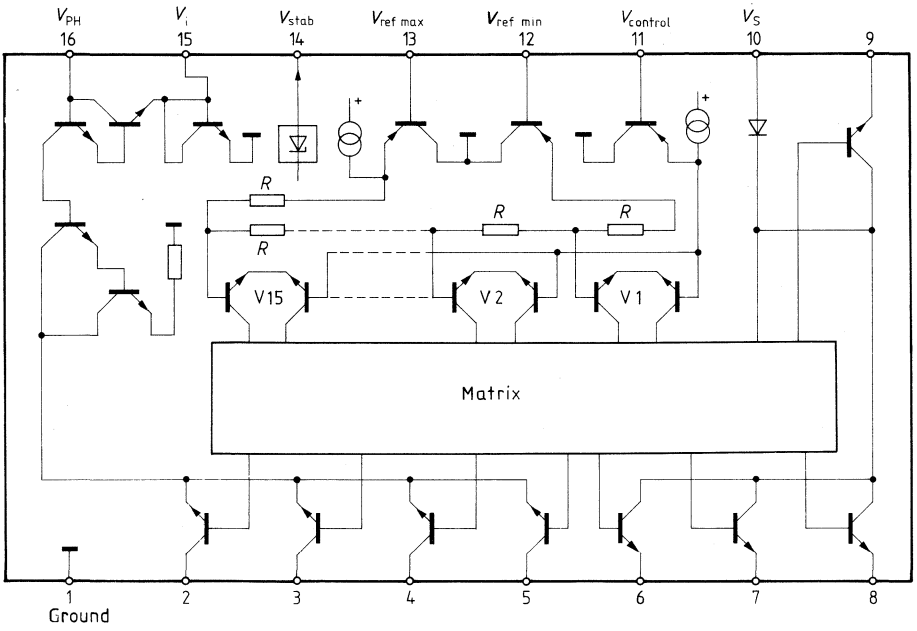
Scale displays by means of a wandering light spot are particularly suitable for indicating approximate values. Applications of this kind are level sensors, VU-meters, tachometers, radio scales etc. When applying the displays in measuring equipment, multicolored light emitting diodes can be used as range limitation. Ring scales are obtained by a circular arrangement of the diodes. The IC UAA 170 has especially been developed for driving a scale of 16 LEDs.

The input voltages at pins 11, 12 and 13 are freely selectable between 0 and 6 V. Any kind of adjustment becomes possible by suitable voltage drivers. The DC value $V_{control}$ is always assigned to a certain spot of the diode chain.

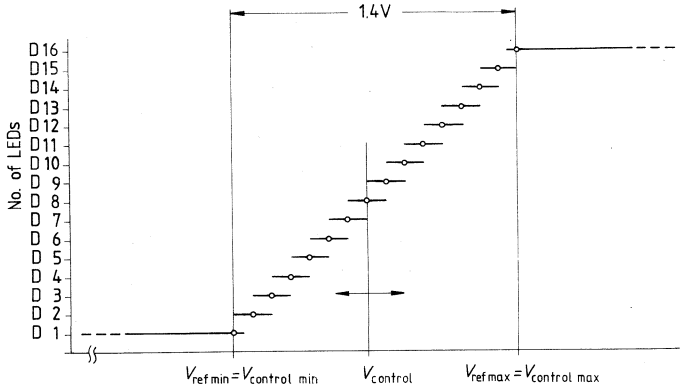
The voltage difference between pins 12 and 13 thereby corresponds to the possible indication range. $\Delta V_{12/13}$ defines at the same time the light transition between two diodes. With $\Delta V_{12/13}$ approx. 1.4 V, the light point glides smoothly along the scale. With increasing voltage difference, the passage becomes more abrupt. With $\Delta V_{12/13}$ approx. 4 V, the light point jumps from diode to diode.

Input voltages beyond the selected indication range cause the diodes D1 or D16 respectively, to light up, identifying only that the range has been exceeded.

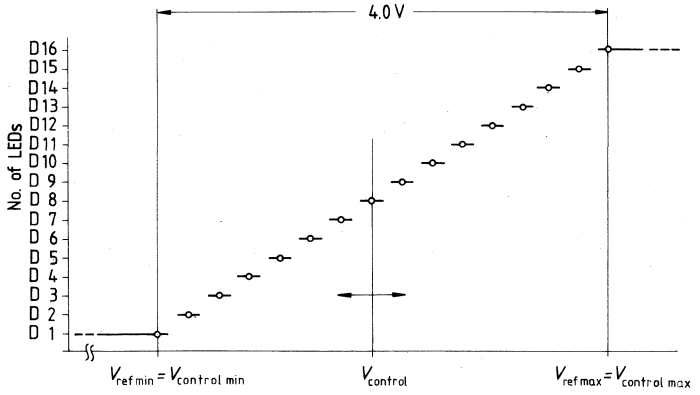
Block diagram



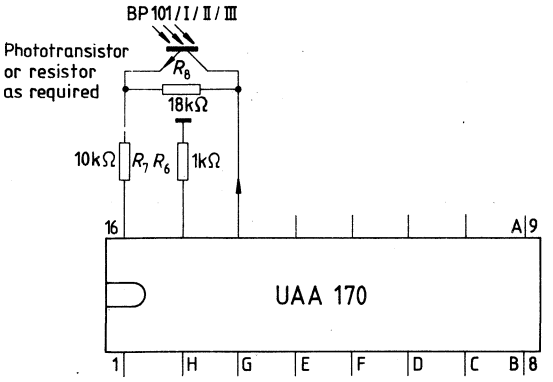
Indication for smooth transition UAA 170



Indication for abrupt transition UAA 170



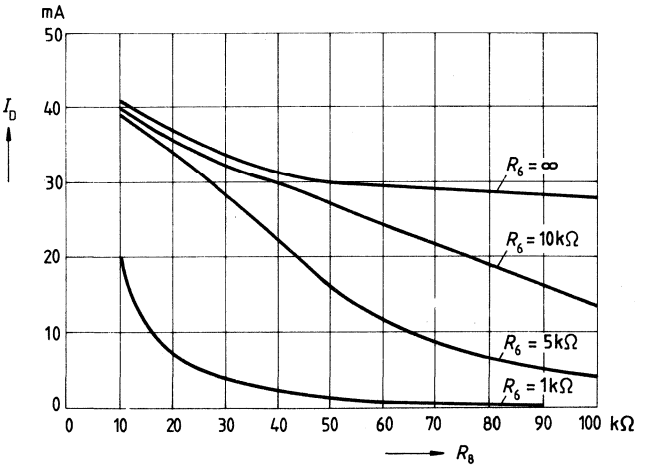
Brightness control



Pins 14, 15, and 16 serve to determine the diode current. Corresponding to the desired light intensity, the forward current of the diodes is linearly variable in the range I_f approx. 0 to 50 mA. The resistance at pin 15 defines the adjusting range. The resistances between pin 14 and 16 determine the current.

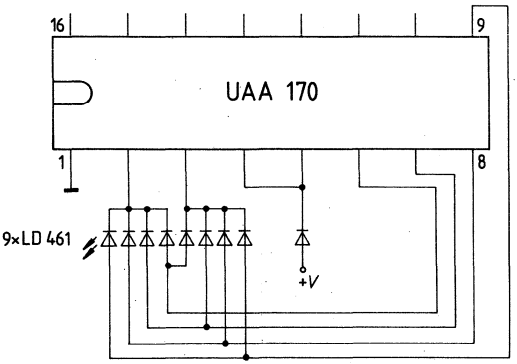
With the aid of a phototransistor, such as BP 101, the light intensity of the LEDs can be adjusted to the light fluctuations of the environment.

Diode current versus base emitter resistance
$V_S = 12$ V; $T_{amb} = 25$ °C; $V_{14} = 5.4$ V; red LEDs

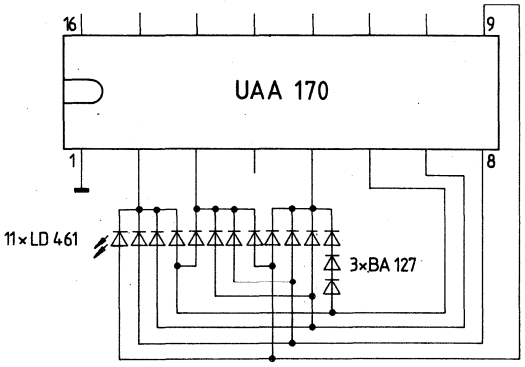


Operation of less than 16 LEDs

Control of 9 LEDs

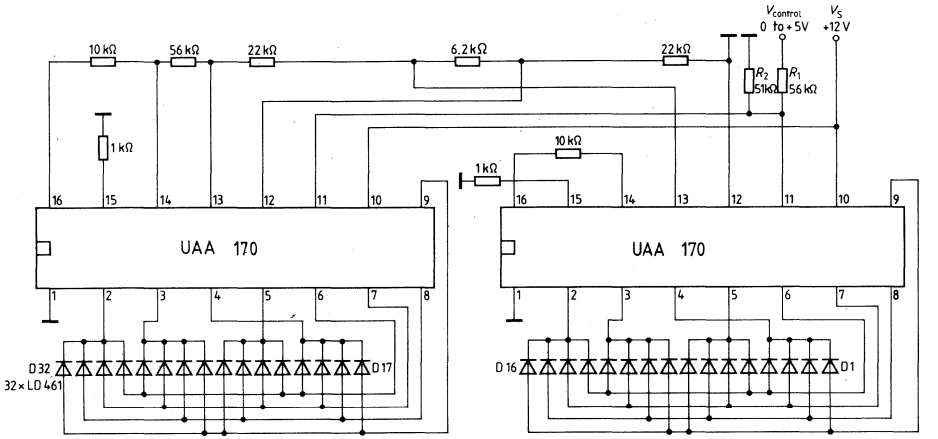


Control of 11 LEDs



Application circuit for the control of 30 LEDs with 2 x UAA 170

Range of control voltage $V_{control} = 0$ to 5 V
Voltage difference $V_{12/13} = 2 \times 1.2\ V = 2.4\ V$
Since the diodes D16 or D17 are permanently lit when the maximum or minimum voltages V_{13} or V_{12} adjusted by R_3, R_4, R_5, are exceeded or fall short the diodes should be covered, if necessary.



The figure shows an expansion of the circuit to 30 diodes with 2 ICs UAA 170. The diodes D16 or D17 light permanently, when the reciprocal absolute ratings are exceeded. They should be covered. The reference voltage $\Delta V_{12/13} = 2 \times 1.2 = 2.4$ V is derived from a stabilized dc voltage of typ. 5 V available at pin 14. A resistance of 6.2 kΩ provides an overlapping of the ranges in order to ensure a smooth transition from D15 to D18. The control voltage $V_{control}$ is forwarded in a parallel mode to pins 11 via a divider $R_1 : R_2$. The voltage divider is to be dimensioned according to the desired input voltage. With a divider current of $I = 100\ \mu A$ and a control voltage of $V_{control} = 10$ V, the following is valid:

$$R_2 = \frac{\Delta V_{12/13}}{I} = \frac{2.4}{0.1} = 24\ k\Omega \text{ and}$$

$$R_1 = \frac{V_{control} - \Delta V_{12/13}}{I} = \frac{7.6}{0.1} = 76\ k\Omega$$

The nearest standard value is $R_1 = 75$ kΩ. The voltage difference for switching an incremental step is then $\Delta V_{control} = \frac{10\ V}{30} = 0.16\ V$.

Bipolar circuit

Type	Ordering code	Package outline
UAA 180	Q67000-A1104	DIP 18

Integrated circuit for driving 12 light emitting diodes. Corresponding to the input voltage the LEDs forming a light band are controlled similar to a thermometer scale.

By using an appropriate circuitry the brightness of the LEDs can be varied and the light passage between two adjacent LEDs can be arranged between "smooth" and "abrupt".

Maximum ratings

Supply voltage	V_S	18	V
Input voltage	V_3	6	V
	V_{16}	6	V
	V_{17}	6	V
Storage temperature range	T_{stg}	−40 to 125	°C
Junction temperature	T_j	150	°C
Thermal resistance (system-air)	$R_{th\,SA}$	78	K/W

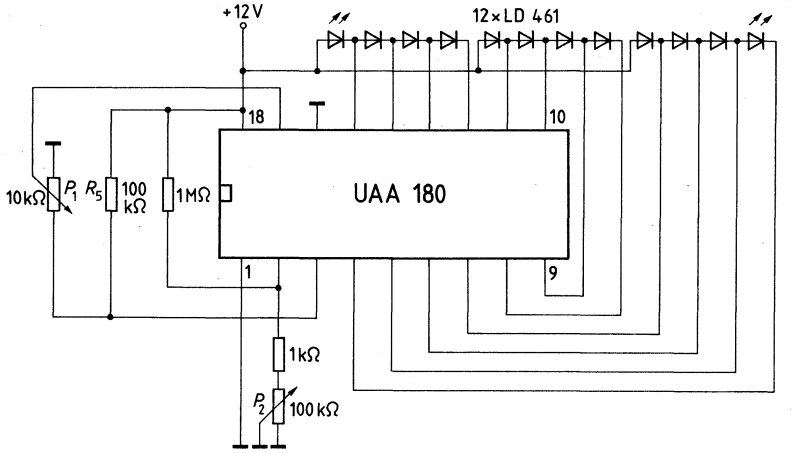
Operating range

Supply voltage range	V_S	10 to 18	V
Ambient temperature range	T_{amb}	−25 to 85	°C

Characteristics ($V_S = 12$ V, $T_{amb} = 25$ °C)

		min	typ	max	
Current consumption ($I_2 = 0$) (without LED current)	I_{18}		5.5	8.2	mA
Input currents ($V_3 - V_{16} < 2$ V)	I_3		0.3	1	µA
	I_{16}		0.3	1	µA
	I_{17}		0.3	1	µA
Voltage difference for smooth light transition	$V_{16/3}$	1			V
Voltage difference for abrupt light transition	$V_{16/3}$	4			V
Diode current per diode	I_D		10		mA
Tolerance of LED forward voltages	ΔV_D			1	V

Measurement circuit



P_1 light band test
P_2 brightness test

Scale display with light emitting diodes

Scale displays by means of a growing light band are particularly suitable for the measuring of approximate values. Applications of this kind are level sensors, VU meters, tachometers, field strength indicators etc. When applying the displays in measuring equipment, multi-colored LEDs can be used as range limitation.

The voltage difference between pins 16 and 3 thereby corresponds to the possible indication range. $\Delta V_{16/3}$ defines at the same time the light passage between two diodes. With $\Delta V_{16/3} \geqq 1$ V, the light band glides smoothly along the scale. With increasing voltage difference, the passage becomes more abrupt. With $\Delta V_{16/3}$ approx. 4 V, the light band jumps from diode to diode.

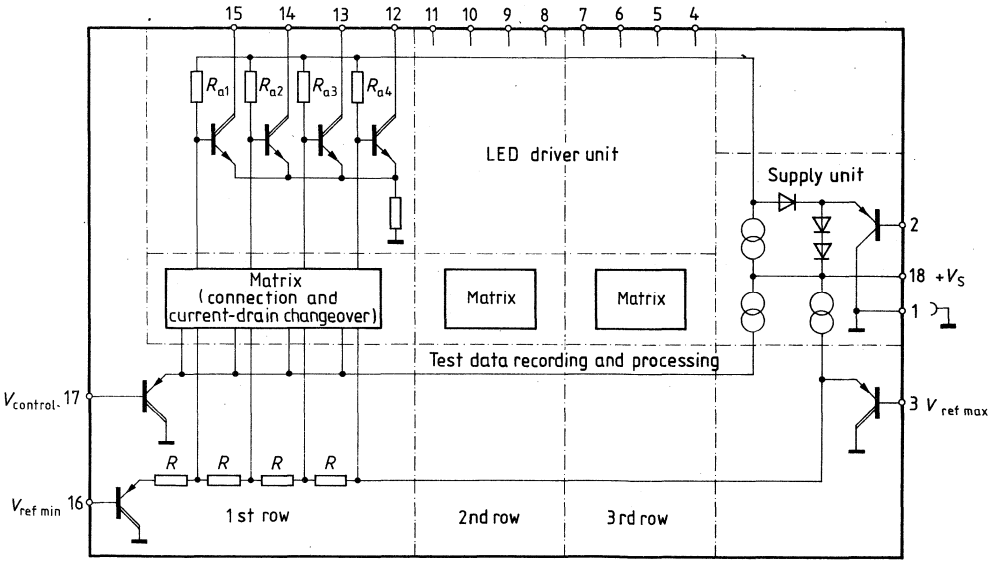
Each quartet must consist of identical diodes in order to maintain its functional characteristics.

It is therefore possible to design the first and third quartet as diodes emitting the color red and the second quartet as diodes emitting the color green to delineate a certain operational area.

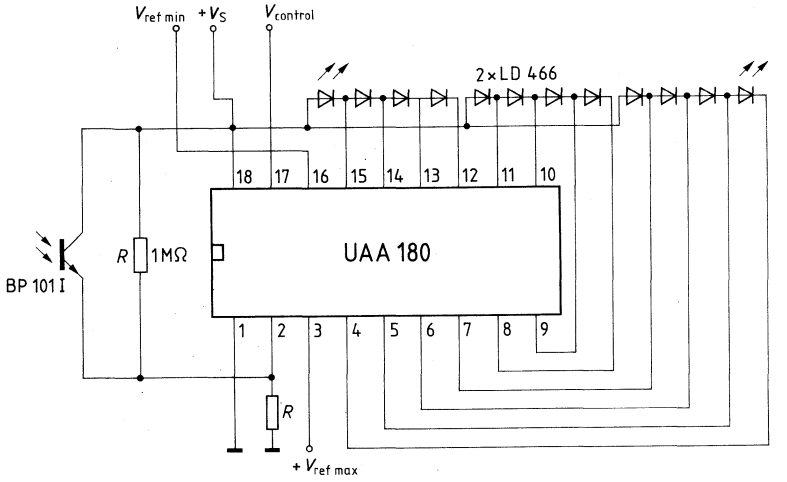
Pin 2 serves to determine the diode current. Corresponding to the desired light intensity, the forward current of the diodes is variably linear in the range I_f approx. 0 to 10 mA.

Application circuit 1 shows the possibility of designing this resistance, adjustable by means of a phototransistor BP 101, in order to adapt the light intensity to changing ambient brightness. The adjusting range of the diode current lies between I_f approx. 5 mA (BP 101 not lit) and I_f approx. 10 mA (BP 101 fully lit). If pin 2 is open the diode current is 10 mA.

Block diagram



Application circuit 1

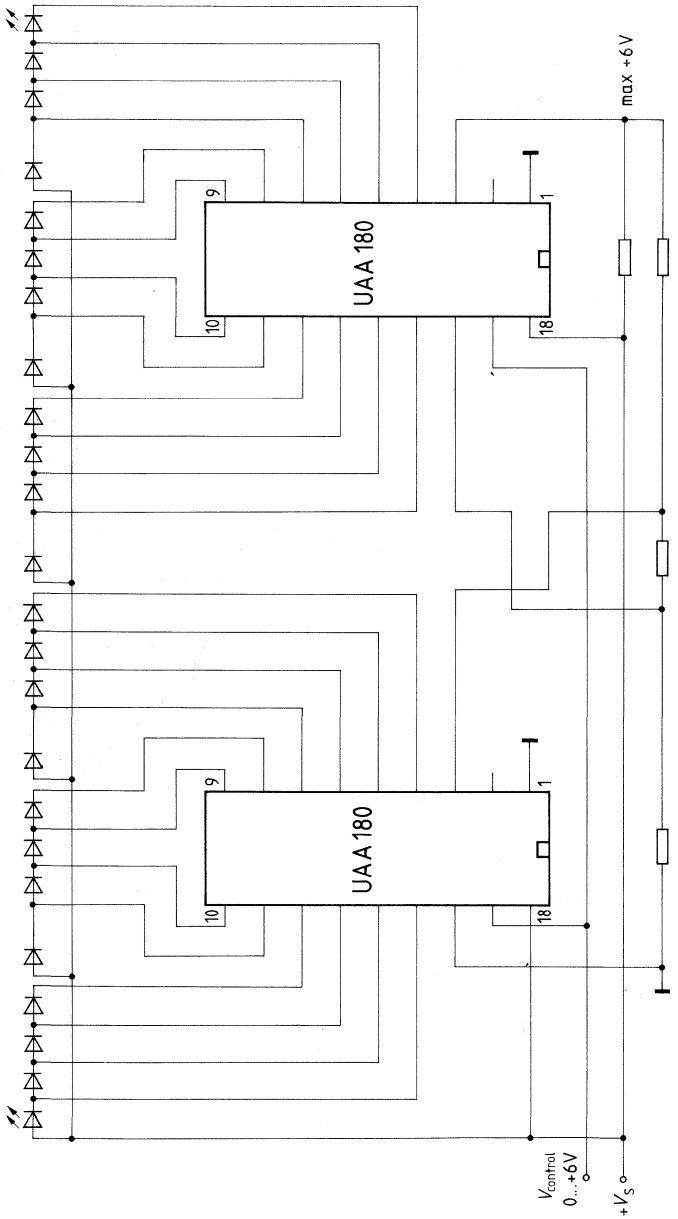


Depending on the actual maximum ratings, the resistances R_1 to R_7 can be varied widely as follows:

$R_3 = 820\ \Omega$
$R_4 = 56\ k\Omega$
$R_5 = 220\ k\Omega$
$R_6 = 2.2\ k\Omega \ldots 100\ k\Omega$

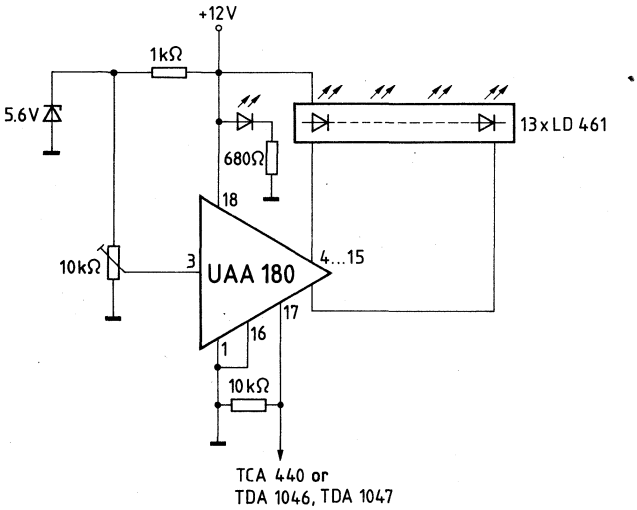
If a quartet does not need the full number of display diodes and if the first wired diodes shall be left luminous at full driving, bridges have to be inserted replacing the missing LEDs. Otherwise the first diodes of the quartet switch off when their display range is exceeded.

Application circuit 2
for cascading several UAA 180 ICs (up to 7)



Application circuit 3

for field strength indication



System Descriptions

Brief description

The SDA 210 is a modular frequency synthesis tuning and operating system with two selectable microcomputers SDA 2010, SDA 2110 and at least four further system components. The SDA 2110 with 28 pins is a cost effective version with standby operation.

SDA 220 and SDA 230 are derived from the system SDA 210 and make use of the same system components. The difference in these systems is defined by the corresponding microprocessors. SDA 220 uses the SDA 2020 with 1 KByte program memory. The SDA 2030 with 2 KByte memory is provided for SDA 230. That means both microcomputers are function and pin compatible. The basic system offers up to 30 program memory locations and the possibility to store 4 analog values, direct channel access for 100 channels, control interface for videotext operation and the option to indicate program/channel number on a two-digit LED display.

Microcomputer and system components:

System	SDA 210	SDA 220	SDA 230
Microcomputer	SDA 2010 SDA 2110	SDA 2020	SDA 2030
Divider	SDA 2101/SDA 2201/SDA 2311		
PLL	SDA 2112-2		
Nonvolatile memory	SDA 2006, SDA 2116		
Static LED driver	SDA 2131		

Two additional components enable an IR remote control of all TV and videotext functions.

IR transmitter	SDA 2008, SDA 2208
IR preamplifier	TDA 4050 B

If requested, program and channel numbers can be indicated by two separate double digit LED displays or can be displayed on the screen of a TV set. For this the following integrated circuits are needed:

MUX LED driver	SDA 2014
Onscreen IC	SDA 2005

The modular structure of this computer-controlled system is not only based on the number and type of the applied integrated circuits, but also on the computer software. Since the operational design for TV functions varies from manufacturer to manufacturer, the computer software program includes multiple solutions, which can be implemented by programming diodes.

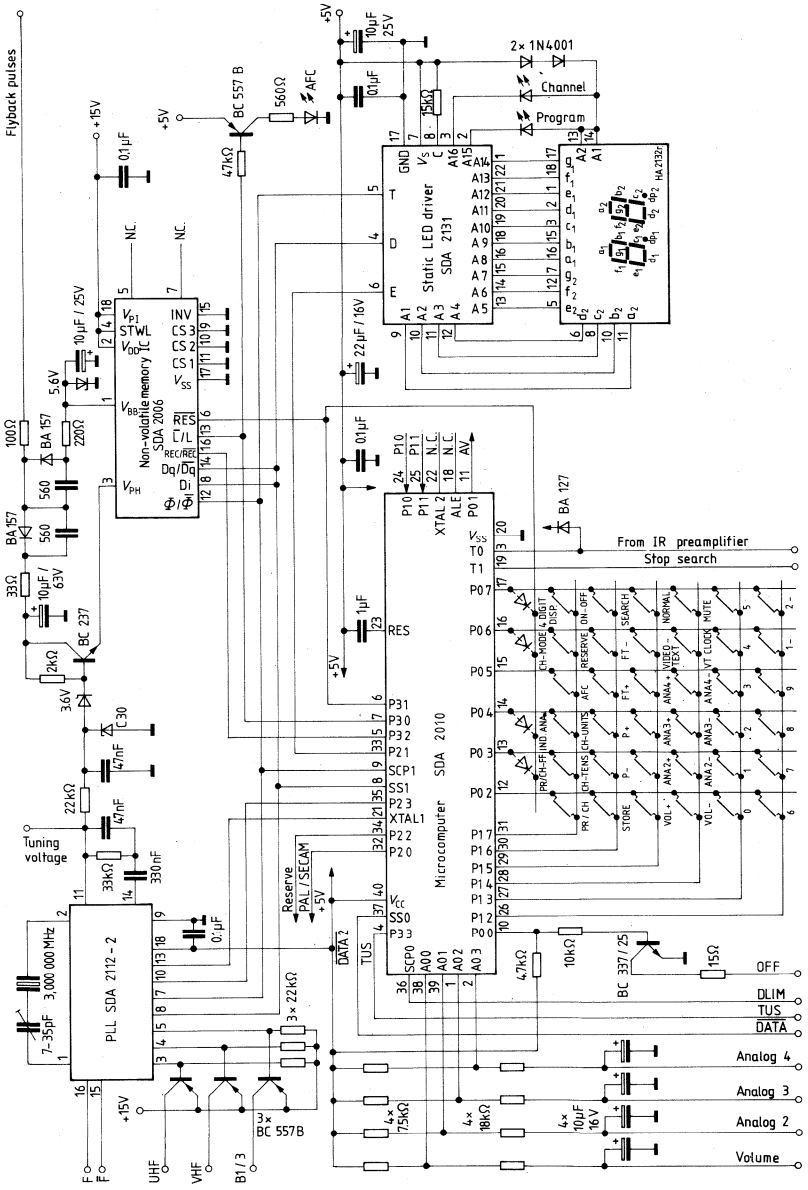
The unusually extensive console and remote control keyboard matrix, which enables the user to select the most efficient instructions, also adds to the flexibility of the system. The modular hardware and software concept of this new IC package allows the manufacturer to develop customer-specific frequency synthesis tuning systems with cost-effective standard ICs.

Test aids for microcomputer

The piggy-back components SDA 3010 and SDA 3110 enable field tests under definite conditions. With plugged-in EPROM SAB 2716 the SDA 3010 or SDA 3110 acts as the requested mask programmed version.

Configuration

Block diagram



Siemens Digital Tuning System (Frequency Synthesis) for CATV Converters — SIECON 21 M

SIECON 21 M is a cost-optimized modular frequency synthesis tuning system for CATV converters.

It is possible to set up to 2 x 63 cable channels on the TV intermediate frequeny of 612.75 MHz.

The corresponding TV channel is seized by a further converter with fixed frequency.

The program covers the US standards STANDARD and HCR (Harmonically Related Carries).

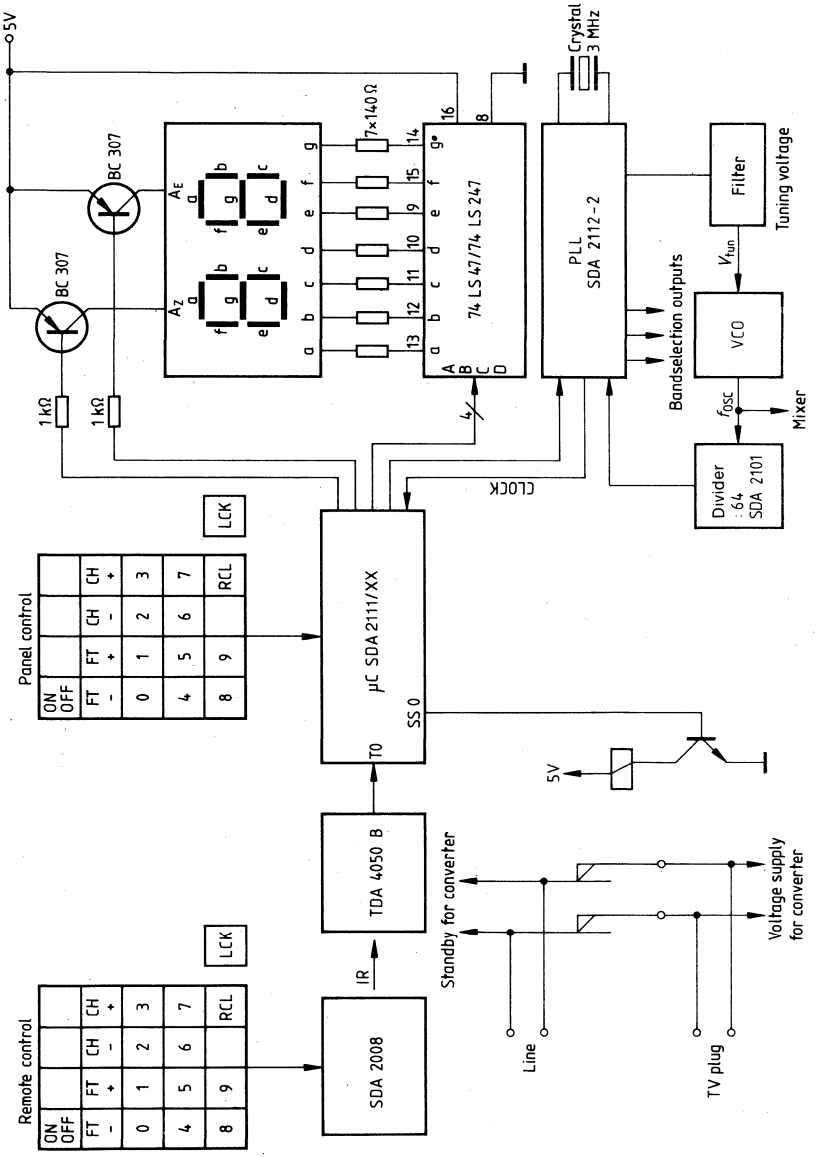
The microprocessor SDA 2110 ensures the selection of the appropriate cable tuner in the system.

All necessary functions of the cable converter are controllable either by a keyboard at the device or by an IR remote control. The SDA 2110 as a receiver processes the incoming IR signals directly.

Components of the system

PLL	SDA 2112-2
Divider	SDA 2101
Microcomputer	SDA 2110
IR transmitter	SDA 2008
IR preamplifier	TDA 4050 B

Block diagram



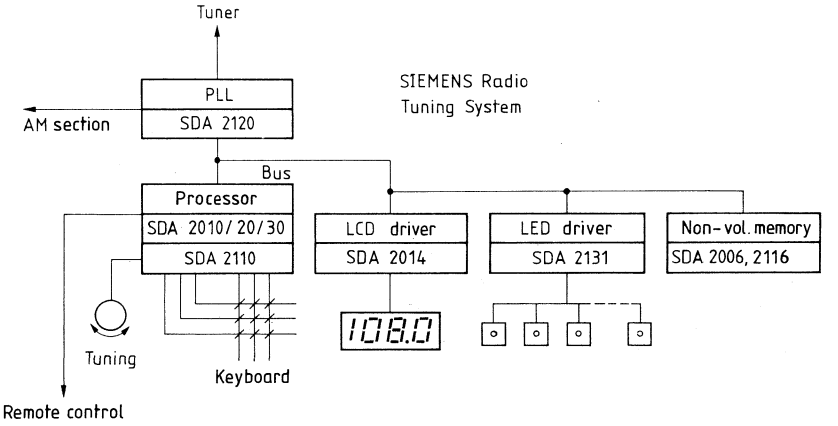
Siemens Digital Tuning System for Radio Application
Siemens Radio Tuning System (SRS)

Brief description

The definition Siemens Radio Tuning System includes a series of integrated circuits which have been developed specifically for the configuration of frequency synthesis tuning and operating systems for automobile and hi-fi stereo sector. The design includes a single chip microcomputer with its various options (SDA 2010, SDA 2020, SDA 2030 and SDA 2110, see also TV circuits), a static LED driver for 16 LED diodes (SDA 2131) as well as a MUX LED driver for two or four digit 7-segment display, a radio PLL for input frequencies up to 120 MHz (SDA 2120) and two optional nonvolatile station memories (SDA 2006, SDA 2116). All peripheral components can be connected to the microcomputer via a serial interface.

Furthermore, an extensive package of software modules is available. These modules can be combined by the device manufacturer into a user-specific program.

Block diagram



System for the Reception of Road Traffic Transmitters
(Car Driver Broadcasting Information – ARI)

S 0280
S 0281
S 551
S 552

In West Germany the so-called car driver broadcasting information (ARI) was introduced about 5 years ago.

This system is intended to provide the car driver with traffic information. For this purpose a particular identification frequency was assigned to the transmitters which broadcast messages intermittently, this transmitter signal includes the following three components.

1. Station decoding SK

Station decoding is used to locate a road traffic transmitter. For this purpose a 57 kHz pilot tone is superimposed on the normal AF signal.

2. Message decoding DK

In order to alert the car driver although he/she might be listening to cassette music or the loudness level has been lowered, a 125 Hz pilot tone is being transmitted during the message transmission. Thus, the message in the loudspeaker of the receiver is amplified.

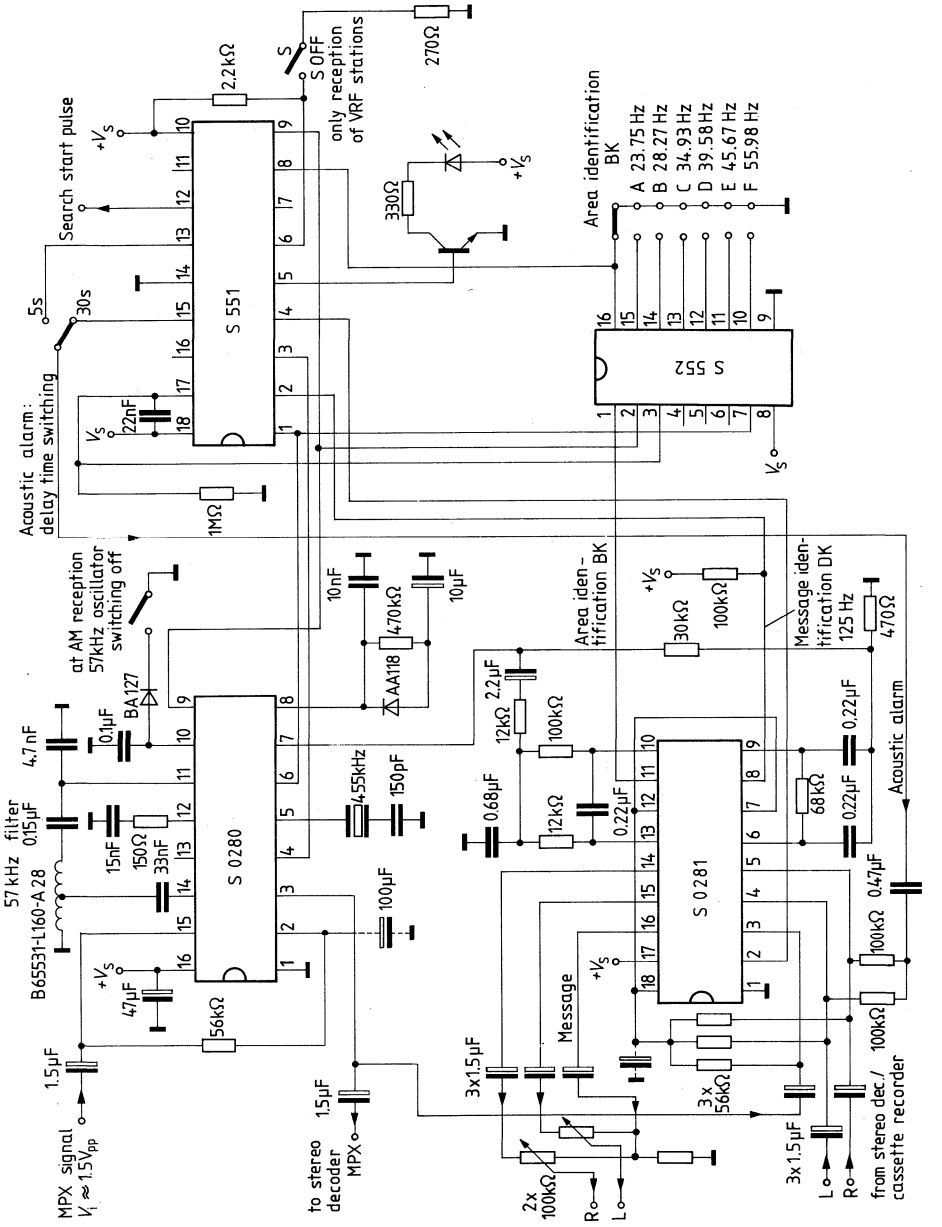
3. Area decoding BK

Since road traffic messages are transmitted regionally, the appropriate transmitter of the area referred to can be located by area decoding. For this purpose special frequencies in the range between 25 and 60 Hz are assigned to certain areas.

To decode road traffic broadcasting signals the ICs S 0280, S 0281, S 551, and S 552 are available.

Application of S 0280, S 0281, and S 551 results in a system which recognizes road traffic transmitters and transmits road traffic messages. If the system has been extended to the IC S 552, the regional frequencies of the VRF transmitters can be decoded and, thus, road traffic messages of preselected regions can be received.

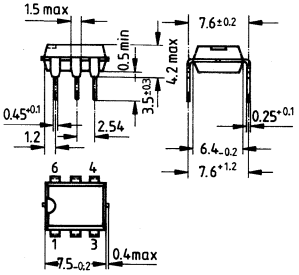
Application circuit for the reception of VRF transmitters with SK+DK+BK



Packaging Information

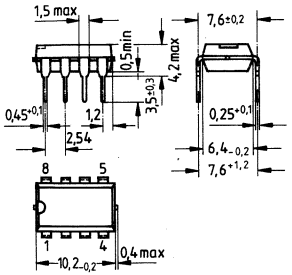
Package Outlines

Plastic plug-in package 20 A 6 DIN 41866,
6 pins, DIP



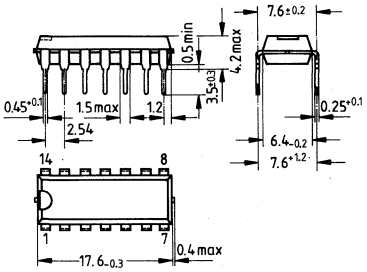
Approx. weight 0.7 g

Plastic plug-in package 20 A 8 DIN 41866,
8 pins, DIP



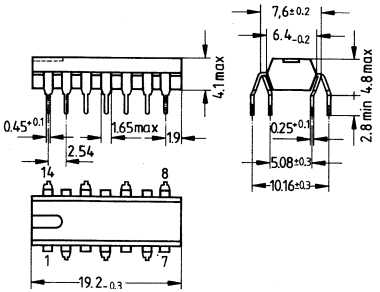
Approx. weight 0.7 g

Plastic plug-in package 20 A 14 DIN 41866,
14 pins, DIP



Approx. weight 1.1 g

Plastic plug-in package 20 C 14 DIN 41866,
14 pins, QUIP

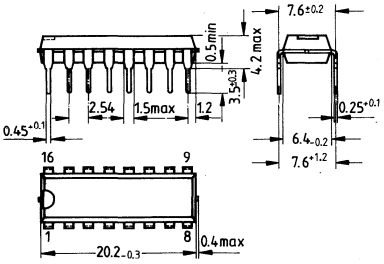


Approx. weight 1.1

Dimensions in mm

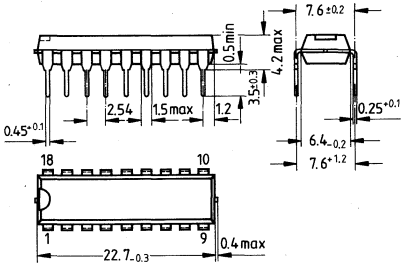
Package Outlines

Plastic plug-in package 20 A 16 DIN 41866, 16 pins, DIP



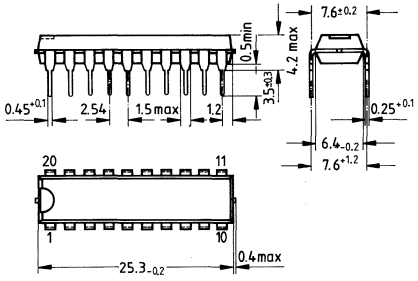
Approx. weight 1.2 g

Plastic plug-in package 20 A 18 DIN 41866, 18 pins, DIP



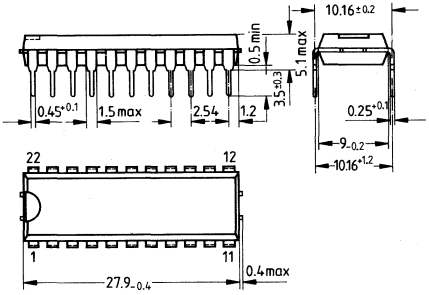
Approx. weight 1.3 g

Plastic plug-in package 20 A 20 DIN 41866, 20 pins, DIP



Approx. weight 1.5 g

Plastic plug-in package 20 D 22 DIN 41866, 22 pins, DIP

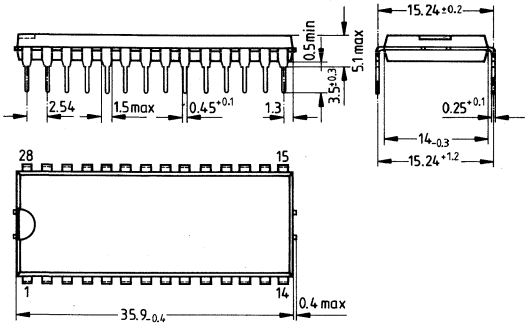


Approx. weight 2.1 g

Dimensions in mm

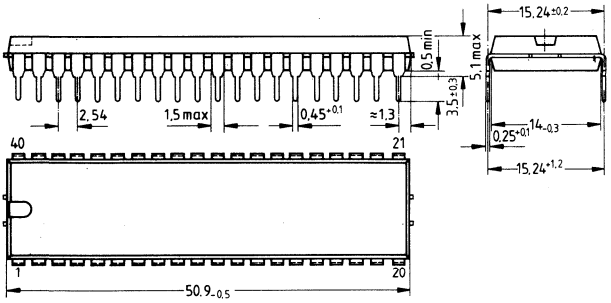
Package Outlines

Plastic plug-in package 20 B 28 DIN 41866,
28 pins, DIP



Approx. weight 3 g

Plastic plug-in package 20 B 40 DIN 41866,
40 pins, DIP

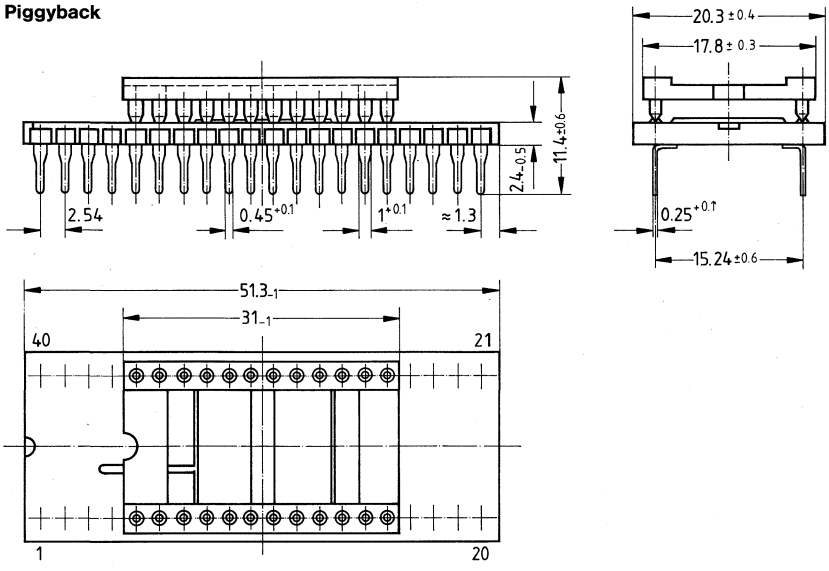


Approx. weight 5.9 g

Dimensions in mm

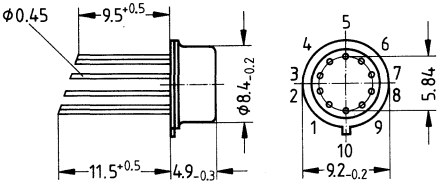
Package Outlines

Piggyback



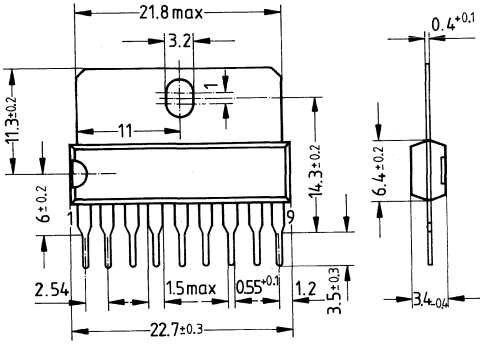
Dimensions in mm

Metal case 5 J 10 DIN 41873 (similar to TO-100)



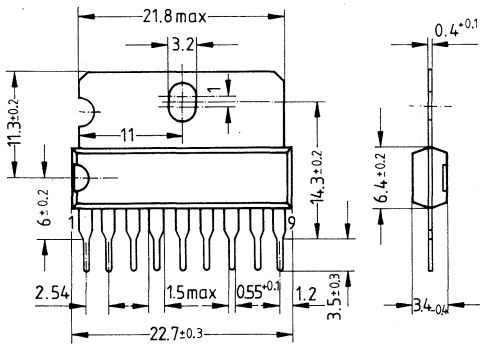
Approx. weight 1.1 g

Plastic power package
with cooling fin and 9 pins, SIP



Approx. weight 1.9 g

Plastic power package
with cooling fin and 9 pins, SIP
(TDA 4601 only)



Approx. weight 1.9 g

Dimensions in mm

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Contents
Summary of Types

General Information

Technical Data

System Descriptions

Packaging Information

List of Sales Offices

Ordering No. B/2749-101
Printed in Germany
KG 048410.